Family 10h
AMD Opteron™ Processor
Product Data Sheet

Publication # **40036**
Revision: **3.04**
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Revision History

Date	Revision	Description
June 2010	3.04	Fourth Public Release. • Added support for C32 package processors.
March 2010	3.03	Third Public Release. • Added support for G34 package processors. • Updated: Fr6 (1207) package processor features.

June 2009	3.02	Second Public Release.
		• Added support for:
		  • Socket Fr6 (1207) and Socket AM3 socket infrastructures.
		  • Fr6 (1207) and AM3 package processors.
		  • Rev D processors.
		• Updated: descriptions of LGA packages.

March 2009	3.00	Initial Public Release.

1 Family 10h AMD Opteron™ Processor Features

The following is a list of features and capabilities of the Family 10h AMD Opteron™ processor.

- **Compatible with Existing 32-Bit Code Base**
  - Including support for SSE, SSE2, SSE3, SSE4a, ABM, MMX™, 3DNow!™ technology and legacy x86 instructions
  - Runs existing operating systems and drivers
  - Local APIC on the chip
- **AMD64 Technology**
  - AMD64 technology instruction-set extensions
  - 64-bit integer registers, 48-bit addresses
  - Sixteen 64-bit integer registers
  - Sixteen 128-bit SSE/SSE2/SSE3/SSE4a registers
- **Multi-Core Architecture**
  - Twelve-core, eight-core, six-core, or quad-core options*
    * Six-core option available in Fr6 (1207) and C32 package processors; twelve-core and eight-core options available in G34 package processors
  - AMD Balanced Smart Cache
    - Discrete L1 and L2 cache structures for each core
    - Shared L3 cache structure
- **Machine-Check Architecture**
  - Includes hardware scrubbing of major ECC-protected arrays
  - Improved Fault-Avoidance Support for L3 cache (supported by Rev C and later processors)
- **Cache Structures**
  - **64-Kbyte 2-Way Associative ECC-Protected L1 Data Cache**
    - Two 64-bit operations per cycle, 3-cycle latency
  - **64-Kbyte 2-Way Associative Parity-Protected L1 Instruction Cache**
    - With advanced branch prediction
  - **512-Kbyte 16-Way Associative ECC-Protected L2 Cache**
    - Exclusive cache architecture storage in addition to L1 caches
    - TLB support for 1-Gbyte pages (supported by Rev C and later processors)
  - **6128-Kbyte (6-Mbyte)*† Maximum 48-way Associative ECC-Protected L3 Cache**
    * 6-Mbyte L3 cache available in Rev C and later processors

    † 6 MB total includes space used by HT Assist (when enabled; applicable to C32, G34 and Fr6 (1207) package processors)
    - Shared cache architecture storage in addition to exclusive L1 and L2 caches
- **Floating-Point Unit**
  - AMD Wide Floating-Point Accelerator
    - 128-bit Floating-Point Unit (FPU)
- **Managemement and Virtualization Features**
  - Advanced Platform Management Link (APML)*
    * Supported by C32 and G34 package processors and Fr6 (1207) package processors in the Fr6 (1207) socket infrastructure

  - SMBus v2.0-compatible interface
  - Remote-Management Interface (SB-RMI)
- AMD Virtualization™ technology (AMD-V™)
  - Secure Virtualization Machine (SVM) disable and lock
  - Nested paging*
    * Performance improvements in Rev C and later processors
  - Rapid Virtualization Indexing
  - Improved world-switch speed in Rev C and later processors
  - SVM Pause count capability
- **Power Management**
  - Multiple low-power states
  - AMD Smart Fetch Technology (supported by Rev C and later processors)
  - Independent Dynamic Core Technology
  - AMD CoolCore™ Technology
  - Dual Dynamic Power Management
  - System Management Mode (SMM)
  - ACPI-compliant, including support for processor performance states
  - Supported power states: C0, C1, C1E*, S0, S1, S3, S4, S5
    * C1E supported by C32, G34, AM2r2, and AM3 package processors
- **Electrical Interfaces**
  - DDR2 SDRAM: SSTL_1.8 per JEDEC specification
  - DDR3 SDRAM: Compliant to JEDEC DDR3 1.5-V and LV-DDR3 1.35V* SDRAM specification
    * 1.35V LV-DDR3 on C32 and G34 package processors only
  - Refer to the *AMD Family 10h Processor Electrical Data Sheet*, order# 40014, for electrical details of AMD Family 10h processors.
- **HyperTransport™ Technology Interfaces**
  - HyperTransport 1 and HyperTransport 3* technology supported on each link
    * HyperTransport 3 technology support varies by package and socket infrastructure.
  - Maximum four (4) links on G34 package and three (3) links on other packages, each 16 bits in each direction
    - Each link supports up to 2000 MT/s (4.0 GB/s) in each direction in HyperTransport Generation 1.0 mode and up to 6400 MT/s (12.8 GB/s)† in each direction in HyperTransport Generation 3.0* mode.
      * Generation 3.0 mode is supported on connections to I/O devices by C32, G34, AM2r2, and AM3 package processors, and by Fr5 (1207) and Fr6 (1207) package processors when used in the socket Fr6 (1207) socket infrastructure. Generation 3.0 mode is also supported on connections to other DP or MP processors by C32 and G34 package processors and by Fr5 (1207) and Fr6 (1207) package processors when used in the socket Fr5 (1207) or socket Fr6 (1207) socket infrastructures. See *AMD Infrastructure Roadmap*, order# 41842.

      †C32 and G34 packages support up to 6400 MT/s (12.8 GB/s), Fr6 (1207) supports up to 4800 MT/s (9.6 GB/s) and other packages support up to 4400 MT/s (8.8 GB/s).
    - Each link on uniprocessor (UP) models supports connections to I/O devices.
    - Each link on dual-processor (DP) models supports connections to I/O devices, and any one of the three available links may connect to another DP or MP processor.
    - Each link on multi-processor (MP) models supports connections to I/O devices or other DP or MP processors.
  - HT Assist Technology (supported by C32, G34 and Fr6 (1207) package processors)
    - Increases HT bandwidth for multi-socket systems
- **Integrated Memory Controller**
  - AMD Memory Optimizer Technology

- Low-latency, high-bandwidth
- Prefetching Support
  - Improved Prefetching with Coherency Support (supported by Rev C and later processors)
  - Adaptive Prefetching (supported by Rev C and later processors)
- ECC checking with double-bit detect and single-bit correct
- Package AM2r2
  - 144-bit DDR2 SDRAM controller operating at frequencies up to 800 MT/s (400 MHz)
  - Supports up to four (4) unbuffered DIMMs
- Package AM3
  - 144-bit DDR3 SDRAM controller operating at frequencies up to 1333 MT/s (667 MHz)
  - Supports up to four (4) unbuffered DIMMs
- Packages Fr2 (1207), Fr5 (1207), and Fr6 (1207)
  - 144-bit DDR2 SDRAM controller operating at frequencies up to 800 MT/s (400 MHz)
  - Supports up to eight (8) registered DIMMs
  - On-line spare feature provides single-rank DRAM redundancy
- Package C32
  - 144-bit DDR3 SDRAM controller operating at frequencies up to 1333 MT/s (667 MHz)
  - Supports up to six (6) registered DIMMs
  - Supports up to four (4) unbuffered DIMMs
  - On-line spare feature provides single-rank DRAM redundancy
- Package G34
  - 144-bit DDR3 SDRAM controller operating at frequencies up to 1333 MT/s (667 MHz)
  - Supports up to twelve (12) registered DIMMs
  - Supports up to eight (8) unbuffered DIMMs
  - On-line spare feature provides single-rank DRAM redundancy

- **Available Packages**
  - Compliant with RoHS (EU Directive 2002/95/EC) with lead used only in small amounts in specifically exempted applications
  - Package AM2r2
    - Refer to the *AM2r2 Processor Functional Data Sheet*, order# 41697, for functional and mechanical details of the AM2r2 package processor.
    - 940-pin lidded micro PGA package
    - 1.27-mm pin pitch
    - 31-row x 31-col pin array
    - Organic C4 die attach
  - Package AM3
    - Refer to the *AM3 Processor Functional Data Sheet*, order# 40778, for functional and mechanical details of the AM3 socket.
    - 938-pin lidded micro PGA package
    - 1.27-mm pin pitch
    - 31-row x 31-col pin array
    - Organic C4 die attach
  - Package Fr2 (1207)
    - Refer to the *Fr2 (1207) Processor Functional Data Sheet*, order# 41698, for functional and mechanical details of the Fr2 (1207) package processor.
    - 1207-land lidded LGA package
    - 1.10-mm land pitch
    - 35-row x 35-col land array
    - Organic C4 die attach

- Package Fr5 (1207)
  - Refer to the *Fr5 (1207) Processor Functional Data Sheet*, order# 45602, for functional and mechanical details of the Fr5 (1207) package processor.
  - 1207-land lidded LGA package
  - 1.10-mm land pitch
  - 35-row x 35-col land array
  - Organic C4 die attach
- Package Fr6 (1207)
  - Refer to the *Fr6 (1207) Processor Functional Data Sheet*, order# 45603, for functional and mechanical details of the Fr6 (1207) package processor.
  - 1207-land lidded LGA package
  - 1.10-mm land pitch
  - 35-row x 35-col land array
  - Organic C4 die attach
- Package C32
  - Refer to the *C32 Processor Functional Data Sheet*, order# 47390, for functional and mechanical details of the C32 package processor.
  - 1207-land lidded LGA package
  - 1.10-mm land pitch
  - 35-row x 35-col land array
  - Organic C4 die attach
- Package G34
  - Refer to the *G34 Processor Functional Data Sheet*, order# 45937, for functional and mechanical details of the G34 package processor.
  - 1944-land lidded LGA package
  - 1.00-mm land pitch
  - 57-row x 40-col land array
  - Organic C4 die attach

2 Compatible Socket Infrastructures

Refer to the *AMD Infrastructure Roadmap*, order# 41842 for information on platform-feature implications of package and socket-infrastructure combinations. Family 10h AMD Opteron™ processors support the following socket infrastructures:

- **Socket AM2 Socket Infrastructure**
  - Compatible with AM2 and AM2r2 package processors
  - Refer to the *Socket AM2 Processor Functional Data Sheet*, order# 31117, for functional and mechanical details of the AM2 socket**.**
- **Socket AM2r2 Socket Infrastructure**
  - Compatible with AM2, AM2r2, and AM3 package processors
  - Refer to the *AM2r2 Processor Functional Data Sheet*, order# 41697, for functional and mechanical details of the AM2r2 socket**.**
- **Socket AM3 Socket Infrastructure**
  - Compatible with AM3 package processors
  - Refer to the *AM3 Processor Functional Data Sheet*, order# 40778, for functional and mechanical details of the AM3 socket.
- **Socket F (1207) Socket Infrastructure**
  - Compatible with F (1207), Fr2 (1207), and Fr5 (1207) package processors
  - Refer to the *Socket F (1207) Processor Functional Data Sheet*, order# 31118, for functional and mechanical details of the F (1207) socket**.**
- **Socket Fr2 (1207) Socket Infrastructure**
  - Compatible with F (1207), Fr2 (1207), Fr5 (1207), and Fr6 (1207) package processors
  - Refer to the *Fr2 (1207) Processor Functional Data Sheet*, order# 41698, for functional and mechanical details of the Fr2 (1207) socket**.**
- **Socket Fr5 (1207) Socket Infrastructure**
  - Compatible with F (1207), Fr2 (1207), Fr5 (1207), and Fr6 (1207) package processors
  - Refer to the *Fr5 (1207) Processor Functional Data Sheet*, order# 45602, for functional and mechanical details of the Fr5 (1207) socket.
- **Socket Fr6 (1207) Socket Infrastructure**
  - Compatible with Fr5 (1207) and Fr6 (1207) package processors
  - Refer to the *Fr6 (1207) Processor Functional Data Sheet*, order# 45603, for functional and mechanical details of the Fr6 (1207) socket.
- **Socket C32 Socket Infrastructure**
  - Compatible with C32 package processors
  - Refer to the *C32 Processor Functional Data Sheet*, order# 47390, for functional and mechanical details of the C32 socket.
- **Socket G34 Socket Infrastructure**
  - Compatible with G34 package processors
  - Refer to the *G34 Processor Functional Data Sheet*, order# 45937, for functional and mechanical details of the G34 socket.