AMD 890FX Product Errata

Silicon Errata for AMD 890FX (RD890)

Publication # **46377**	Revision: **3.0**
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Trademarks

Revision History

Date	Revision	Description
February 2012	3.0	• Initial release based on OEM version 1.2

Product Errata Summary

A unique errata reference number (ERN) has been assigned to each erratum within this document for user convenience in tracking the errata within specific revision levels. Table 1 cross-references the revisions of the part to each erratum. An "X" indicates that the erratum applies to the revision. The absence of an "X" indicates that the erratum does not apply to the revision. An "*" indicates advance information that the erratum has been fixed but not yet verified. "No fix planned" indicates that no fix is planned for current or future revisions of the ASIC.

Note: *There may be missing errata numbers. Errata that have been resolved from early revisions of the ASIC have been deleted.*

Table 1: Cross-Reference of Product Revision to Errata

#	Errata Description	ASIC Revision
		A21
1	IOMMU L1 Interrupt Identification	No fix planned
2	Non-optimal HTIU Splitting of Host Requests	No fix planned
4	HyperTransport™ Compat Bit Set in Upstream Isoc DMA	No fix planned
6	Downstream Stomped HyperTransport™ Responses	No fix planned
9	Glitch on the HyperTransport™ Interface When Using LS1 Combined with the PHY_OFF Inactive Lane State when Increasing the HyperTransport Link Width	No fix planned
10	IOMMU Event Log Consistency	No fix planned
12	Attributes for "Special" Upstream TgtDone Responses may be Incorrect	No fix planned
49	LDTSTOP# Assertion During HyperTransport™ Link Training May Lead to an Incorrect Link State Transition	No fix planned
56	HyperTransport™ Clock Data Recovery (CDR) Disabled Too Late When Changing Link Width Using LDTSTOP	No fix planned
58	IOMMU May Pass Reads in the HyperTransport™ System Management Address Range	No fix planned
60	Zero-Byte DMA Reads are Sent to Physical Address 0x0	No fix planned
61	IOMMU Aborts ATS Address Translation Requests to the Exclusion Range when DTE.TV=0	No fix planned
62	HyperTransport™ BIST ErrLnNum Priority is Incorrect	No fix planned
63	IOMMU Blocks Writes in the HyperTransport™ System Management Address Range when SysMgt=0x1	No fix planned
64	Certain IOMMU Registers Not Initialized/Cleared Properly	No fix planned
67	Replay Timer Timeout Status Set Incorrectly	No fix planned
71	Loss of Flow Control During LDTSTOP# When Using HyperTransport™ Gen1 Mode	No fix planned
74	Incorrectly Addressed HD Audio Requests from the Southbridge Issued Using the VC1 Channel Are Not Aborted	No fix planned
76	Read Completion Timeout with Relaxed Ordering	No fix planned
77	Read Completion Timeout	No fix planned
79	IOMMU Event Log Ordering Violation	No fix planned

Product Errata

1 IOMMU L1 Interrupt Identification

Description

IOMMU L1 identifies all requests <= 1DW in size in the interrupt ranges (HyperTransport™ or MSI) as interrupts when real interrupts should only be 1DW in size.

Potential Effect on System

Malformed interrupt requests (not all byte enables set) may be treated by IOMMU as normal interrupts.

Suggested Workaround

None, as these types of requests are not expected during normal operation.

Fix Planned

No

2 Non-optimal HTIU Splitting of Host Requests

Description

HTIU will split host requests that are not naturally aligned but may do so in a non-optimal way.

Potential Effect on System

Lower performance for requests that are not naturally aligned.

Suggested Workaround

None

Fix Planned

No

4 HyperTransport™ Compat Bit Set in Upstream Isoc DMA

Description

The chipset sets the compat bit whenever it sets the Isoc bit for upstream DMA.

Potential Effect on System

None. The processor ignores the compat attribute in upstream DMA requests.

Suggested Workaround

None

Fix Planned

No

6 Downstream Stomped HyperTransport™ Responses

Description

Downstream stomped read responses on the HyperTransport interface may result in data corruption.

Potential Effect on System

None, as it has been confirmed that the processor will not send this type of request.

Suggested Workaround

None

Fix Planned

No

9 Glitch on the HyperTransport Interface When Using LS1 Combined with the PHY_OFF Inactive Lane State when Increasing the HyperTransport Link Width

Description

Under this condition (PHY_OFF inactive lane state and LS1), the HyperTransport transmitter is reset to realign the active and inactive lanes when doing an HyperTransport link width increase. However, given that the clock lanes are also reset, a glitch is observed on the clock.

Potential Effect on System

Cannot support this particular configuration (PHY_OFF inactive lane state and LS1).

Suggested Workaround

Either set the inactive lane state to “operational” while continuing to support LS1 or configure HyperTransport to use LS2 while continuing to support the PHY_OFF inactive lane state.

Fix Planned

No

10 IOMMU Event Log Consistency

Description

When the IOMMU detects specific combinations of errors within the same transaction, the resulting IOMMU event log entry may contain event information in reserved bits that should have only been set for another event log type. These reserved bits should be ignored by software. The Device ID, Address fields, and defined status bits are correct.

Potential Effect on System

IOMMU event logs may be generated that do not strictly correspond to any of the formats defined in the IOMMU specification.

Suggested Workaround

None

Fix Planned

No

12 Attributes for "Special" Upstream TgtDone Responses May Be Incorrect

Description

When HTIU converts a non-posted host write to a posted one, it internally creates a TgtDone response. This response may have PassPW attributes set incorrectly.

Potential Effect on System

None expected. TgtDone responses that may have the incorrectly set PassPW attributes have no ordering requirements relative to other packets.

Suggested Workaround

None

Fix Planned

No

49 LDTSTOP# Assertion During HyperTransport™ Link Training May Lead to an Incorrect Link State Transition

Description

If LDTSTOP# is asserted while the Northbridge HyperTransport receiver is in training 2 state and the HyperTransport transmitter is in training 3 state, the transmitter does not proceed to operational or send 200 ns of disconnect NOPs before shutting off the link. Instead, the transmitter sends training patterns for 200 ns before shutting off the link.

Potential Effect on System

None expected.

Suggested Workaround

None required.

Fix Planned

No

56 HyperTransport™ Clock Data Recovery (CDR) Disabled Too Late When Changing Link Width Using LDTSTOP#

Description

When decreasing HyperTransport link width using LDTSTOP#, the PHY receiver CDR is disabled too late. The CDR may pick up garbage samples and drift slightly off the nominal position.

Potential Effect on System

HyperTransport training may take slightly longer when doing a width increase using LDTSTOP#.

Suggested Workaround

None, as HyperTransport width changes are not made during normal system operation.

Fix Planned

No

58 IOMMU May Pass Reads in the HyperTransport™ System Management Address Range

Description

Under a highly specific sequence of requests and internal timing conditions, the IOMMU may pass through read requests in the HyperTransport system management address range when the associated device table entry has the SysMgt field set to 01b (pass through writes). These are erroneous requests since devices should not be allowed to issue reads to this address range when SysMgt=01b.

Potential Effect on System

Unpredictable system behavior. This issue has only been observed in the simulation environment.

Suggested Workaround

Only set DTE.SysMgt=01b for the Southbridge ACPI controller. The Southbridge is the only device that should be generating requests in the HyperTransport interrupt address range and it is not expected to propagate read requests in this range.

Fix Planned

No

60 Zero-Byte DMA Reads are Sent to Physical Address 0x0

Description

All zero-byte DMA reads are sent to physical address 0x0.

Potential Effect on System

None

Suggested Workaround

None

Fix Planned

No

61 IOMMU Aborts ATS Address Translation Requests to the Exclusion Range when DTE.TV=0

Description

IOMMU master aborts ATS address translation requests to the exclusion range when the associated device table entry has DTE.TV=0 and either DTE.EX=1 or the EX_ALLOW register is set to 1. Having DTE.TV=0 implies that the device does not have any page tables and is only issuing DMA requests into the exclusion range.

Potential Effect on System

Endpoint devices are prevented from issuing translated requests to the exclusion range under the described device table entry configuration.

Suggested Workaround

Set DTE.TV=0, set DTE.TV=1, DTE.IR=0 and DTE.IW=0.

Fix Planned

No

62 HyperTransport™ BIST ErrLnNum Priority is Incorrect

Description

The HyperTransport specification defines the BIST ErrLnNum register to record the highest numbered lane with an error but the device reports the lowest numbered lane with an error.

Potential Effect on System

None, however, this is an HyperTransport specification violation.

Suggested Workaround

None

Fix Planned

No

63 IOMMU Blocks Writes in the HyperTransport™ System Management Address Range when SysMgt=0x1

Description

Write requests to the HyperTransport system management address range may be blocked by the IOMMU when the associated device table entry has the SysMgt field set to 01b (pass through writes) with V=1, TV=1 and IW=0.

Potential Effect on System

Unpredictable system behavior. This issue has only been observed in the simulation environment.

Suggested Workaround

Only set DTE.IW=1 for the south bridge ACPI controller as this is the only device in the system that should issue system management requests.

Fix Planned

No

64 Certain IOMMU Registers Not Initialized or Cleared Properly

Description

The IOMMU command buffer and event log tail and head pointers are only reset on a cold boot rather than warm boot and are not reset when the command buffer base register or event log base register are written as per the IOMMU specification.

Potential Effect on System

The IOMMU command buffer tail pointer and event log head pointer are not set to zero when exiting a warm reset or after the associated base address registers are written. This may lead to commands being fetched or events being indicated once either of these features are enabled. Additionally, reading the IOMMU command buffer head pointer or event log tail pointer registers after a reset but before the pointers are explicitly written and before the associated base address registers are written may return an unpredictable value.

Suggested Workaround

The System BIOS should explicitly clear the IOMMU pointer registers on every reset. IOMMU software should explicitly clear the IOMMU pointer registers after writing the command buffer and event log base address registers before enabling the associated feature.

Fix Planned

No

67 Replay Timer Timeout Status Set Incorrectly

Description

If a device sends repeated NAKs on the PCIe® link to the chipset resulting in a REPLAY_NUM rollover event, the Replay Timer Timeout Status register bit is set incorrectly. The REPLAY_NUM Rollover Status register is set as expected.

Potential Effect on System

Error diagnostic software may misdiagnose the cause of a REPLAY_NUM rollover event on the PCIe link. Software may interpret that the REPLAY_NUM rollover event was caused by the absence of ACKs or NAKs when NAKs were received.

Suggested Workaround

None

Fix Planned

No

71 Loss of Flow Control During LDTSTOP# When Using HyperTransport™ Gen1 Mode

Description

Under highly detailed and specific internal timing conditions, the chipset may fail to properly release posted flow-control credits to the processor during a HyperTransport Gen1 disconnect sequence due to an LDTSTOP# assertion. The conditions for this errata can not occur if LDTSTOP# is asserted to enter a processor C-state.

Potential Effect on System

Progressive loss of posted flow control buffers on the HyperTransport link from the processor to the chipset will eventually result in a system hang.

Suggested Workaround

Operate the link between the chipset and the processor in HyperTransport Gen3 mode if LDTSTOP# needs to be asserted for reasons other than processor C-states.

Fix Planned

No

74 Incorrectly Addressed HD Audio Requests from the Southbridge Issued Using the VC1 Channel Are Not Aborted

Description

DMA read requests from the Southbridge HD audio controller with invalid addresses may not be aborted if all of the following conditions are true:

- IOMMU is disabled
- The DMA read is to an address greater than the maximum supported physical address size (52 bits).
- The DMA read is issued over the VC1 channel instead of VC0.

Potential Effect on System

Unpredictable system behavior.

Suggested Workaround

Do not program the Southbridge HD audio controller to issue requests using more than 52-bit addressing. Such a request is invalid and would normally result in a master abort.

Fix Planned

No

76 Read Completion Timeout with Relaxed Ordering

Description

A starvation condition is created when a Relaxed Ordering enabled read from an endpoint device does not make forward progress in the presence of a persistent stream of upstream writes from a device behind the same PCIe® root port.

Potential Effect on System

When this starvation condition lasts longer than the PCIe read completion timeout in the reading device(s), an AER error is reported. This is expected to be a rare event given the common conditions, such as bursts of DMA write traffic from other ports or bursts of A-Link traffic, that will break the starvation. The timeout has not been observed with production software as persistent writes are not common in real-world applications.

Suggested Workaround

Disable Relaxed Ordering by setting NBMiscCfg space IOC_PCIE_DXX_CNTL [2:0] = 0x6 (where XX are the device numbers for PCIe bridge devices 2 through 13) as well as IOC_PCIE_CNTL which is the register for bridge 8 (the Southbridge A-Link bridge). This change is implemented in CIMx version 1.0.1.2.

Fix Planned

No

77 Read Completion Timeout

Description

A DMA read from a PCIe® endpoint device may not make forward progress in the presence of a persistent stream of upstream writes from a device behind the same PCIe root port. Forward progress is prevented if the DMA read is incorrectly blocked by the chipset due to it being followed in the internal pipeline by a second DMA read or write from a different PCIe root port. Once the incorrect blockage occurs, the following conditions can release the blocked read request and allow forward progress:

- One or more DMA reads from the same PCIe root port that issued the blocked read request.
- A burst of DMA writes from a PCIe root port other than the one that issued the blocked read request.

Potential Effect on System

When a DMA read is blocked longer than its PCIe read completion timeout value, an AER error is reported.

Suggested Workaround

Drivers for devices that can issue long streams of DMA writes are advised to modify their DMA access patterns to periodically insert DMA reads. The reads do not need to complete before additional writes are issued. Reads need to be inserted at a sufficient rate to ensure that, if the incorrect blockage occurs, this condition will be broken well within the lowest PCIe completion timeout value in the system.

Fix Planned

No

79 IOMMU Event Log Ordering Violation

Description

The chipset does not maintain producer-consumer ordering between the IOMMU event log DMA writes and IOMMU MMIO register read completions. The CPU may read stale or uninitialized event logs from memory when a read response from the event log tail pointer register passes the corresponding event log DMA write. A series or burst of event log DMA writes are normally required for this issue to occur.

Potential Effect on System

Software may process an event log before it has been completely written, possibly resulting in the operating system or Hypervisor taking improper corrective actions.

Suggested Workaround

The IOMMU driver of the Hypervisor or operating system should initialize the event log buffer to all zeros and write event log entries to zero after they are processed. If software subsequently observes an all zero event log entry, it should re-read the buffer until a non-zero event log is returned.

Fix Planned

No