AMD 780 Product Errata

Silicon Errata for AMD 780G, 780V, 760G, 790GX, 780E, M780G, M780V and M770

Publication #	**48319** Revision: **1.0**
Issue Date:	**April 2010**

Revision History

Date	Revision	Description
April 2010	1.0	• Initial public release based on OEM version ER_RS780B7

Product Errata Summary

Except where otherwise noted, this product errata is applicable to AMD 780 family of Northbridge devices including the AMD 780G, 780V, 760G, 790GX, 780E, M780G, M780V and M770.

Table 1 cross-references the revisions of the part to each erratum. An "X" indicates that the erratum applies to the revision. The absence of an "X" indicates that the erratum does not apply to the revision. An "*" indicates advance information that the erratum has been fixed but not yet verified. "No fix planned" indicates that no fix is planned for current or future revisions of the ASIC.

Note: *There may be missing errata numbers. Errata that have been resolved from early revisions of the ASIC have been deleted.*

Table 1: Cross-Reference of Product Revision to Errata

#	Errata Description	ASIC Revision	
		A12	A13
3	HyperTransport™ Gen3 Instability at 1.2GHz	X	
17	Native PCIe Hot Plug and Native PME Wake-up Interrupt Delivery	X	
18	APC Bridge Subsystem Vendor ID Decode Conflict	No Fix Planned	
19	Software-initiated Interrupt Support	X	
20	External PCIe® Graphics Hang with L1 Enabled	X	
21	Memory Controller FIFO Overflow at Reduced Engine Speeds	X	
22	Dropped Host Read	X	

3 HyperTransport™ Gen3 Low Speed Instability

Description

HyperTransport™ Gen3 instability has been observed when running the HyperTransport link at speeds between 1.2 GHz and 1.6 GHz. This problem, which only affects some ASICs, has been identified as an issue with the receiver DLL in the HyperTransport PHY when running in this frequency range.

Potential Effect on System

For an ASIC that does exhibit this sensitivity, the system will show a high retry count on the HyperTransport link which may result in system failures, including system hangs (black screen), screen corruption, or a frozen screen.

Suggested Workaround

For all configurations, HyperTransport Gen3 speeds should be limited to running between 1.8 GHz and 2.2 GHz.

Fix Planned

Resolved in A13 silicon

17 Native PCIe Hot Plug and Native PME Wake-up Interrupt Delivery

Description

A logic issue has been identified in the Northbridge that prevents internally generated MSI (Message Signal Interrupts) and external PME (Power Management Event) messages from propagating to the CPU.

Potential Effect on System

This issue only affects PCIe native features in which control of PME and hot plug is turned over to the operating system instead of to the BIOS firmware. For example, Windows Vista® native mode PME and native mode hot plug features will be affected. Wake-up using PME is still supported via normal ACPI methods (non-native PCIe mode) which continues to be fully supported by the RS780 and SB700. ACPI-based hot plug, for example, for ExpressCards continues to be supported via normal ACPI methods (General Purpose Event triggered SCI and BIOS ASL code event handler).

Suggested Workaround

For Windows Vista, platforms should implement legacy hot plug and legacy PME features as per normal ACPI methods. From a hardware perspective, this includes the implementation of the sideband connections (CPPE# and WAKE#) from the ExpressCard interface to the south bridge GEVENT pins.

Fix Planned

Resolved in A13 silicon.

18 APC Bridge Subsystem Vendor ID Decode Conflict

Description

Overwriting the sub-system vendor ID (offset 0xB4) in the APC configuration space will result in the vendor ID (offset 0x0) being erroneously overwritten in the APC configuration space.

Potential Effect on System

If the register is overwritten, any utilities that references the APC configuration space will report back the updated vendor ID (OEM data instead of AMD data).

Suggested Workaround

Do not overwrite the SSID/SVID values in the APC configuration space. If required, OEM-specific SSID/SVID data should be programmed in the internal graphics PCI configuration space (bus1, dev5, func0).

Fix Planned

None

19 Software-Initiated Interrupt Support

Description

Software-initiated (display driver and Video BIOS) interrupts do not function on A12 silicon.

Potential Effect on System

Features that would typically employ the use of software-triggered interrupts cannot be implemented using software-triggered interrupts. These features include:

- Display switch requests (e.g., display hotkey switch support)
- Expansion mode change requests (e.g., center/expansion hotkey switch support)
- Forced power state change requests
- System power source change requests
- Display configuration change request (e.g., display mapping change due to docking/ undocking)

Suggested Workaround

A display driver polling scheme (which is enabled via a driver packaging option) is available as a workaround to this issue. Apart from the change to the driver packaging options, this workaround is transparent to the OEM/ODM implementation. All of the existing functionality that relies on the software interrupt will continue to function through the use of the polling method.

Fix Planned

Resolved in A13 silicon

20 External PCIe Graphics Hang with L1 Enabled

Description

When a PCIe® graphics endpoint device issues a PM_REQ (request entry to L1) and the root complex (i.e., Northbridge) issues a TLP (data packet) prior to issuing a PM_REQ (ack entry to L1), the endpoint will enter L1 without acknowledging the TLP. Under this condition, the Northbridge will issue replays and eventually hang because it has not received an ACK to its TLP.

Potential Effect on System

Although ATI/AMD PCIe graphics boards are not subject to this problem, non-AMD graphics boards have been observed to hang when L1 is enabled. Please note, however, that the non-AMD graphics boards that were tested did not support L1 and this issue was only observed after overriding the setting for the L1 capability in the configuration space of the add-in board. As such, there is no end-user impact as a result of this issue until which time non-AMD PCIe graphics card vendors may enable L1 support.

Suggested Workaround

Disable L1 for the PCIe graphics link in the SBIOS upon detecting A12 silicon in combination with a non-AMD/ATI PCIe graphics vendor ID**.**

Fix Planned

Resolved in A13 silicon

21 Memory Controller FIFO Overflow at Reduced Engine Speeds

Description

An issue has been identified that results in an overflow of an internal memory controller FIFO when a specific traffic pattern is exercised. This pattern consists of a non-write-combined transaction followed by a write-combined transaction. The problem is only exposed when write-combining is enabled in conjunction with the PowerShift engine clock frequency scaling feature.

Potential Effect on System

This issue may cause system hangs and/or general system instability on platforms supporting a sideport memory interface.

Suggested Workaround

Exposure to this failure is eliminated by adjusting the PowerPlay table in the VBIOS such that the minimum PowerShift engine frequency is set to 300 MHz.

Fix Planned

Resolved in A13 silicon

22 Dropped Host Read

Description

A host read may get dropped by the Northbridge if it was preceded by a non-posted host memory write under certain highly specific traffic and timing conditions. When the Northbridge IO controller's (IOC) host request buffer is full, an incoming non-posted host memory write will be internally completed and a response will be returned to the processor prior to the IOC actually executing and completing the write which is then queued in a buffer in front of the IOC. In this state, a subsequent host read request received from the processor will try to claim the buffer location that is filled with the pending non-posted write resulting in the read getting dropped. Any forward progress by the IOC's host request buffer during the time between the non-posted write and the read will bring the device out of the previously described state and allow for correct execution.

Potential Effect on System

This issue may cause system hangs and/or general system instability during system stress testing.

Suggested Workaround

A system BIOS workaround is used to set all transactions as non-posted and removes all Southbridge devices from the CPU MMIO map. This workaround was originally introduced in RS780 CIM-X version 2.0.2. It has been recently updated in CIM-X version 4.1.0 to account for compatibility issues involving a limited number of non-HD PCI audio hardware. Testing and qualification has confirmed that there is no performance impact as a result of this workaround.

Fix Planned

Resolved in A13 silicon