

Model Name:GA-78LMT-USB3

Version: 6.01

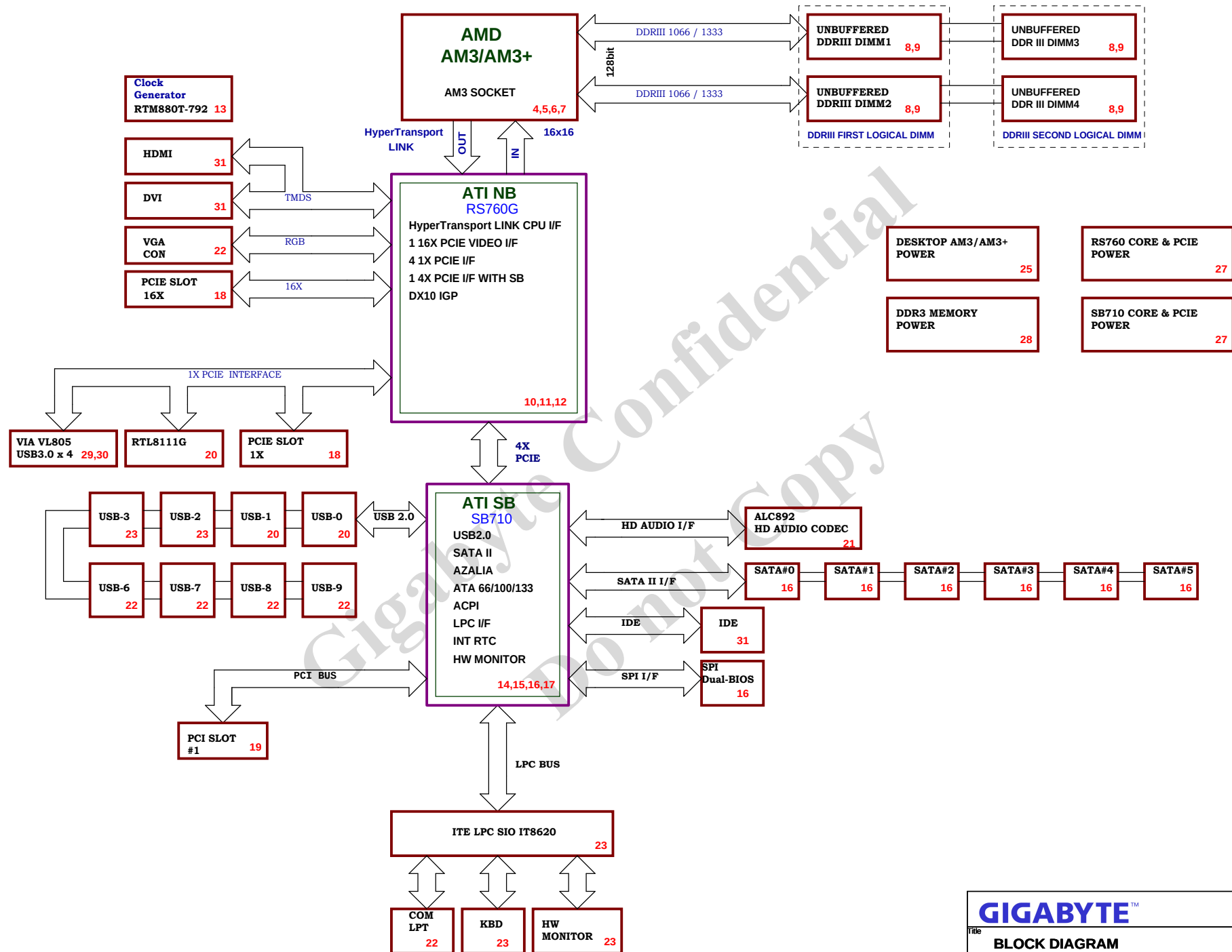
BOM : 9M78LTUB3-00
P-Code: U99098-0

Component value change history

[illegible]

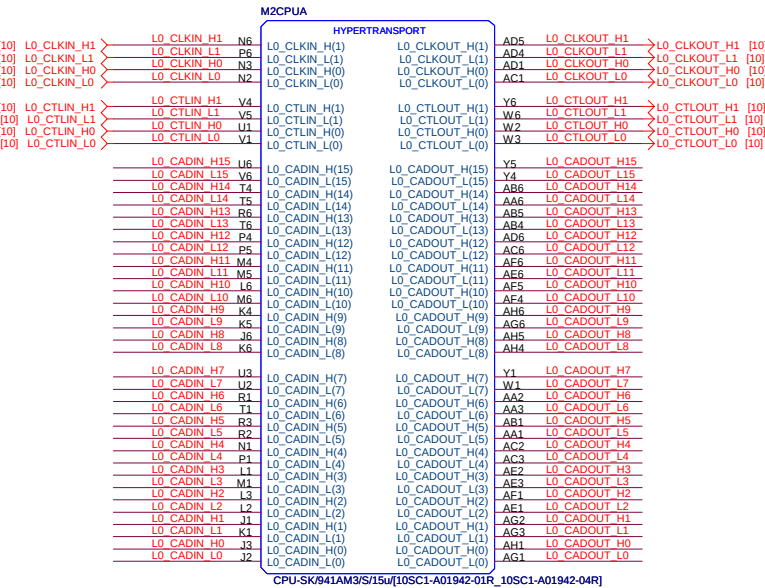
Circuit or PCB layout change for next version

[illegible]



L0_CADIN_L[0..15] <L0_CADIN_L[0..15] [10]
L0_CADIN_H[0..15] <L0_CADIN_H[0..15] [10]

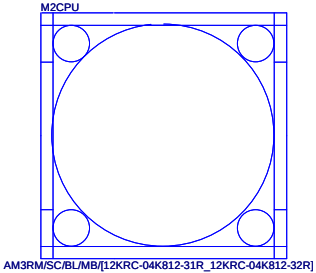
L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] [10]
L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] [10]

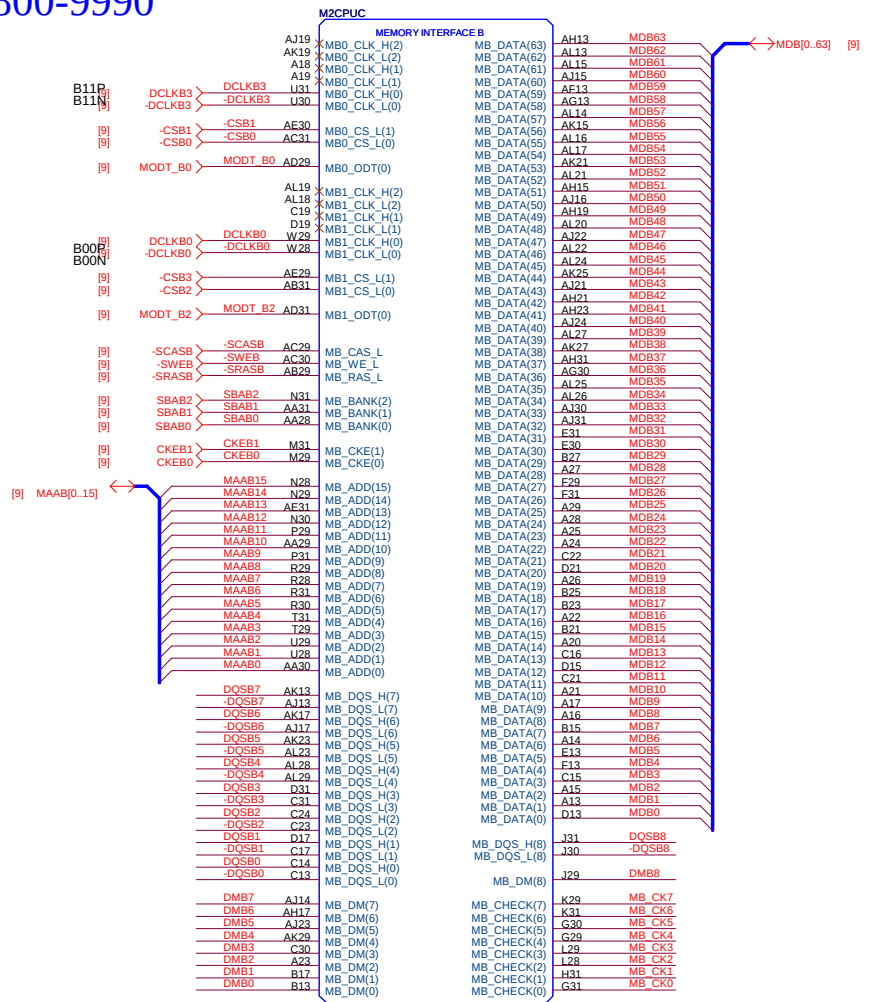
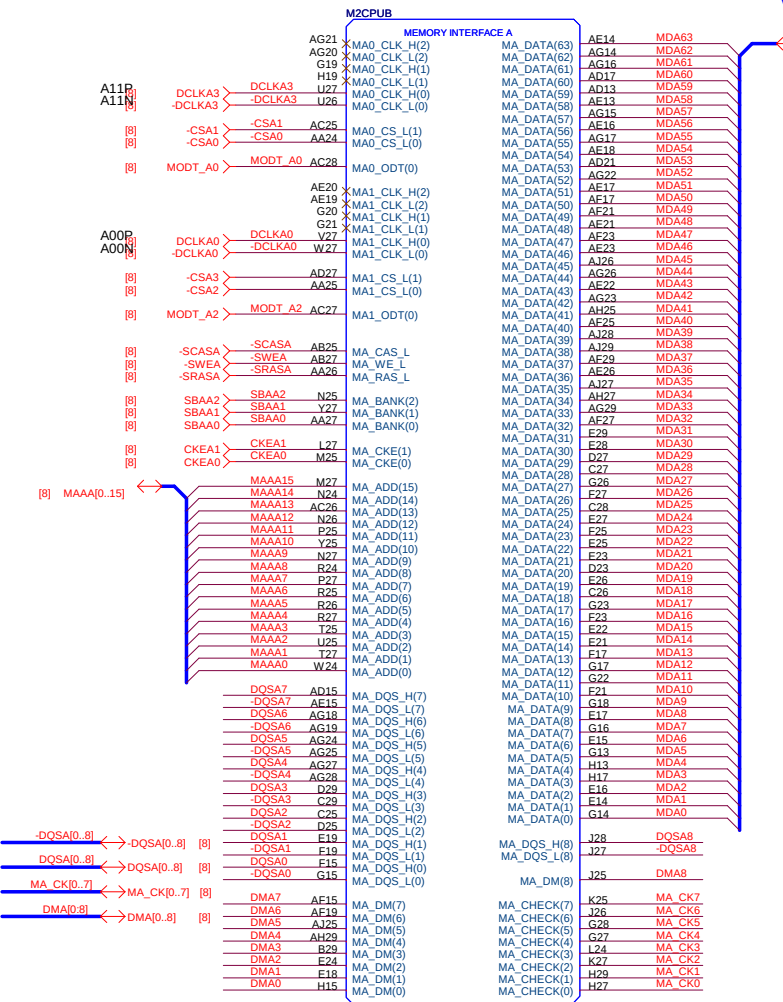


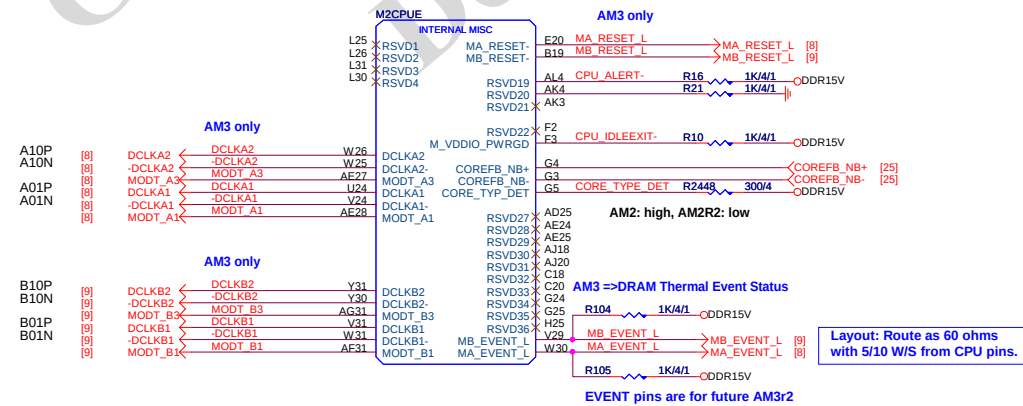
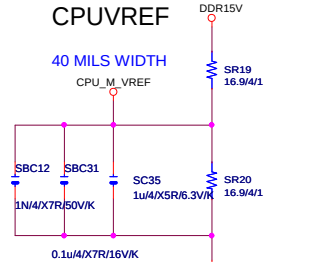
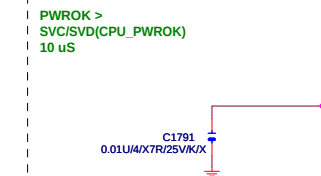
Gigabyte Confidential
Do not Copy

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

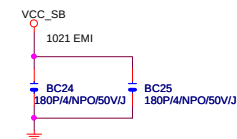
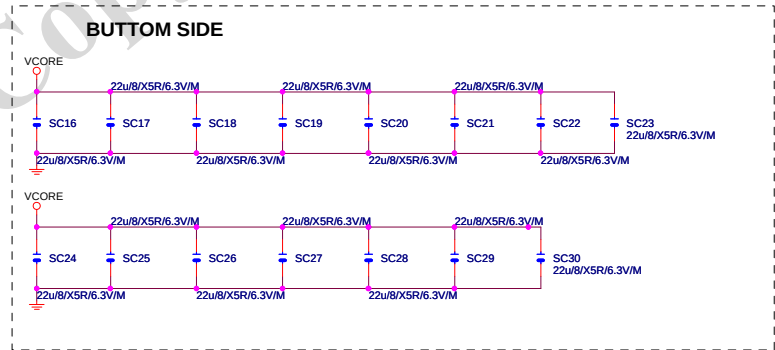
VLDT_A = VCC12_HT
VLDT_B = HT12B

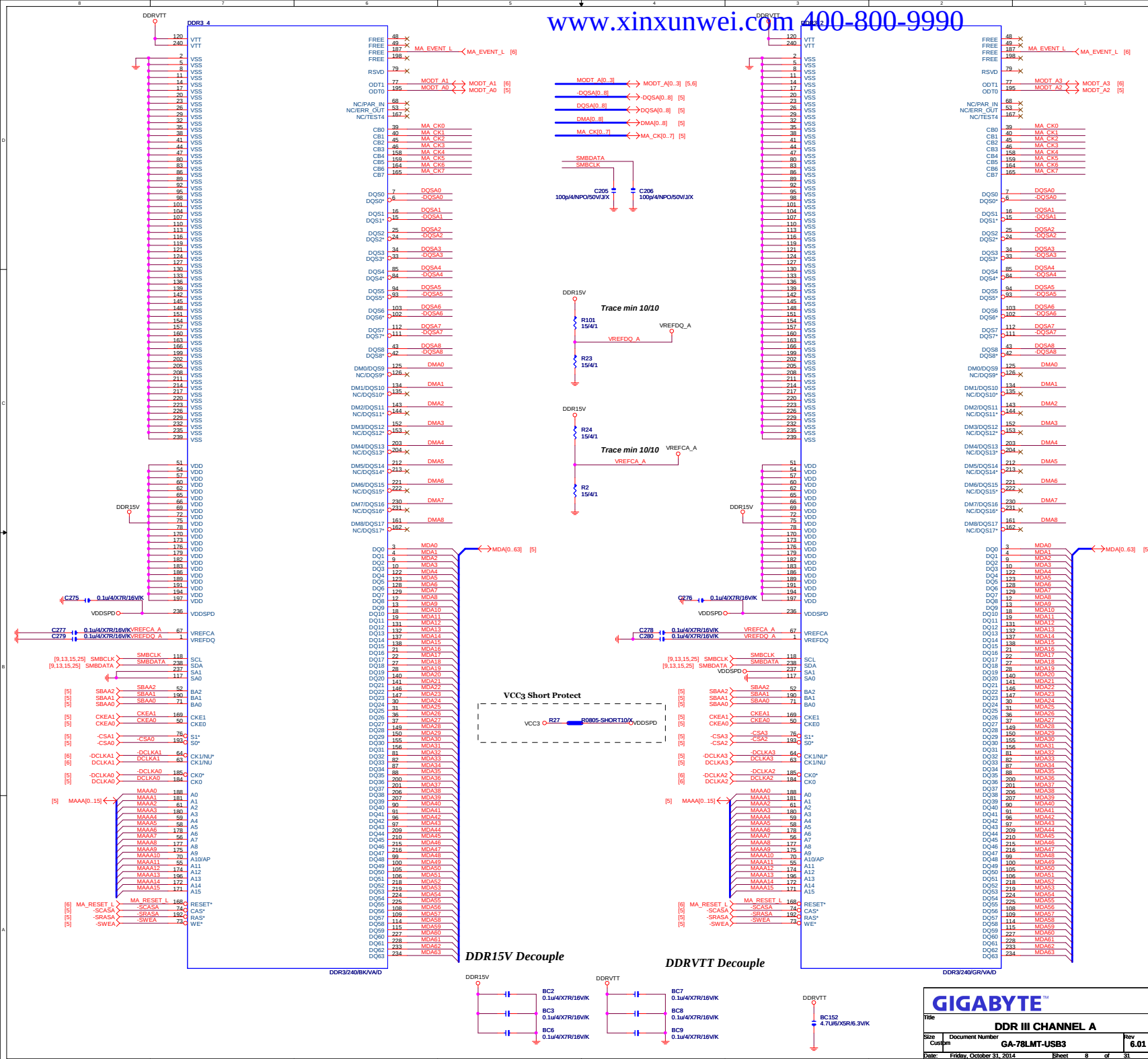


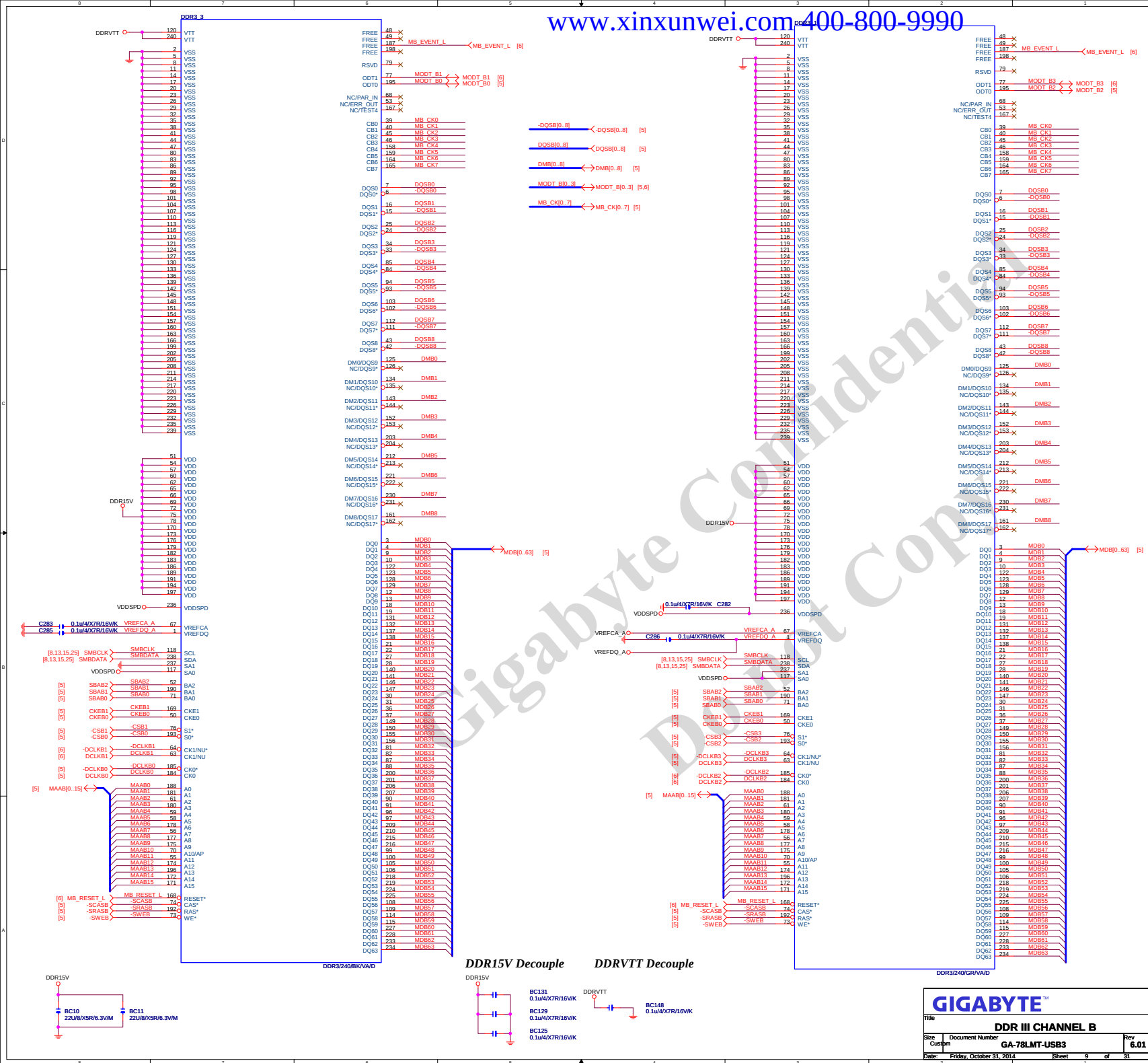


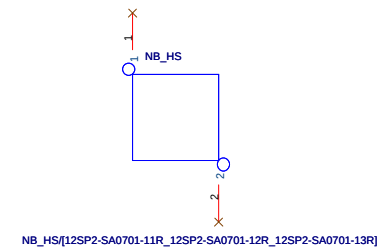
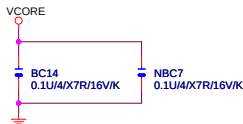
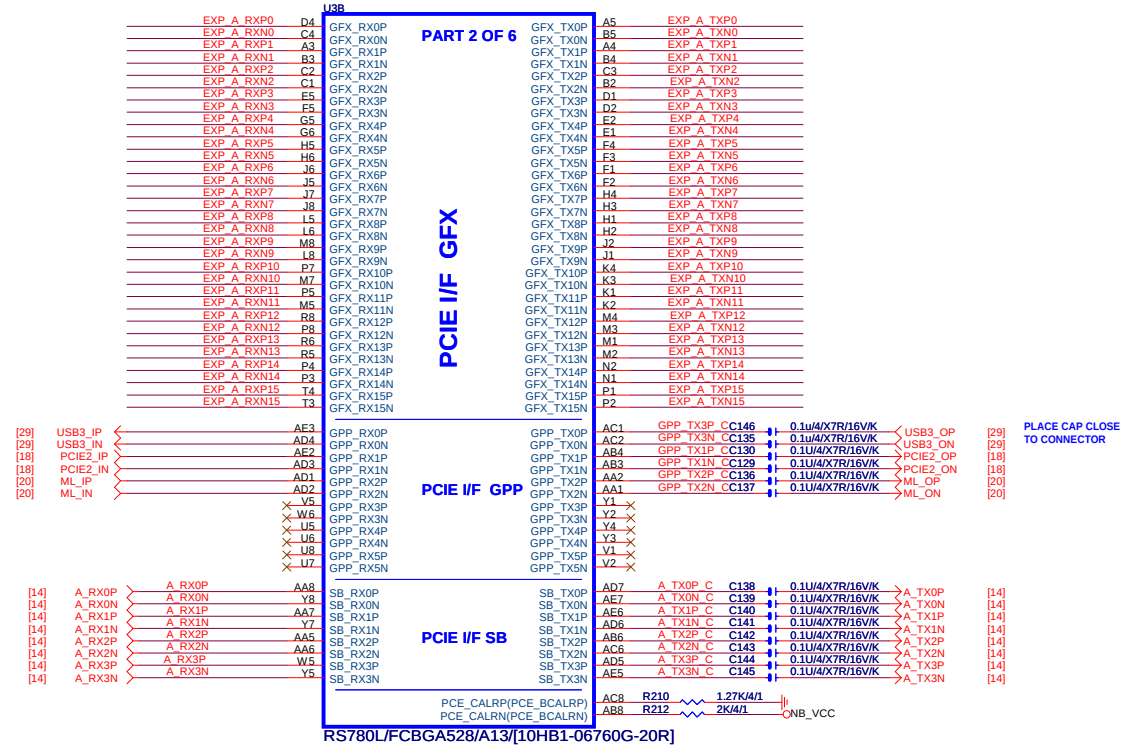


GIGABYTE™			
CPU CONTROL			
Size	Document Number		Rev
Custom	GA-78LMT-USB3		6.01
Date:	Friday, October 31, 2014	Sheet	6 of 31







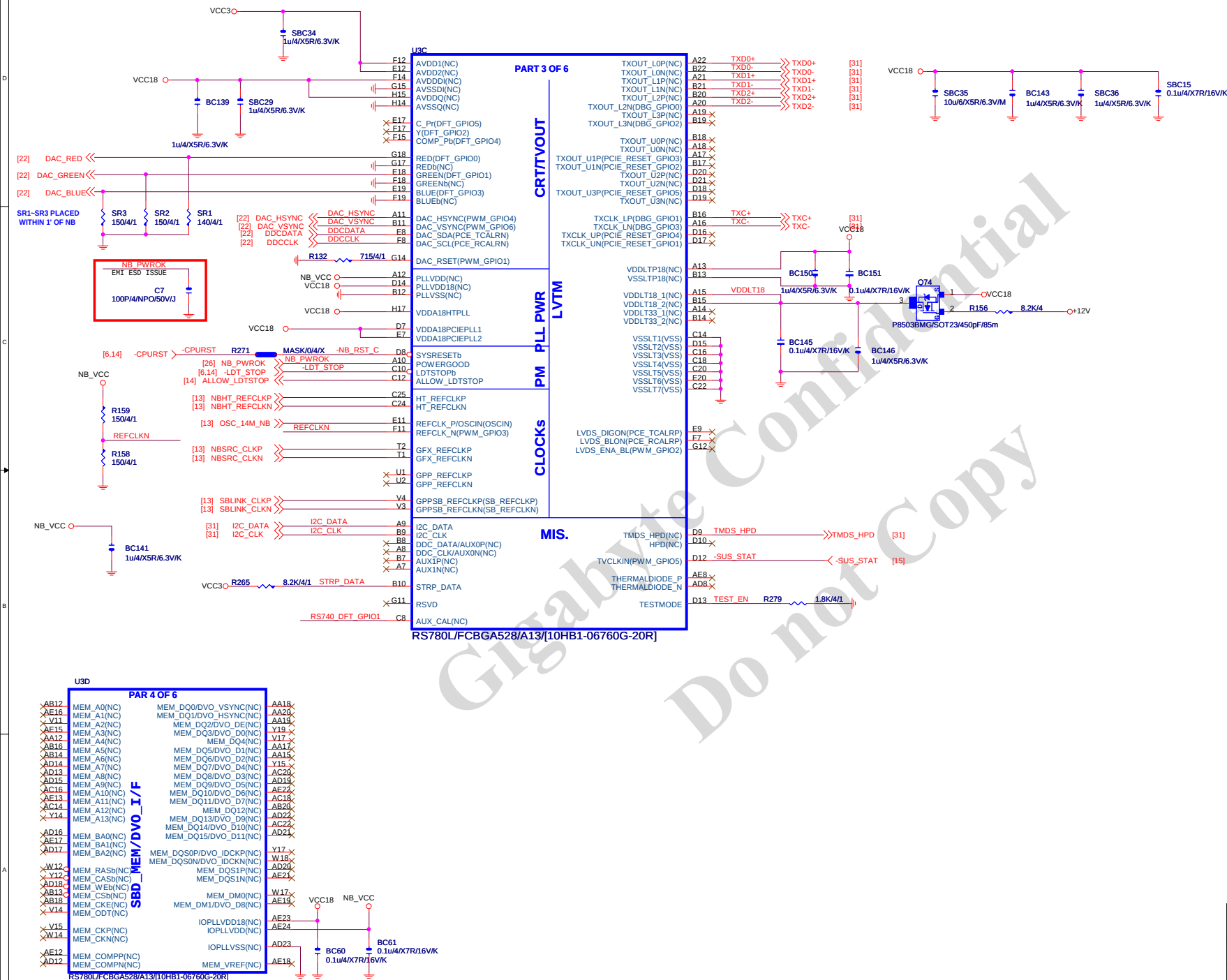


GIGABYTE™

Title		
RS780 HT-LINK I/F		
Size	Document Number	Rev
Custom	GA-78LMT-USB3	6.01
Date:	Friday, October 31, 2014	Sheet 10 of 31

Note: for RS780, change R232 to 150R as AUX_CAL,
place close to pin C8

Note: for RX780, R217 (RX780_DFT_GPIO1) to 3K accordingly



[22] DAC_VSYNC << R276 3K/4/1 VCC3

Note: for RX780, change following pull-down resistor to 3K accordingly
R912 (RX780_DFT_GPIO5)

Note: for RX780, change following pull-down resistor to 3K accordingly

[22] DAC_HSYNC << R285 3K/4/1 VCC3

Note: for RX780, change following pull-down resistor to 3K accordingly
R219 (RX780_DFT_GPIO0)

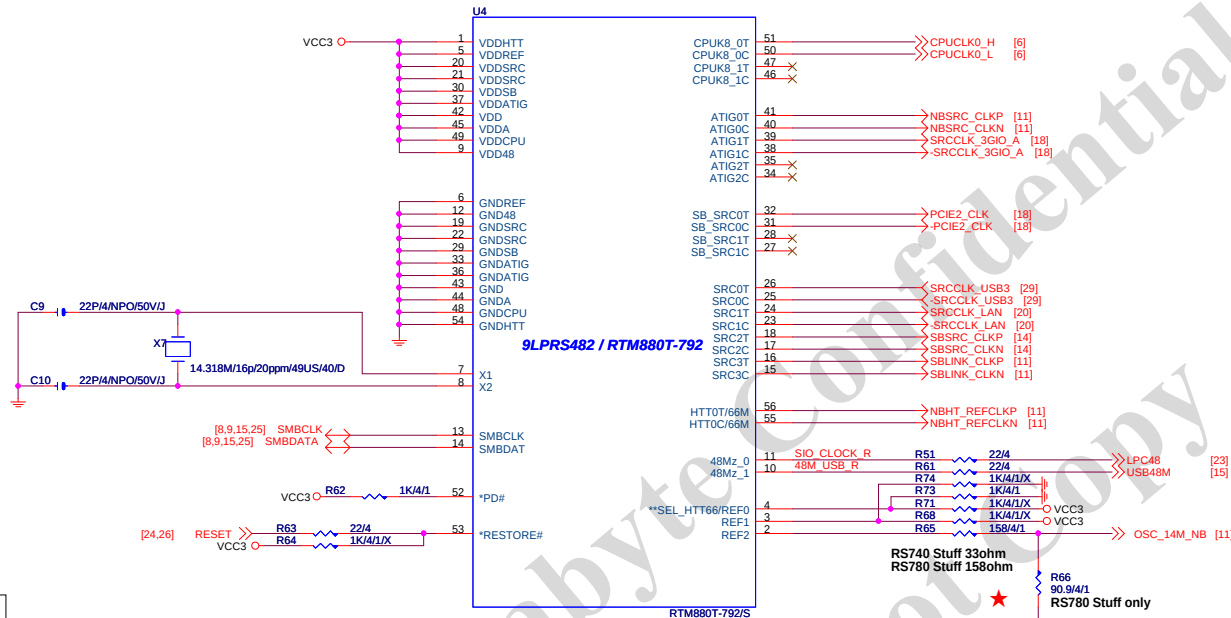
The intersection of the two lines is the solution to the system of equations.

	RS740	RX780	RS780
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* the GFX_REFCLK input is required for all cases



- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

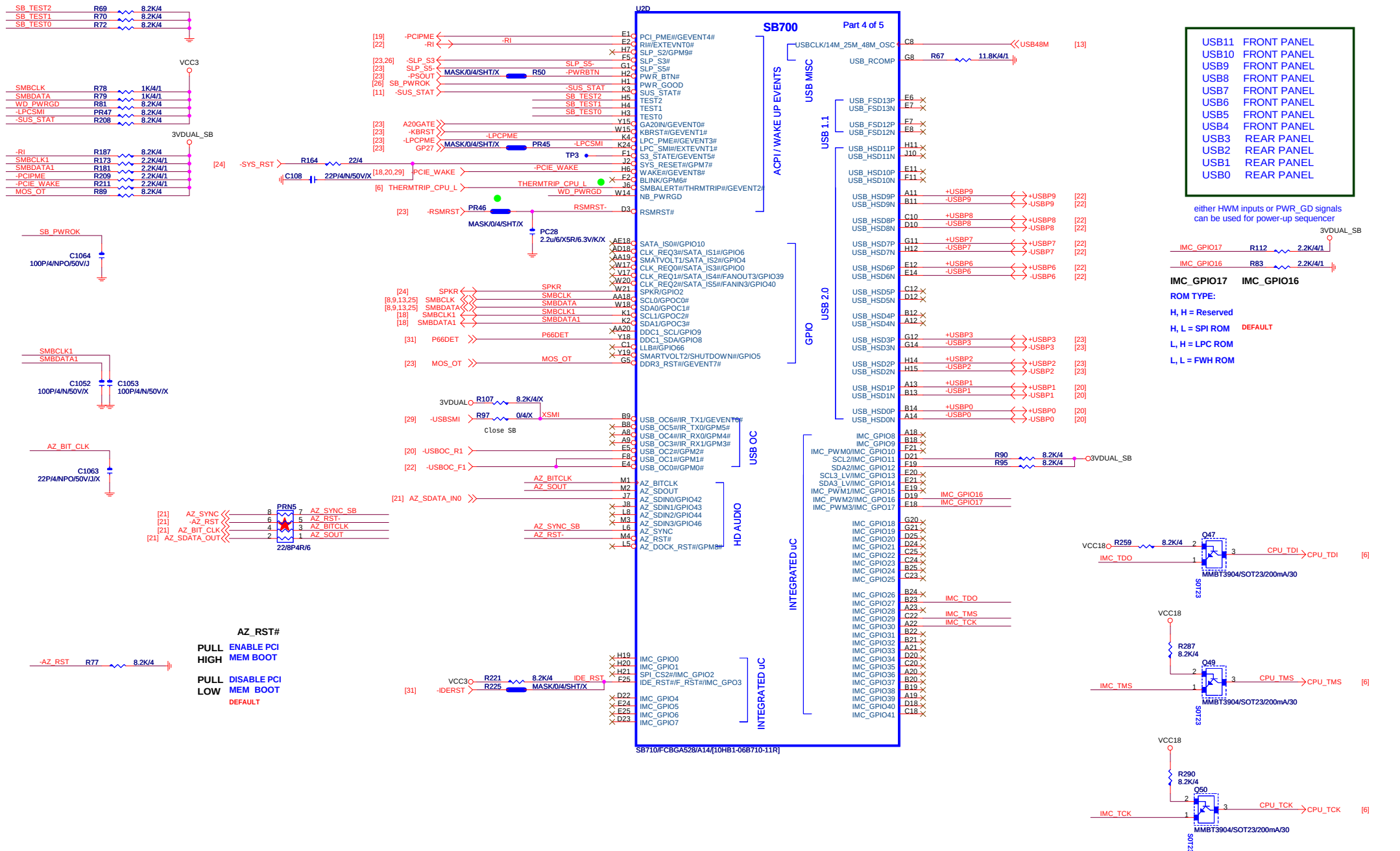


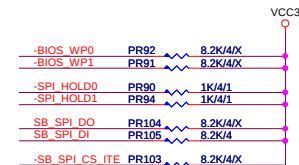
	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

**SEL_HTT66/REF0		OUT 3.3V 14.318MHz REF output.
IN	Low	100MHz differential HT clock, (Internal 120KΩ pull-down)
	High	66MHz 3.3V single ended HT clock.

GIGABYTE™

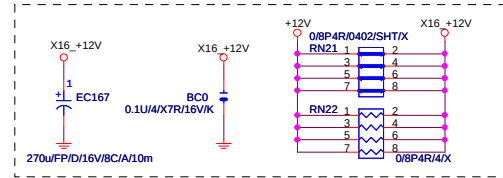
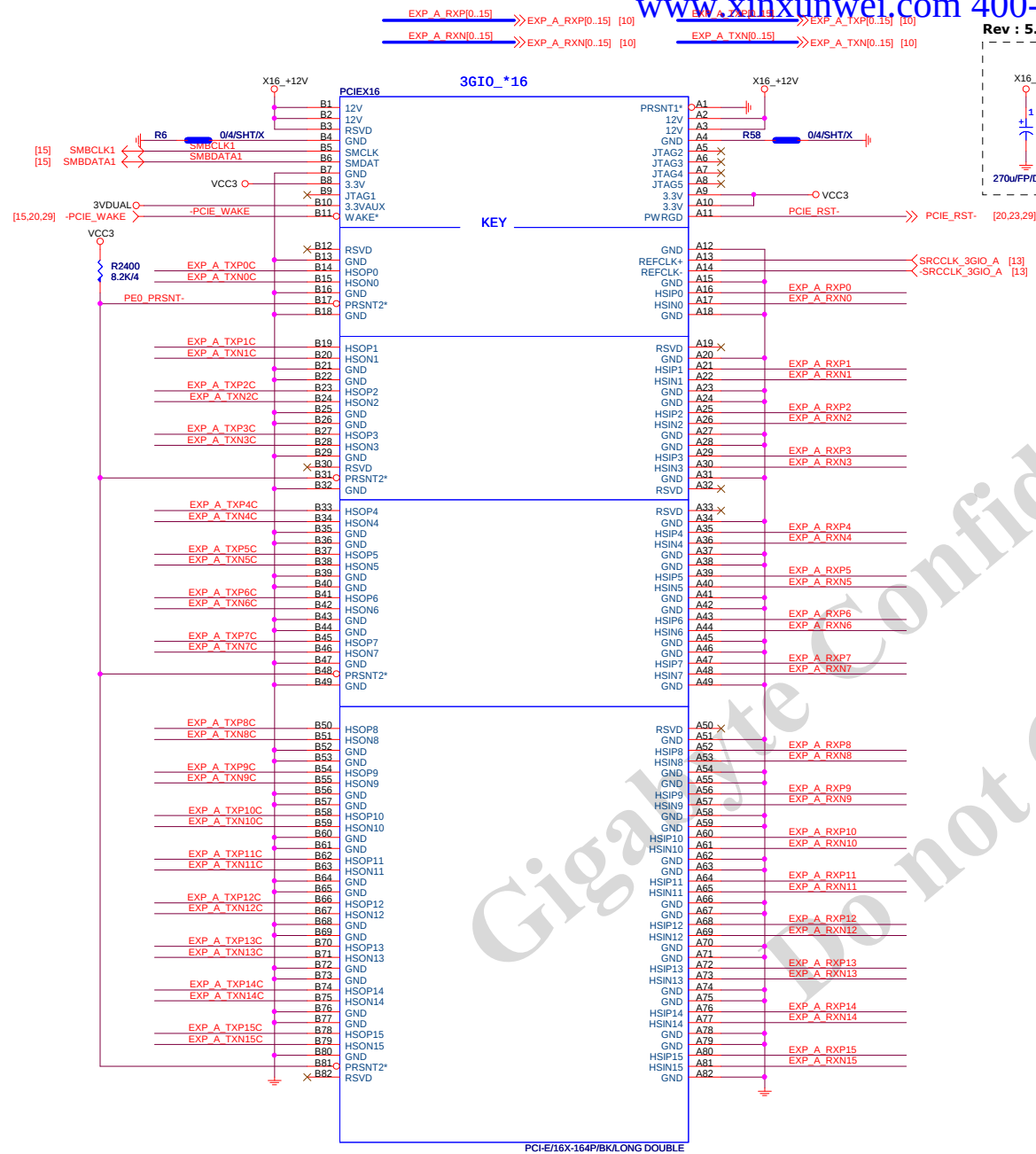
Title			RTM880T-792
Size	Document Number	Rev	
Custom	GA-78LMT-USB3	6.01	
Date:	Friday, October 31, 2014	Sheet	13 of 31



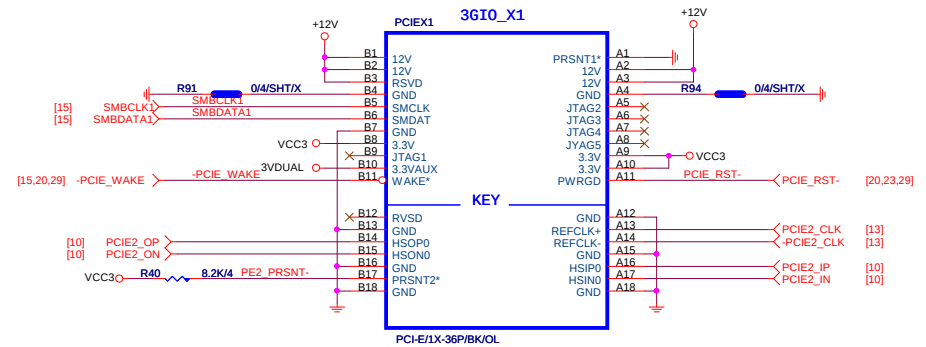
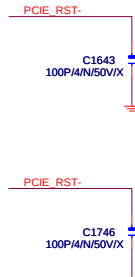


U2E		SB700	
		VSS_1	A2
		VSS_2	A25
		B1	VSS_3
		VSS_3	D7
		VSS_4	F20
		VSS_5	G19
T10	AVSS_SATA_1	VSS_6	H8
U10	AVSS_SATA_2	VSS_7	K3
U12	AVSS_SATA_3	VSS_8	K11
V11	AVSS_SATA_4	VSS_9	K18
V14	AVSS_SATA_5	VSS_10	K16
W9	AVSS_SATA_6	VSS_11	L7
	AVSS_SATA_7	VSS_12	L14
Y11	AVSS_SATA_8	VSS_13	L7
	AVSS_SATA_9	VSS_14	L11
Y14	AVSS_SATA_10	VSS_15	L12
Y17	AVSS_SATA_11	VSS_16	L12
AA9	AVSS_SATA_12	VSS_17	L16
AB0	AVSS_SATA_13	VSS_18	M6
AB11	AVSS_SATA_14	VSS_19	M10
AB13	AVSS_SATA_15	VSS_20	M11
AB15	AVSS_SATA_16	VSS_21	M13
AB17	AVSS_SATA_17	VSS_22	M15
AC6	AVSS_SATA_18	VSS_23	N4
AD8	AVSS_SATA_19	VSS_24	N12
AE8	AVSS_SATA_20	VSS_25	N14
		VSS_26	P9
		VSS_27	P10
		VSS_28	P11
A15	AVSS_USB_1	VSS_29	P17
B15	AVSS_USB_2	VSS_30	P13
C14	AVSS_USB_3	VSS_31	P15
D8	AVSS_USB_4	VSS_32	R1
D9	AVSS_USB_5	VSS_33	R4
D11	AVSS_USB_6	VSS_34	R4
D13	AVSS_USB_7	VSS_35	R4
D14	AVSS_USB_8	VSS_36	R10
D15	AVSS_USB_9	VSS_37	R12
E15	AVSS_USB_10	VSS_38	R14
F12	AVSS_USB_11	VSS_39	T11
G9	AVSS_USB_12	VSS_40	T12
H9	AVSS_USB_13	VSS_41	T14
H17	AVSS_USB_14	VSS_42	U6
J9	AVSS_USB_15	VSS_43	U14
J11	AVSS_USB_16	VSS_44	V16
J12	AVSS_USB_17	VSS_45	V18
J14	AVSS_USB_18	VSS_46	AB1
J15	AVSS_USB_19	VSS_47	AB19
K10	AVSS_USB_20	VSS_48	AB25
K12	AVSS_USB_21	VSS_49	AE1
K14	AVSS_USB_22	VSS_50	AE24
K15	AVSS_USB_23		
	AVSS_USB_24		
		PCIE_CK_VSS_9	P23
		PCIE_CK_VSS_10	R16
		PCIE_CK_VSS_11	T17
		PCIE_CK_VSS_12	U18
		PCIE_CK_VSS_13	U20
H18	PCIE_CK_VSS_1	PCIE_CK_VSS_14	U20
J22	PCIE_CK_VSS_2	PCIE_CK_VSS_15	V18
K25	PCIE_CK_VSS_3	PCIE_CK_VSS_16	V21
K26	PCIE_CK_VSS_4	PCIE_CK_VSS_17	W19
M12	PCIE_CK_VSS_5	PCIE_CK_VSS_18	W19
M17	PCIE_CK_VSS_6	PCIE_CK_VSS_19	W22
P16	PCIE_CK_VSS_7	PCIE_CK_VSS_20	W24
	PCIE_CK_VSS_8	PCIE_CK_VSS_21	W25
F9	AVSSC	AVSSC	L17
Part 5 of 5			
SB710-CBG45A28/A14[10]HBI-06B710-1R			

Title			
ATI SB710 POWER & GND			
Size	Document Number	Rev	
Custom	GA-78LMT-USB3	6.01	
Date:	Friday, October 31, 2014	Sheet	17 of 31

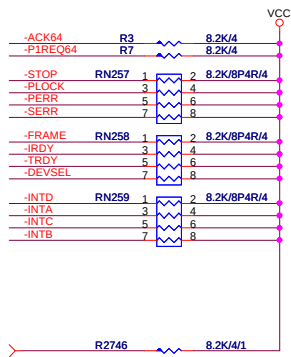
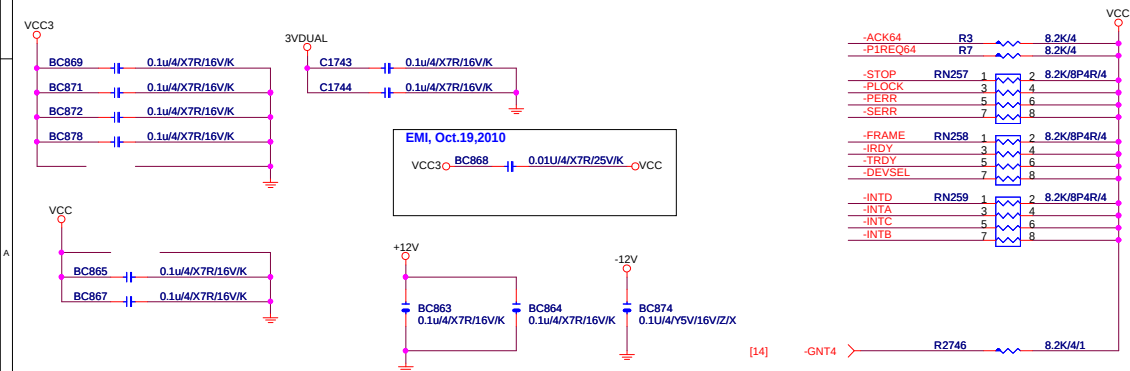
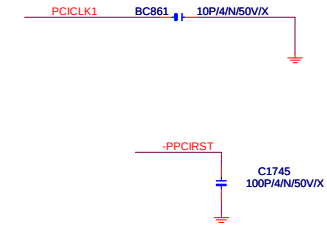
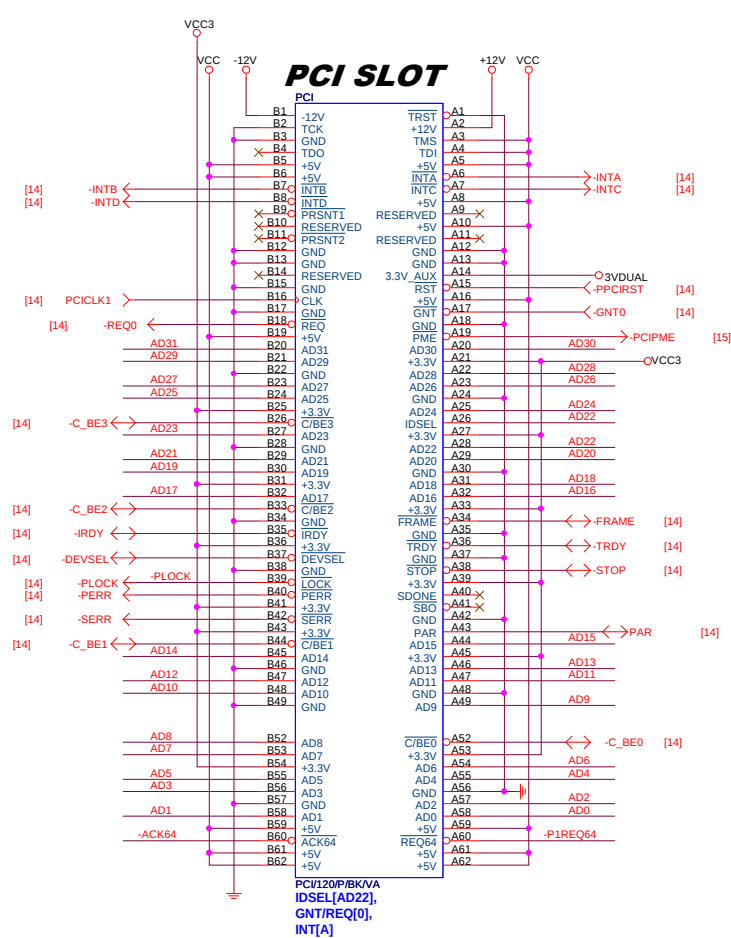


EXP A TXP0	C1644	0.1U/4XTR16V/K	EXP A TXP0C
EXP A TXP1	C1645	0.1U/4XTR16V/K	EXP A TXP1C
EXP A TXP2	C1646	0.1U/4XTR16V/K	EXP A TXP2C
EXP A TXN1	C1647	0.1U/4XTR16V/K	EXP A TXN1C
EXP A TXN2	C1648	0.1U/4XTR16V/K	EXP A TXN2C
EXP A TXN3	C1649	0.1U/4XTR16V/K	EXP A TXN3C
EXP A TXP3	C1650	0.1U/4XTR16V/K	EXP A TXP3C
EXP A TXN3	C1651	0.1U/4XTR16V/K	EXP A TXN3C
EXP A TXP4	C1652	0.1U/4XTR16V/K	EXP A TXP4C
EXP A TXN4	C1653	0.1U/4XTR16V/K	EXP A TXN4C
EXP A TXP5	C1654	0.1U/4XTR16V/K	EXP A TXP5C
EXP A TXN5	C1655	0.1U/4XTR16V/K	EXP A TXN5C
EXP A TXP6	C1656	0.1U/4XTR16V/K	EXP A TXP6C
EXP A TXN6	C1657	0.1U/4XTR16V/K	EXP A TXN6C
EXP A TXP7	C1658	0.1U/4XTR16V/K	EXP A TXP7C
EXP A TXN7	C1659	0.1U/4XTR16V/K	EXP A TXN7C
EXP A TXP8	C1660	0.1U/4XTR16V/K	EXP A TXP8C
EXP A TXN8	C1661	0.1U/4XTR16V/K	EXP A TXN8C
EXP A TXP9	C1662	0.1U/4XTR16V/K	EXP A TXP9C
EXP A TXN9	C1663	0.1U/4XTR16V/K	EXP A TXN9C
EXP A TXP10	C1664	0.1U/4XTR16V/K	EXP A TXP10C
EXP A TXN10	C1665	0.1U/4XTR16V/K	EXP A TXN10C
EXP A TXP11	C1666	0.1U/4XTR16V/K	EXP A TXP11C
EXP A TXN11	C1667	0.1U/4XTR16V/K	EXP A TXN11C
EXP A TXP12	C1668	0.1U/4XTR16V/K	EXP A TXP12C
EXP A TXN12	C1669	0.1U/4XTR16V/K	EXP A TXN12C
EXP A TXP13	C1670	0.1U/4XTR16V/K	EXP A TXP13C
EXP A TXN13	C1671	0.1U/4XTR16V/K	EXP A TXN13C
EXP A TXP14	C1672	0.1U/4XTR16V/K	EXP A TXP14C
EXP A TXN14	C1673	0.1U/4XTR16V/K	EXP A TXN14C
EXP A TXP15	C1674	0.1U/4XTR16V/K	EXP A TXP15C
EXP A TXN15	C1675	0.1U/4XTR16V/K	EXP A TXN15C



PCI SLOT 1,2

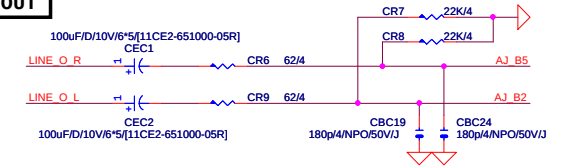
[14] AD[0..31] <--> AD[0..31]



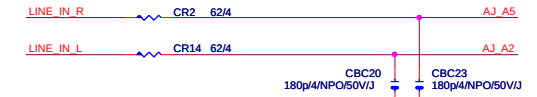
GIGABYTE™

Title			
PCI SLOT			
Size	Document Number	Rev	
Custom	GA-78LMT-USB3	6.01	
Date:	Friday, October 31, 2014	Sheet	19 of 31

LINE-OUT

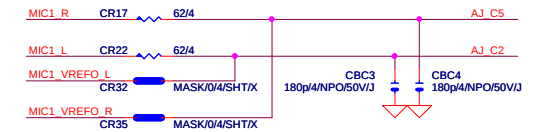


LINE-IN

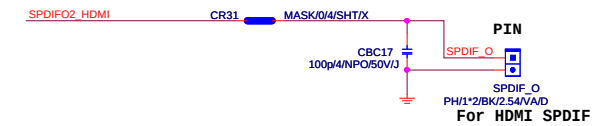


For 889A/888

MIC-IN

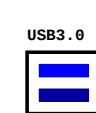


SPDIFO

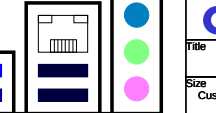


Connect AUDIO & LAN CONN AGND

USB 3.0



Connect AUDIO & LAN CONN AGND



GIGABYTE™		
Title ALC892 CODEC		
Size Custom	Document Number GA-78LMT-USB3	Rev 6.01
Date: Friday, October 31, 2014	Sheet 21	of 31

co-layout

50欧姆: 4/7.5

SPDIF_OUT

Digital Area

Analog Area

JD resistors close to pin13 of CODEC

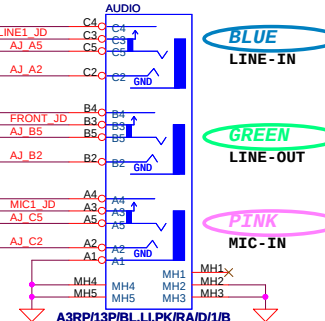
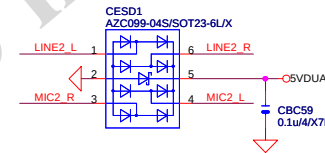
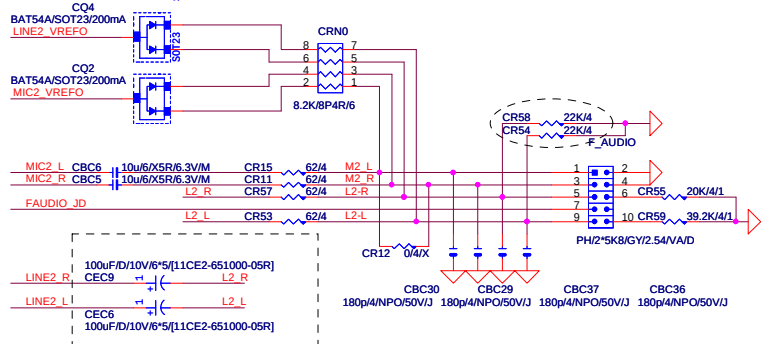
JD resistors close to pin34 of CODEC

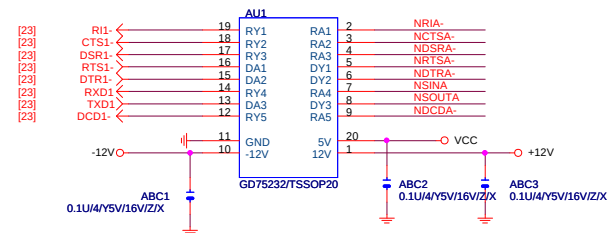
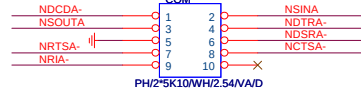
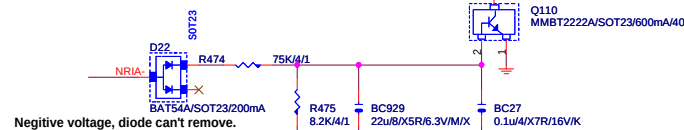
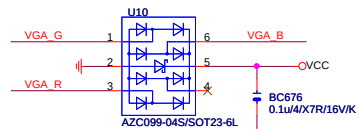
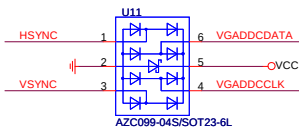
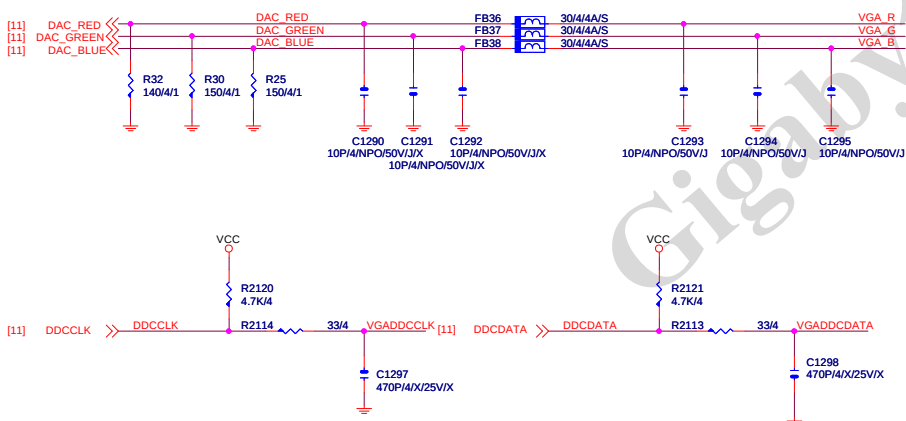
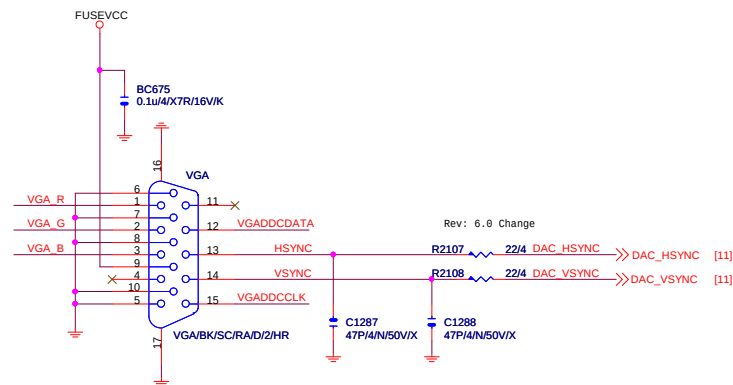
Can Support Amp Out

AZALIA FRONT PANEL

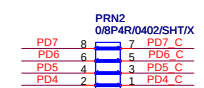
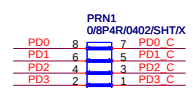
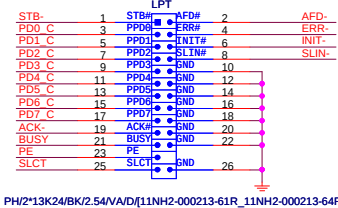
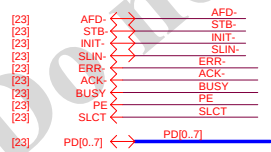
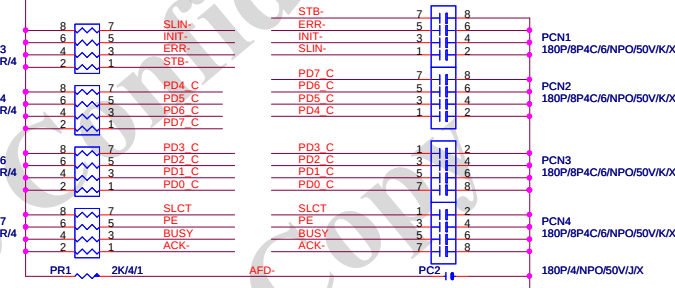
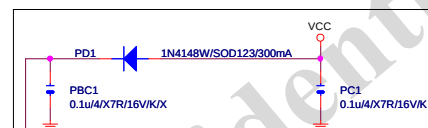
SSOP6-1

VT1708S :3.3K

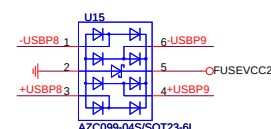
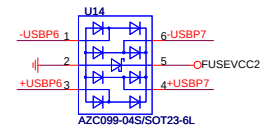
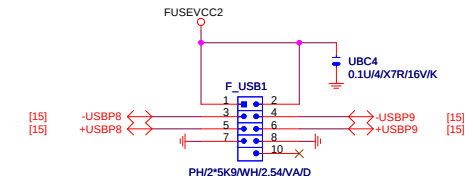
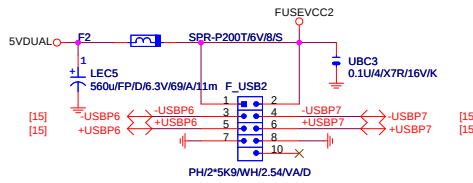


**VGA**

LPT



USB 2.0



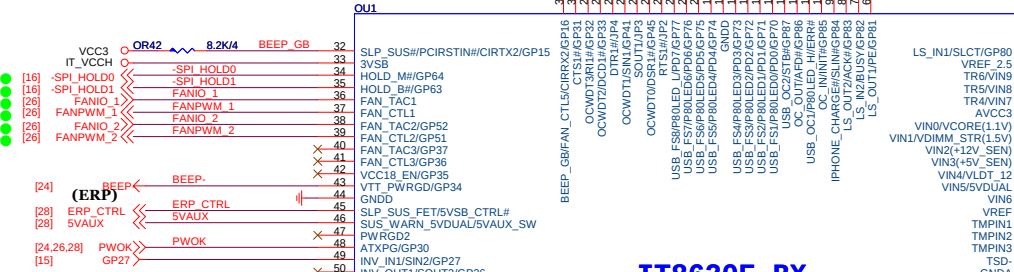
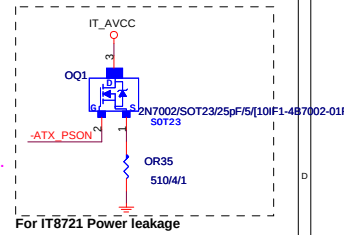
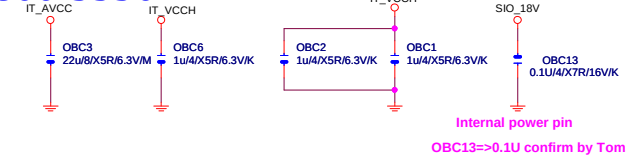
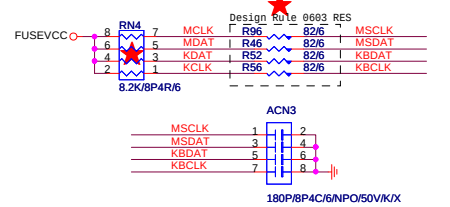
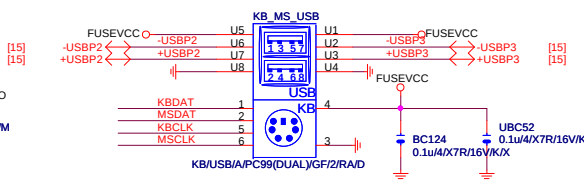
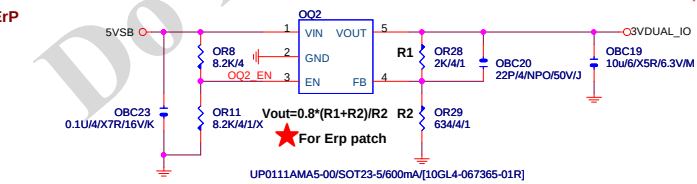
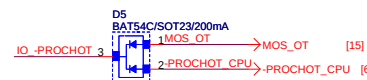
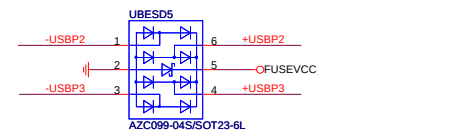
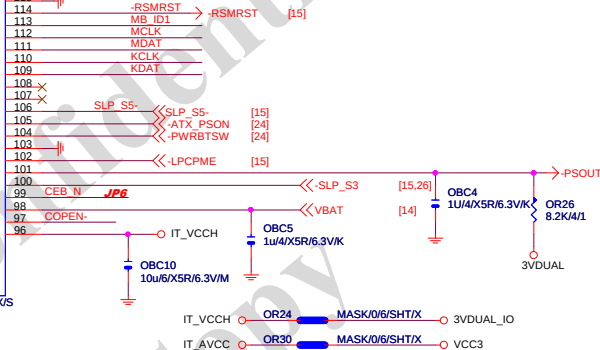
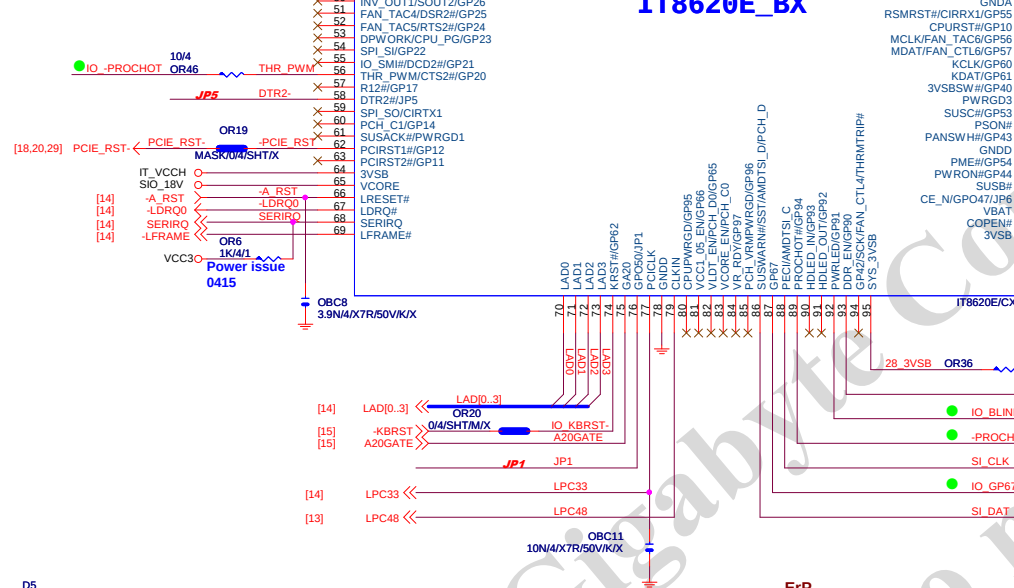
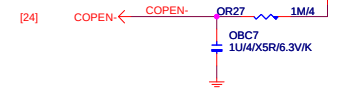


Figure 10 shows the pin connections for the ADXL345. The connections are as follows:

- Pin 5: SLCT, connected to SLCT and 2_SLEVEL.
- Pin 4: TR4, connected to MASK/04/SHT/TX and OR54.
- Pin 128: IT_AVCC, connected to MOS_TEMP.
- Pin 127: VIN0.
- Pin 126: VIN1.
- Pin 125: VIN2.
- Pin 124: VIN3.
- Pin 123: VIN4.
- Pin 122: VREF.
- Pin 120: TEMP1, connected to BC885 and 2.2n/4/X7R/50V/K.
- Pin 119: TMPIN2, connected to TMPIN2.
- Pin 118: TMPIN2.
- Pin 117: TSD+, connected to OR22 and 04/SHT/TM/TX.
- Pin 116: TSD-.



JP1 JP1 OR38 8.2K/4X IT_VCCH
OR53 8.2K/4X

JP2 RTS1- OR0 8.2K/4 VCC3

JP3 TXD1 OR1 8.2K/4 VCC3

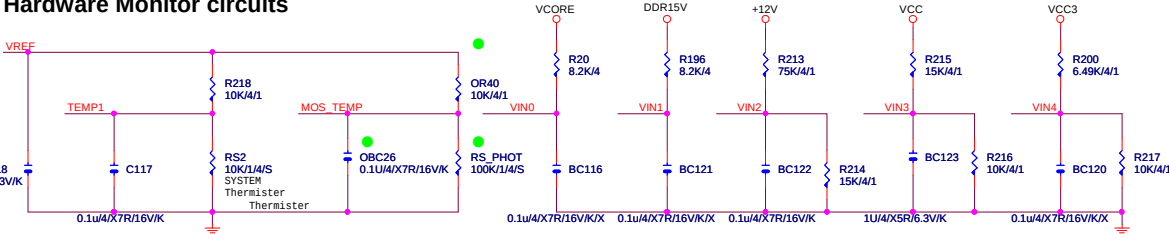
O: EN SPI, I:DIS SPI

JP4 DTR1- OR2 8.2K/4 VCC3

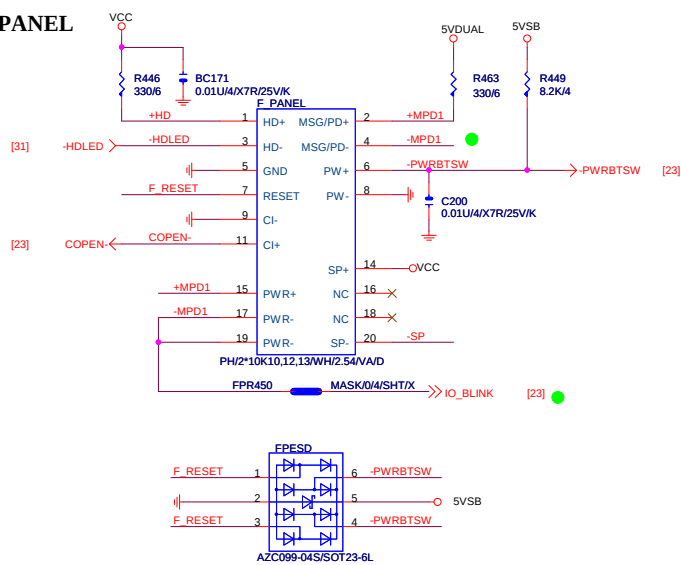
JP5 DTR2- OR4 1K/4/1X VCC3
OR37 1K/4/1X

DTR2- ite recomment change to IT_VCCH

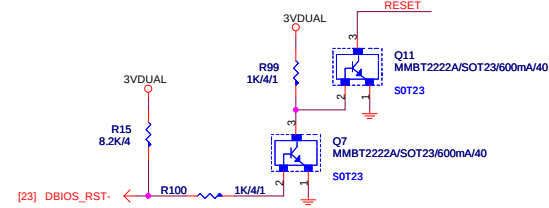
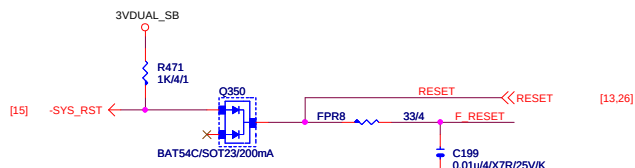
JP6 CEB_N OR5 1K/4/1 VCC3



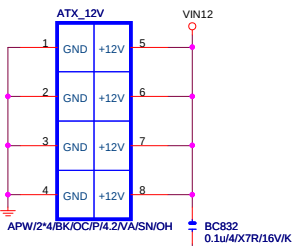
FRONT PANEL



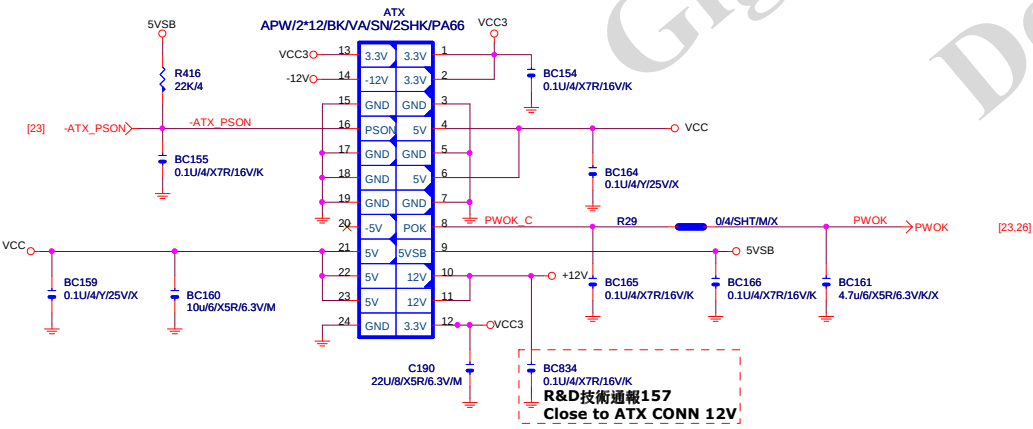
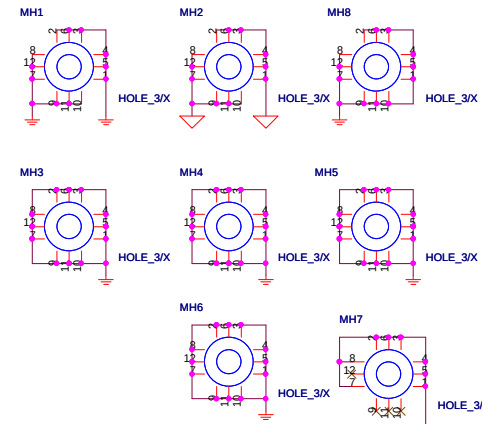
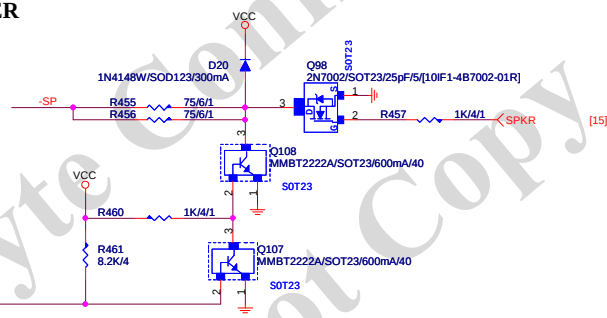
www.gigabyte.com 400-800-9990



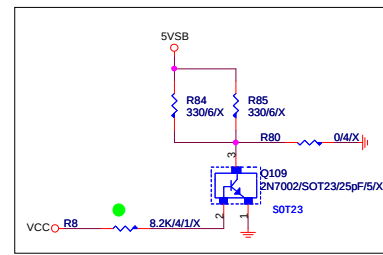
ATX POWER CONNECTOR



PC SPEAKER



5VSB MiniLoad



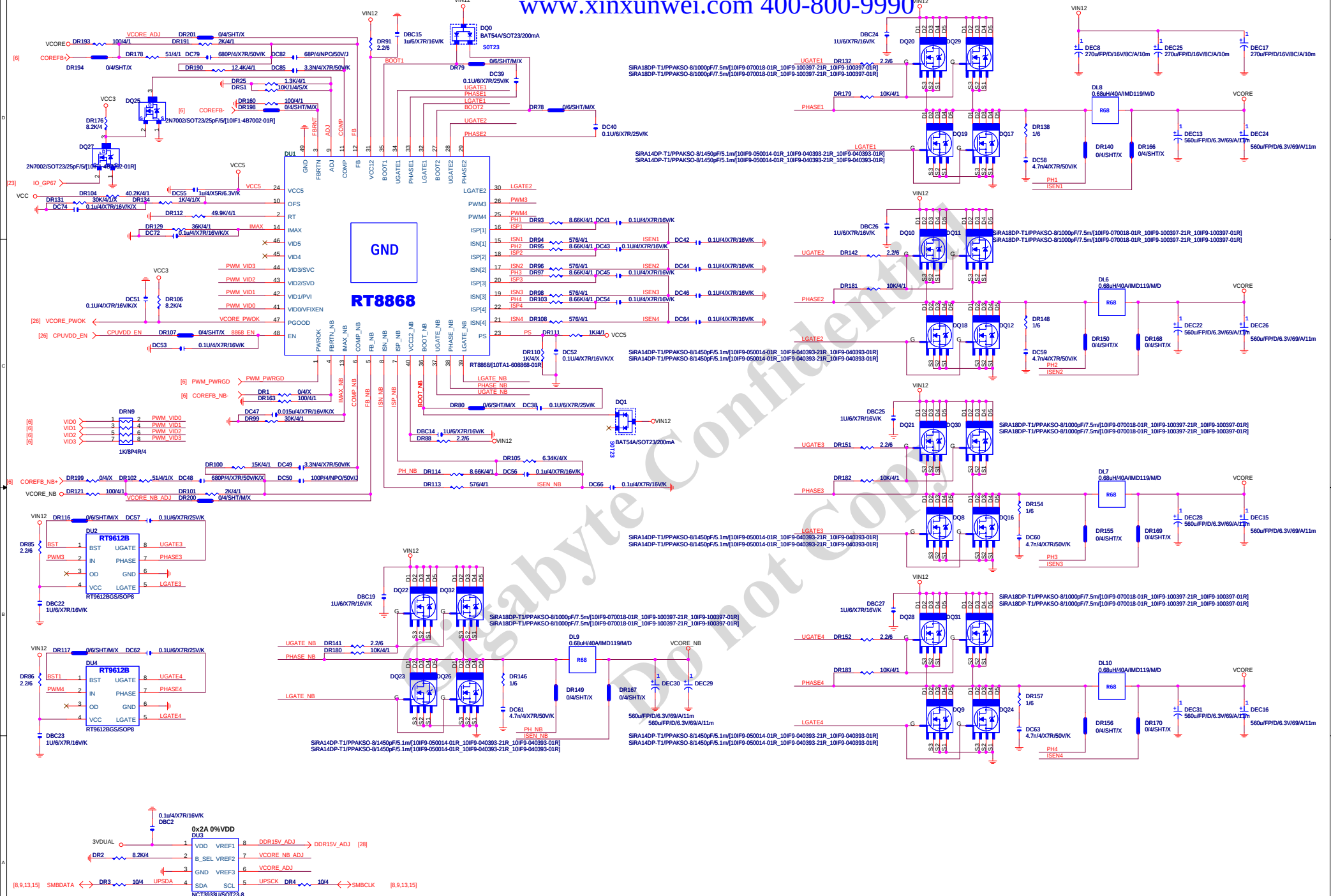
For S28/S12 Can't PWR-ON issue

GIGABYTE

ATX, FRONT PANEL

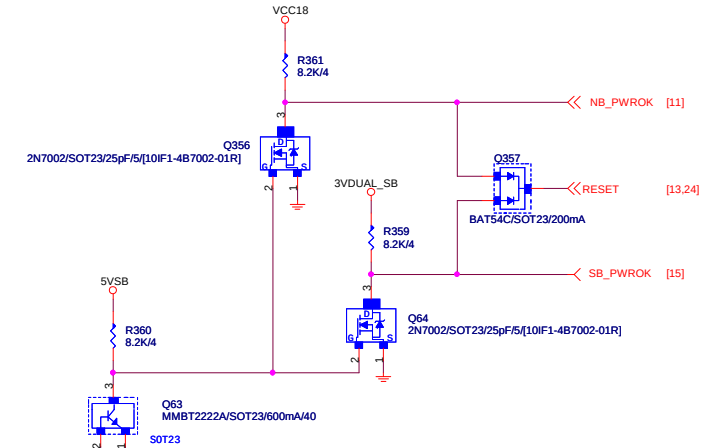
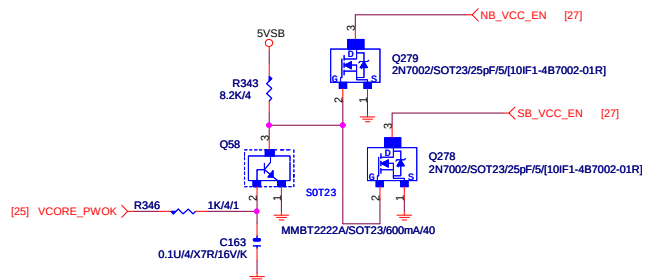
Size: Custom
Date: Friday, October 31, 2014
Sheet: 24 of 31

Rev: 6.01



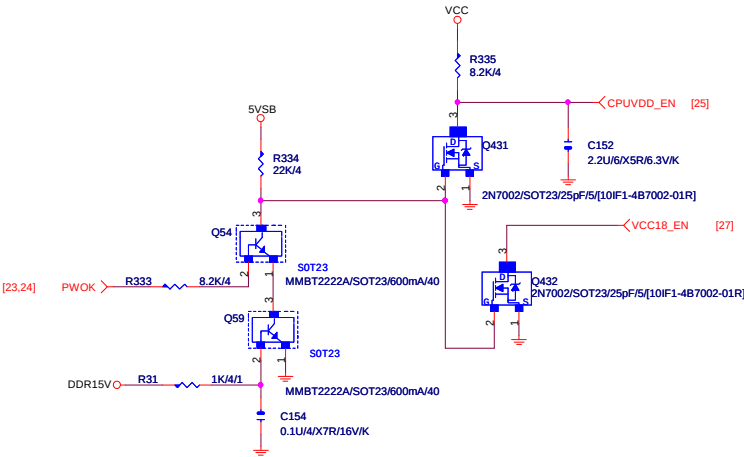
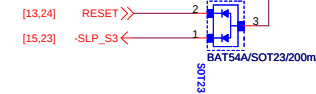
GIGABYTE™

Title		VCORE(RT8868+RT9612)	
Size	Document Number	GA-78LMT-USB3	Rev
C			6.01
Date:	Fri, Oct 31, 2014	Sheet	25 of 31

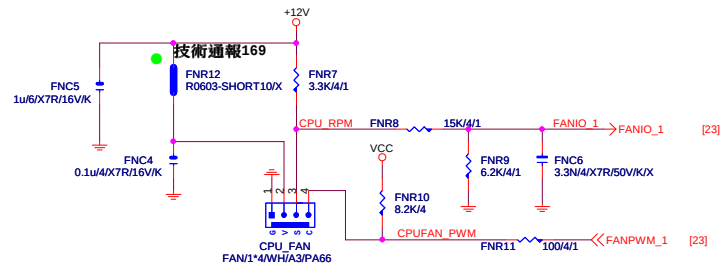


PWOK > NB_PWRGD / SB_PWRGD

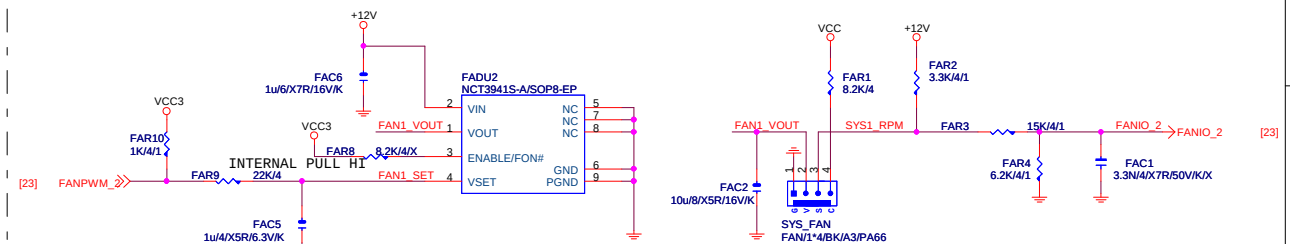
(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms



CPU_FAN PWM Mode

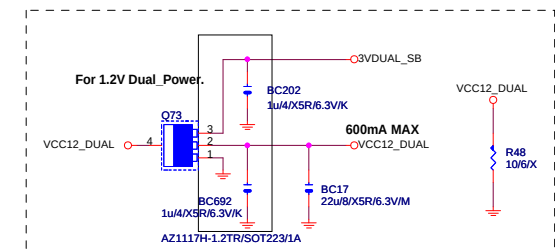
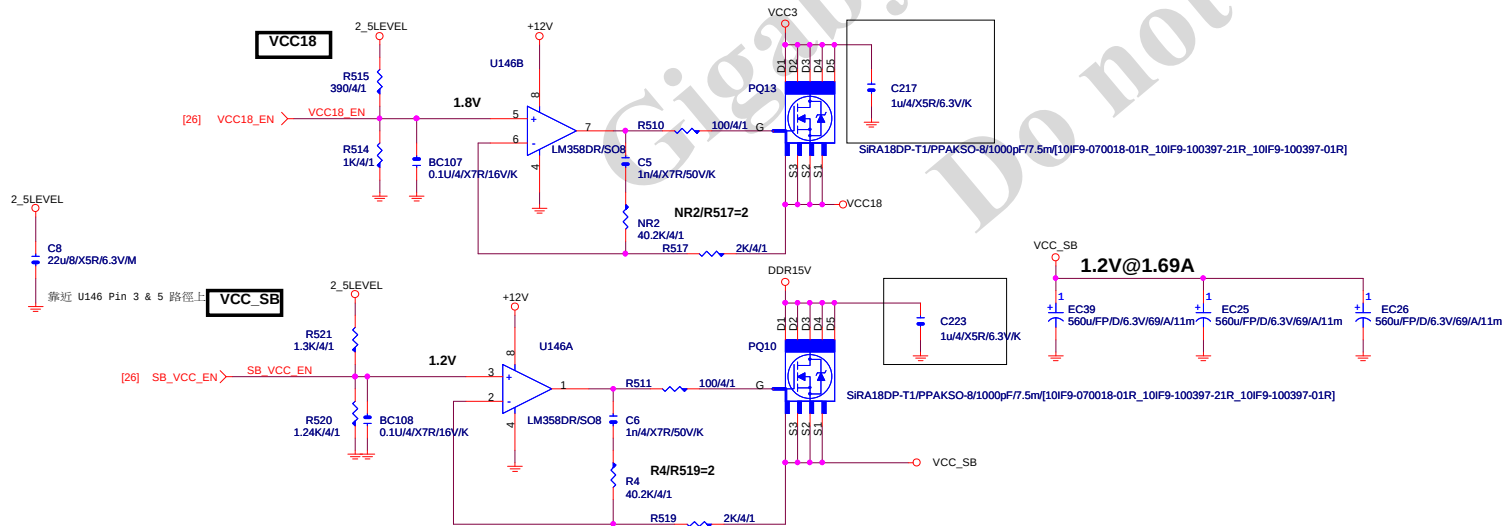
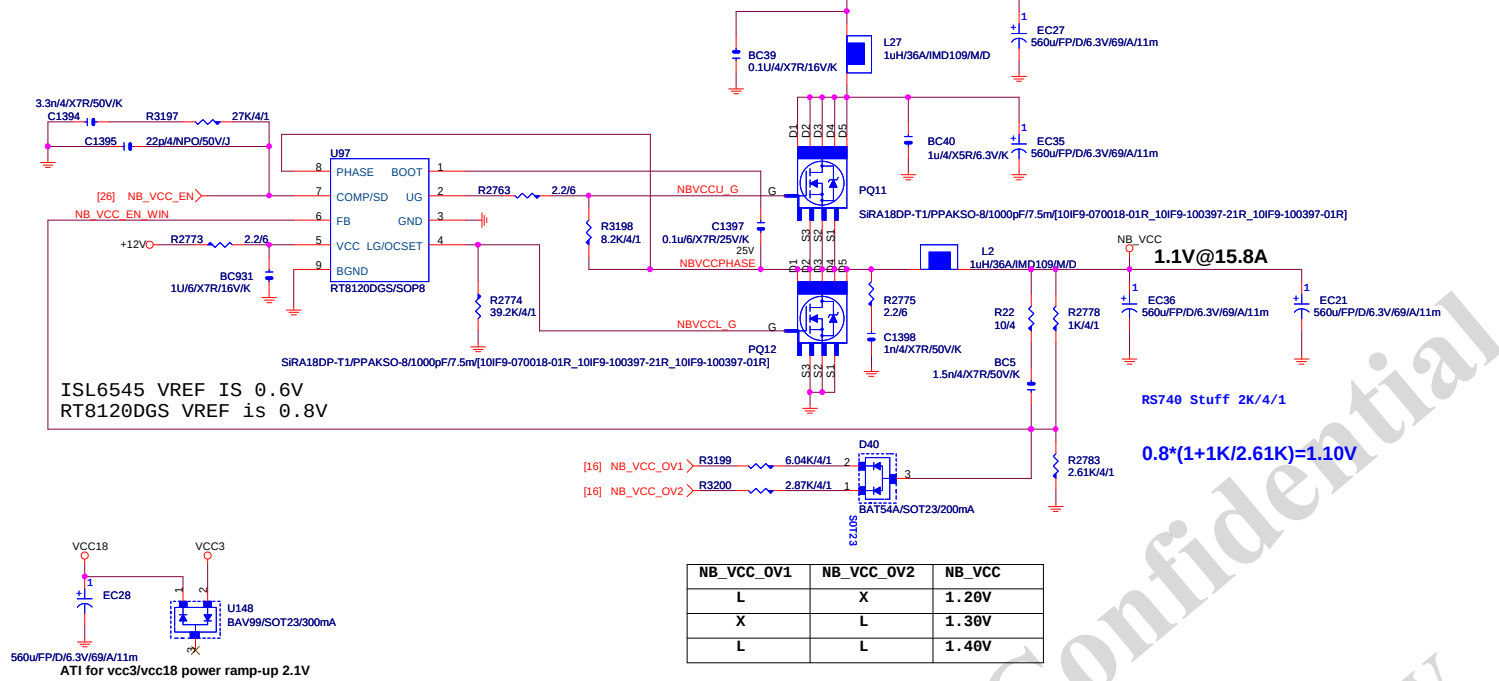


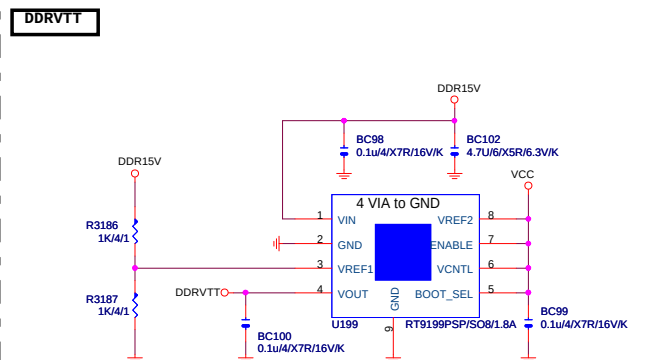
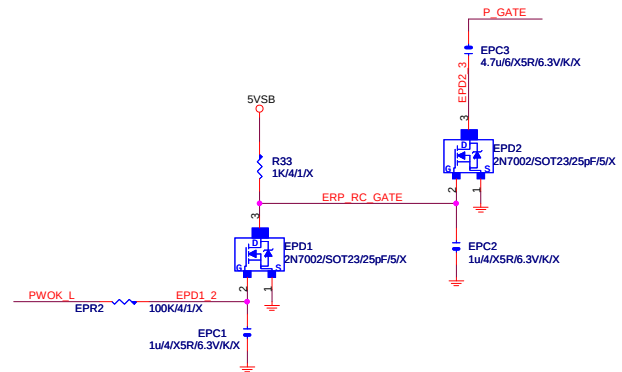
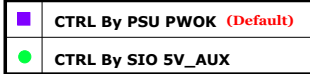
SYS_FAN Voltage Mode



GIGABYTE™

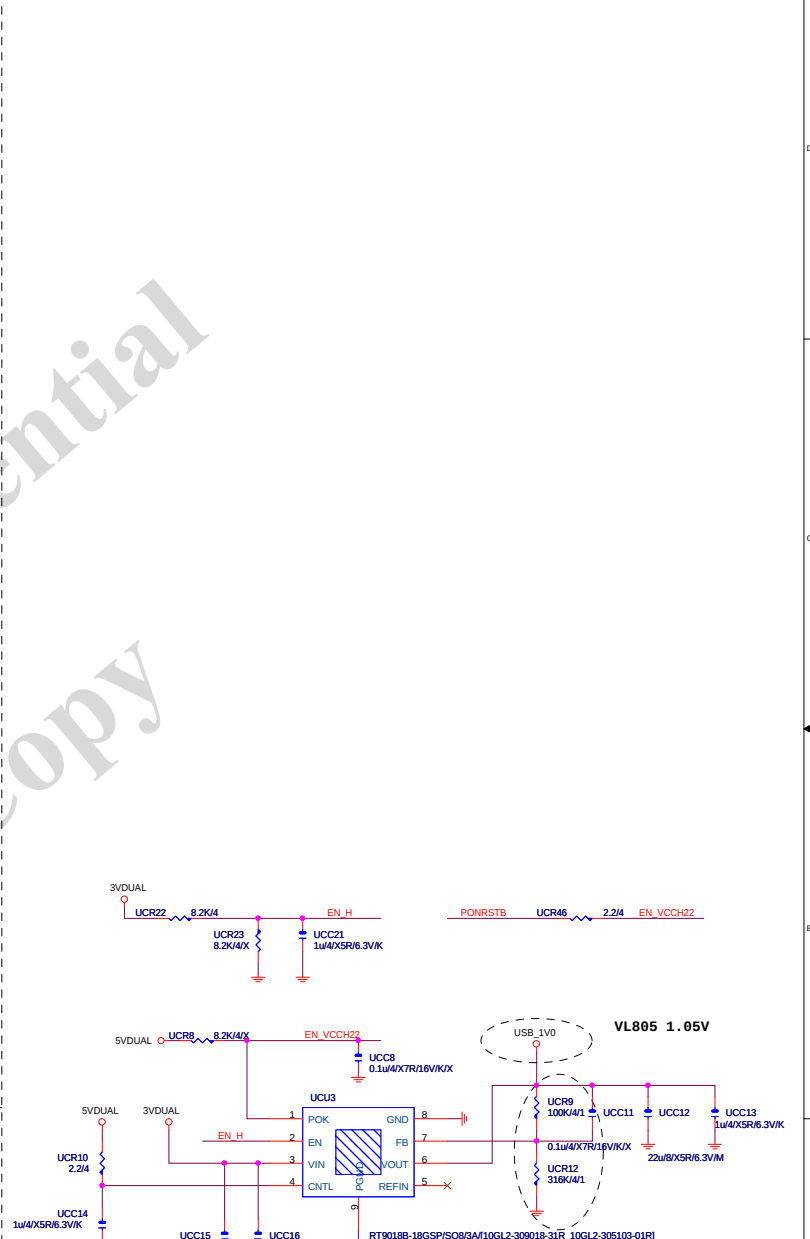
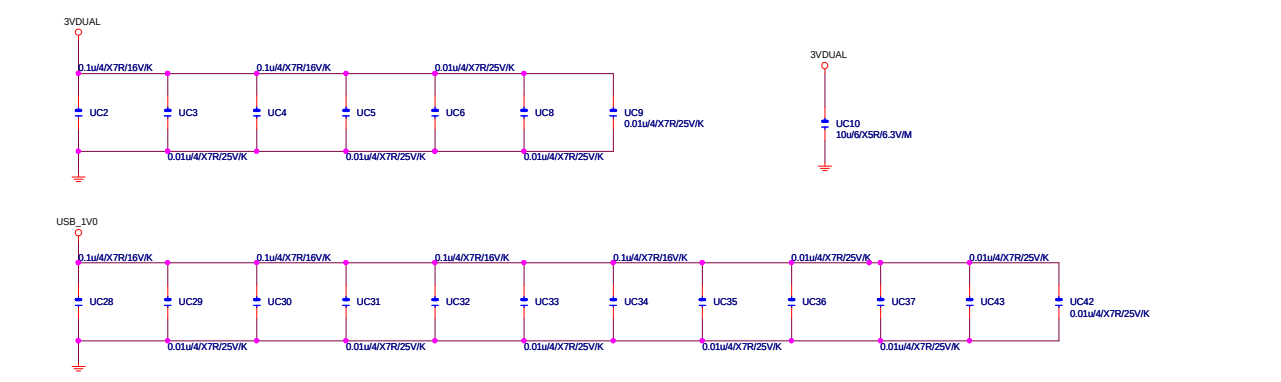
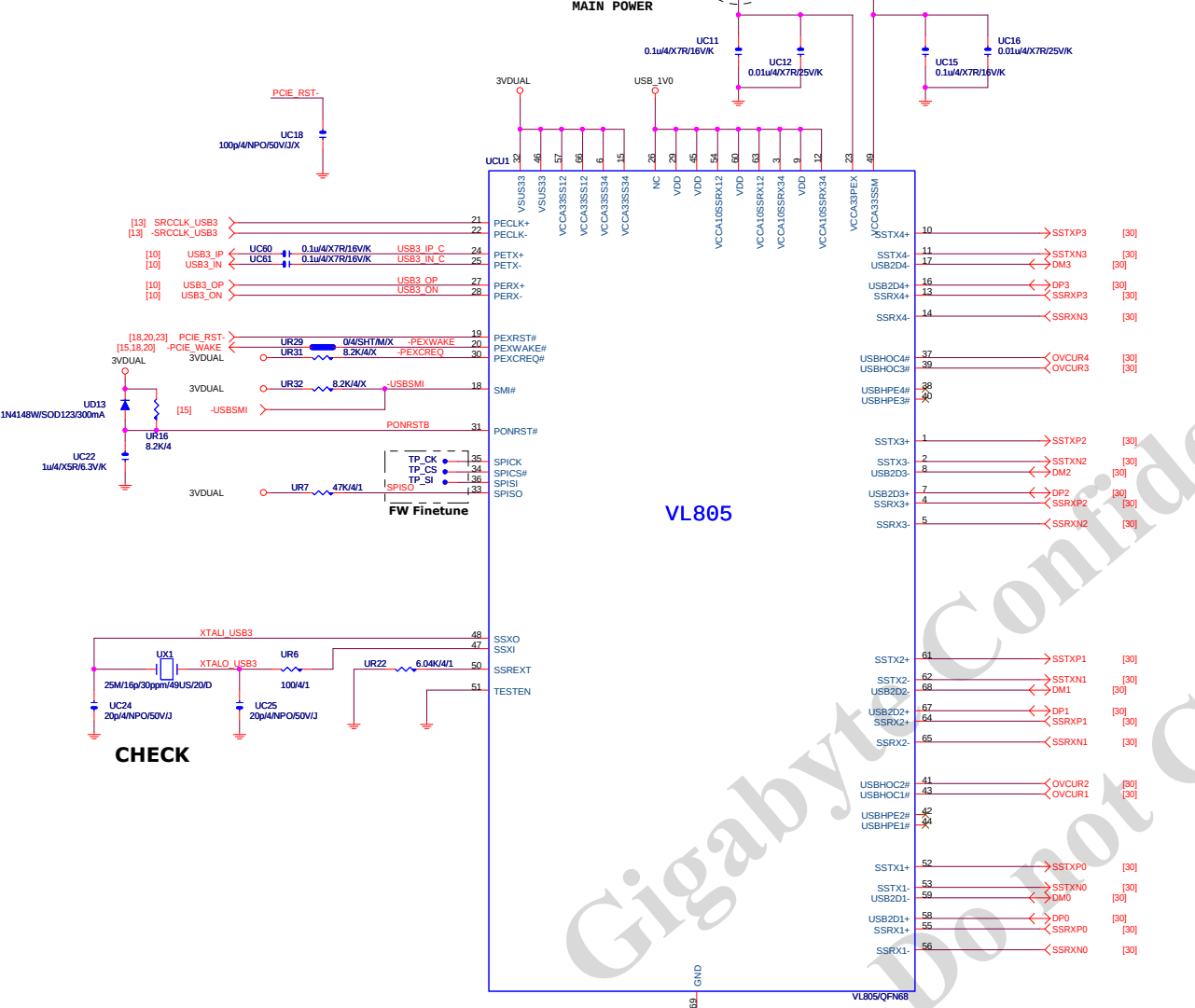
Title		
PWR Sequence & CPU/SYS_FAN		
Size	Document Number	Rev
Custom	GA-78LMT-USB3	6.01
Date:	Friday, October 31, 2014	Sheet 26 of 31



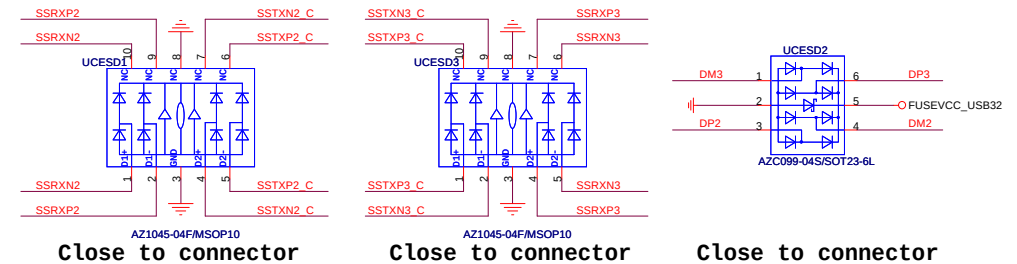


Title			
DDRIII POWER ,5VUDAL ,EUP			
Size	Document Number	Rev	
Custom	GA-78LMT-USB3	6.01	
Date:	Thursday, November 20, 2014	Sheet	28 of 31

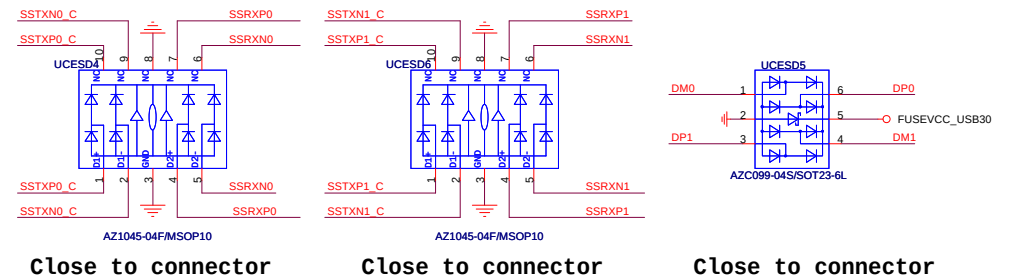
S3/S4 PCIE NEED
MAIN POWER

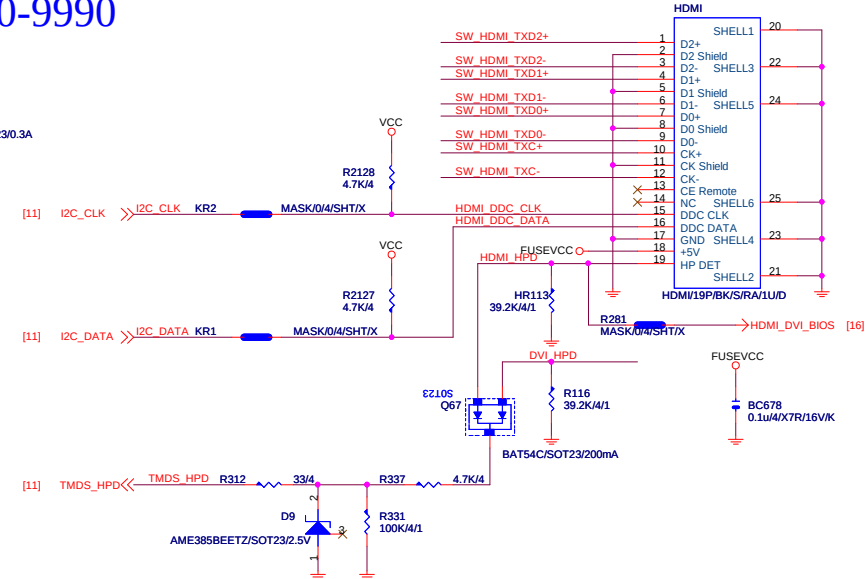
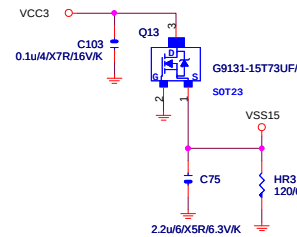
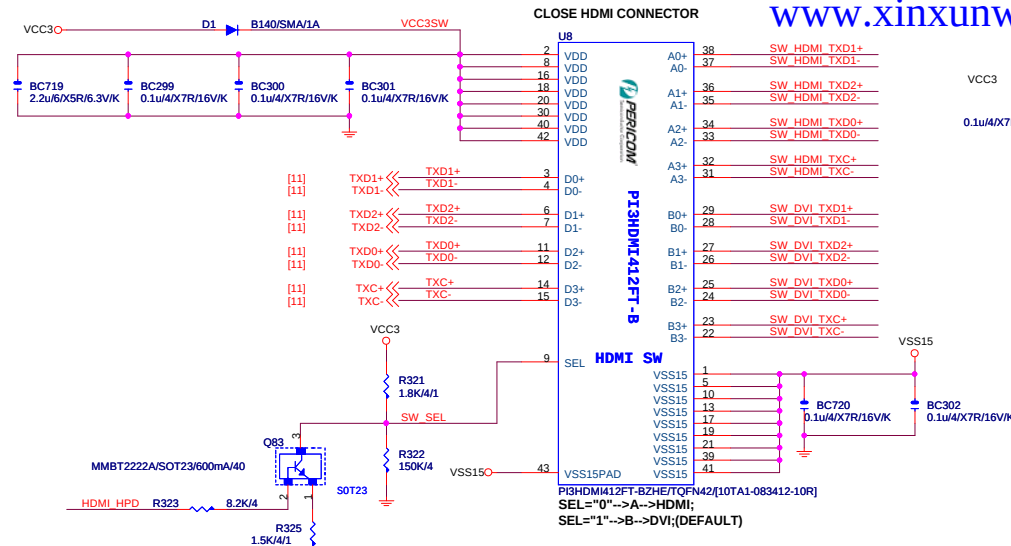


【技術通報R&D技術通報156】
RT9018 (RICHTEK)與NCT3730 (NUVOTON),
EM5103GE (EMC)做共用, 針對PIN7 (FB)分壓阻值部份
須做修改為100K以上電阻值



R_USB30





IDE

