AMD SP5100 Register Programming Requirements

Technical Reference Manual
Rev. 3.02

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Table of Contents

1 Introduction

1.1 About This Manual

This document lists the register settings required for the proper operation of the AMD SP5100 (previously referred to as SB700S). Current sampling of AMD SP5100 is with silicon revision A14 and A15, with the latter being the production part. This document covers settings for prior revision A12 (used exclusively for SB7xx products) as a reference since the SP5100 CIMx is shared between SP5100 and SB7xx. CIMx is a software module that helps OEMs to quickly integrate SP5100 support in their products. References to register settings for revision A12 apply only to SB7xx products. References to register settings for Revision A14, A14 and above, A15, or All Revs apply to SP5100.

Most of the register settings are mandatory and should be implemented as described in this document. The document will be updated periodically with new or revised settings that are determined during the qualification of the SP5100. Please refer to the latest updated document on the AMD NDA website.

This document should be used in conjunction with the related *AMD SP5100 BIOS Developer's Guide* and the *AMD SP5100 Register Reference Guide.*

Note: In this document, changes/additions from the previous release are highlighted in red. Refer to Appendix B: Revision History at the end of this document for a detailed revision history.

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1.2 AMD SP5100 Block Diagram

This section contains a block diagram for the SP5100. *Figure 1* below shows the SP5100 internal PCI devices and major functional blocks.

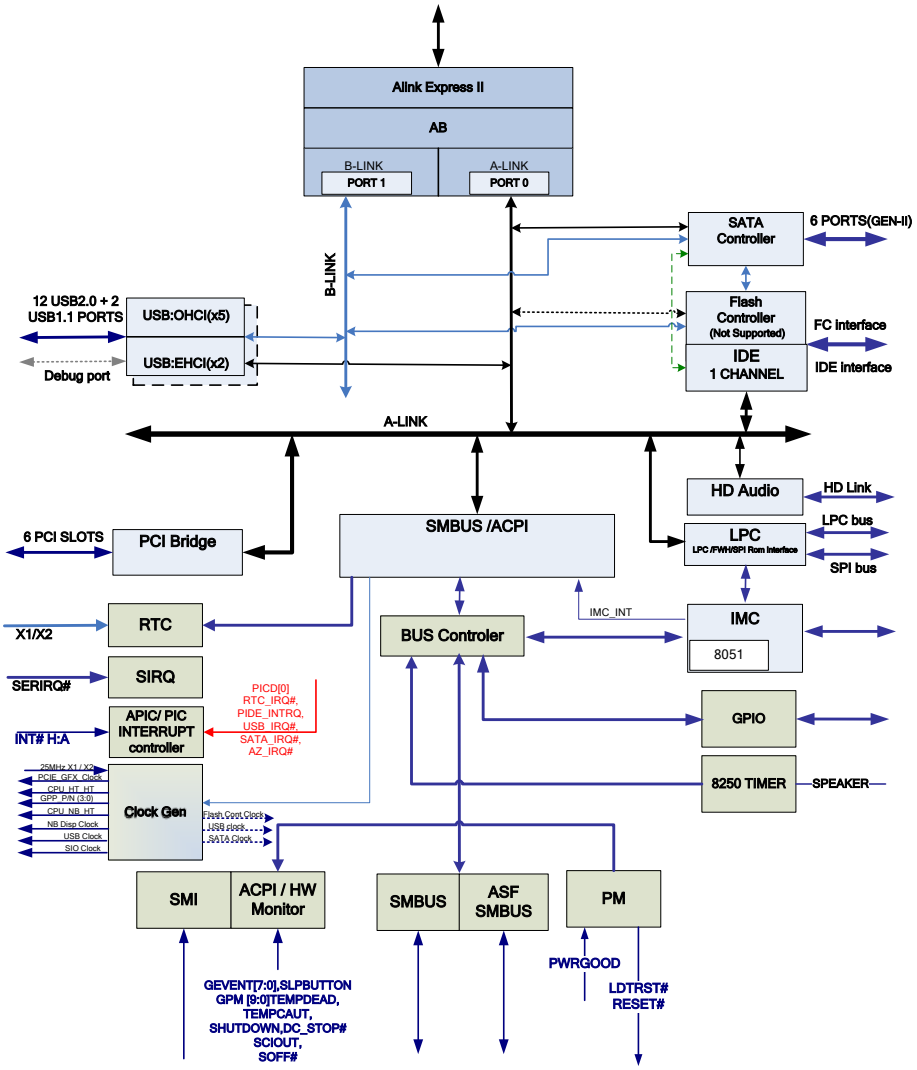

Figure 1 SP5100 Internal PCI Devices and Major Functional Blocks

1.3 Register Reference Information

Tables within this document contain information showing the applicable revision, recommended settings, and comments associated with the register. Consider the following example:

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PM_IO 0x52[5:0] = 08h	Recommended Delay for S3/S4/S5 resume sequence

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide.
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

- ASIC Rev → All Revs SP5100 = Applicable to all revisions of the SP5100
- ASIC Rev → SP5100 A14 and above = Applicable to revisions A14 and A15 of the SP5100
- ASIC Rev → SP5100 A14 = Applicable to revision A14 of the SP5100
- ASIC Rev → SP5100 A12 = Not applicable, included for reference only (see section 1.1 “About this Manual”)
- Register Settings → Recommended register setting with the register name.

For more detailed information about the registers found within this document refer to the *AMD SP5100 Register Reference Guide*. The applicable sections in the register reference guide where the information can be found are marked with “x” in the tables in this document.

2 ACPI/SMBUS Controller (bus-0, dev-20, fun-0)

2.1 Enabling Legacy Interrupt

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Smbus_PCI_config 0x62 [2] = 1	This bit enables legacy interrupt.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
		x						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

2.2 Unblocked SMI Command Port

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Smbus_PCI_config 0xAC [4] = 0	Set the bit to 0 to disable unblocked smi delivery from smi command port so that smi from smi command port is gated by EOS bit too.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
		x						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

2.3 WakeIO Base Address

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Smbus_PCI_config 0xF4 [15:0]	This register is the I/O base address used to generate the C-state wake event by the processor. The BIOS should program this register with the I/O base address for the SP5100. The base address in the CPU should also be programmed. The CPU can use it to generate an I/O write to the SB to wake the system from the C-state.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
		x						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

2.4 C-State and VID/FID Change

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	BIOS should not report ARB_DIS to OS if C3 pop-up is enabled.	With C3 pop-up, ARB_DIS should not be set or cleared by software.
	PM_IO 0x9A [5] = 1	For system with dual core CPU, set this bit to 1 to automatically clear BM_STS when the C3 state is being initiated.

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PM_IO 0x9A [4] = 1	For system with dual core CPU, set this bit to 1 and BM_STS will cause C3 to wakeup regardless of BM_RLD.
All Revs SP5100	PM_IO 0x8F [5] = 1	Ignores BM_STS_SET message from NB
All Revs SP5100 + RS4x0 ASIC family of NB	PM_IO 0x8F [4] = 1	The SB will monitor BmReq# for C3 pop-up. The SB will de-assert LDTSTP# when BmReq# is active.
All Revs SP5100 + RS690 ASIC family of NB	PM_IO 0x8F [4] = 0	The SB will not monitor BmReq# for C3 pop-up. The SB will de-assert LDTSTP# when AllowLdtStop is not active. BmReq# activity is combined on AllowLdtStop in the RS690 ASIC family of NB.
Stutter time: The following setting is for Stutter time (minimum time LDTSTP# is asserted before entering C3 state). There are two settings that apply to different cases as listed below. **Case 1:** The following registers should be programmed only when Platform BIOS detects the CPUs listed below: • Family 10h with LS2 mode capability enabled: Model=(8|9) && Stepping >= 1 || Model Ah OR for any CPU that has the HT link speed set to 200 MHz. • Family 15h with LS2 mode capability enabled: Model= (00-0Fh) && C32r1 package || Model= (00-0Fh) && G34r1 package **Case 2:** Any CPU that does not meet the requirements set in Case 1.		
All Revs SP5100	PM_IO 0x8B = 0x0A	**Case 1:** StutterTime = 0x0A for minimum LDTSTP# assertion duration of 10 us in C3.
	PM_IO 0x8B = 0x01	**Case 2:** StutterTime = 01h for minimum LDTSTP# assertion duration of 1us in C3.
All Revs SP5100	PM_IO 0x8A = 0x90	Bit[7] - Enable Stutter Mode for C3 Bits[6:4] - VidFidTime = 001b for LDTSTP# assertion duration of 2us in VID/FID change.
All Revs SP5100	PM_IO 0x89 = 0x10	This provides 16us delay before the assertion of LDTSTP# when C3 is entered. The delay will allow USB DMA to go on in a continuous manner.
All Revs SP5100	PM_IO 0x88 = 0x10	LdtStartTime = 10h for minimum LDTSTP# de-assertion duration of 16us in StutterMode. This is to guarantee that the HT link has been safely reconnected before it can be disconnected again. If C3 pop-up is enabled, the 16us also serves as the minimum idle time before LDTSTP# can be asserted again. This allows DMA to finish before the HT link is disconnected.
The following two registers should be programmed only if the following is true: *MTC1E is enabled but FID/VID is not enabled* **or** *MTC1E is enabled but FID/VID is not enabled*		
All Revs SP5100	PM_IO 0x9A [2] = 1	Enables pop-up for C3 For internal bus mastering or BmReq# from the NB, the SB will de-assert LDTSTP# (pop-up) to allow DMA traffic, then assert LDTSTP# again after some idle time.
	PM_IO 0x7C [0] = 1	Set this bit to 1 to allow wakeup from C3 if break event happens before LDTSTOP# assertion.

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PM_IO 0x7C [1] = 1	Set this bit to 1 to allow pop-up request being latched during the minimum LDTSTP# assertion time. Pop-up will happen thereafter even if the request has gone.
All Revs SP5100	PM_IO 0x61 [2] = 0	This bit should be cleared to 0 if C3 pop-up is enabled. If this bit is set to 1, the BmReq# input or internal bus mastering will set BM_STS.
All Revs SP5100	PM_IO 0x42 [2] = 0	If this bit is set to 1, the SB will convert C2 into C3, i.e. LVL2 read is treated the same as LVL3 read by hardware. This feature needs to be turned off because of the following reason. Some USB applications require continuous DMA transfer and are very sensitive to C3. The SB is configured to allow USB to set BM_STS and cause immediate exit from C3. When BM_STS is set the OS will issue C2 instead of C3. If C2 is converted into C3, the exit will not happen until the next interrupt because the OS does not set BM_RLD before issuing C2 and BM_STS is not considered a break event. Setting PM_IO 0x9A [4] = 1 can guarantee immediate exit in this case. But then the C2 to C3 conversion does not offer any power saving benefit. The feature is pending for future exploration.

Note: C3 pop-up is recommended for all systems.

Quick reference: Settings for dual-core system:
PM_IO 0x9A [5] = 1
PM_IO 0x9A [4] = 1
PM_IO 0x9A [2] = 1 (default)
PM_IO 0x8F [5] = 1 (default)
PM_IO 0x8F [4] = (1 for SP5100 + RS4x0 NB; 0 for SP5100 + RS690 NB)
PM_IO 0x8B = 0x01 (default)
PM_IO 0x8A = 0x90 (default)
PM_IO 0x88 = 0x06 (default)
PM_IO 0x7C [0] = 1 (default)
PM_IO 0x7C [1] = 1 (default)
PM_IO 0x61 [2] = 0 (default)
PM_IO 0x42 [2] = 0 (default)

Quick reference: Settings for single-core system:
PM_IO 0x9A [5] = 0
PM_IO 0x9A [4] = 0
PM_IO 0x9A [2] = 1 (default)
PM_IO 0x8F [5] = 1 (default)
PM_IO 0x8F [4] = (1 for SP5100 + RS4x0 NB; 0 for SP5100 + RS690 NB)
PM_IO 0x8B = 0x01 (default)
PM_IO 0x8A = 0x90 (default)
PM_IO 0x88 = 0x06 (default)
PM_IO 0x7C [0] = 1 (default)
PM_IO 0x7C [1] = 1 (default)
PM_IO 0x61 [2] = 0 (default)
PM_IO 0x42 [2] = 0 (default)

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		x						

2.5 Enable C1e Stutter Timer and Limit Link Disconnect to < 20 ms

ASIC Rev	Register Settings	Function/Comment
Stutter timer settings The following settings will program the stutter timer settings. There are two different values that need to be applied based on the condition listed below. Case 1 The following registers should be programmed only when Platform BIOS detects the CPUs listed below: • Family 10h with LS2 mode capability enabled: Model=6 && Stepping=2 II Model=(4I5|6) && Stepping >=3 || Model=(8|9) && Stepping >= 1 || Model Ah Case 2 Any CPU that does NOT meet the requirement in Case 1		
SP5100 Rev A14 and above	PM_IO 0xCB [5] =1	AutoStutterTimerEn. Set to 1 to enable.
	PM_IO_0XCB[6] =1	Auto Stutter Timer time base select. 1 = millisecond 0 = 2 microseconds (set to 1 to select millisecond increments)
	SMBUS PCI config 0x5C[7] = 1	Monitor C3 state if set to 1.
	Case 1 SMBUS PCI config 0x5C[22:16] = 14h	This register defines the timer value to trigger in 1 millisecond increments. (Set to 20 ms)
	Case 2 SMBUS PCI config 0x5C[22:16] = 10h	This register defines the timer value to trigger in 1 millisecond increments. (Set to 16 ms)
SMBUS PCI config 0x5C should be restored after resume from S3 and S4.		

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the SP5100 Register Reference Guide.
		x						
RTC	**ACPI**	**PM REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			
		x						

This part of logic borrows another function within SB to automatically stutter the C1e state when LDTSTOP# has been asserted continuously for a period of time defined by SmartVolt time. Originally this logic was for monitoring system activity, by setting AutoStutterTimerEn PMIO_CB[5], this logic becomes a timer to stutter the C1e.

2.6 MTC1e and FID VID Setting

ASIC Rev	Register Settings	Function/Comment
The following registers should be programmed only if FIDVID is enabled in conjunction with MTC1e		
SP5100 All Revs	PM_IO 0x9A [2] = 0	K8CpopUp is disabled
	PM_IO 0x7C 0] = 0	EnableBreak is disabled

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide.
RTC	ACPI	PM_REG	A-LINK	I/O REG	XIOAPIC			
		x						

2.7 C1e Exit on Assertion of IDLE Exit# (for A15 Only)

ASIC Rev	Register Settings	Function/Comment
The following registers should be programmed to support the C1e exit when Sp5100 IDLE_EXIT# is connected to BM_REQ# as break event		
SP5100 rev A15.	SMBUS PCI 0x64[5]=1	Enable BMREQ# pin to the C state logic
	PMIO_61[2]=1	Monitor BM_STS pin from NB and BM from SB
	PMIO_9A[4]=1	BM_STS cause SB to wakeup from C3
	PMIO_9A[5]=1	Clear BM_STS when system enters C3
	SMBUS PCI 0x64[4]=0	Force IDLE_EXIT# to set BM_STS and wakes from C3.
	SMBUS PCI 0x64[5]=1	
SMBUS PCI config 0x64 should be restored after resume from S3 and S4.		

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the SP5100 Register Reference Guide.
		x						
RTC	ACPI	PM_REG	A-LINK	I/O REG	XIOAPIC			
		x						

2.8 Support for Entering C1e on HALT# Message (for A15 Only)

ASIC Rev	Register Settings	Function/Comment
The following registers should be programmed to support the CE1e with HALT# message.		
SP5100 rev A15.	PMIO_BB[7]=1	Count HALT number and go into C3 automatically
	PMIO_C9[4]=1	Monitor number of HALT messages
	PMIO_C9[3:0]=1	number of HALTS to enter C1e

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the SP5100 Register Reference Guide.
		x						
RTC	ACPI	PM_REG	A-LINK	I/O REG	XIOAPIC			
		x						

2.9 Enabling Non-Posted Memory Write

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	AXINDC:0x10 [9] = 1	Enables non-posted memory write.

Programming Sequence:

```
OUT AB_INDX, 0x00000030    // Load AB_INDX with pointer to AX_INDXC
OUT AB_DATA, 0x00000010    // Write 0x10 to AX_INDXC
OUT AB_INDX, 0x00000034    // Load AB_INDX with pointer to AX_DATAC
IN  AB_DATA, TMP           // Read PCIE_CTL register (AXINDC:0x10)
OR TMP,      0x00000200    // Set bit 9
OUT AB_DATA, TMP           // Set PCIE_HT_NP_MEM_WRITE.
```

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

2.10 Therm Trip Settings

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PM_IO 0x68 [3]	0 = Disable the ThermTrip function on GEvent#2 pin. 1 = Enable the ThermTrip function on GEvent#2 pin.
	PM_IO 0x55 [0] = 1 (default)	With this bit set to 1, the ThermTrip function once activated will shutdown the system.
	PM_IO 0x67 [6:5]	These two bits are used to set the polarity of the ThermTrip and the TempCaut signals. Default = 00 (this means that the signals are active low).

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

2.11 Sx State Settings

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PM_IO 0x65 [7] = 0 (default)	Use 8us clock for delays in the S-state resume timing sequence.
	PM_IO 0x68 [2] = 1 (default)	Delay the APIC interrupt to the CPU until the system has fully resumed from the S-state.
Note: These 2 registers need to be set correctly for the S-state to work properly. Otherwise the system may hang during resume from the S-state.		

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

2.12 Output Drive Strength Settings

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Smbus_PCI_config 0xC0 [29:0] Setting TBD	These register bits configure the drive strength of each individual bus. Refer to the *AMD SP5100 Register Reference Guide*, SMBUS section describing the PCI config C0h for the recommended driving strength values.

Note: For more detail please refer to the *AMD SP5100 Register Reference Guide*.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
		X						
RTC	**ACPI**	**PM REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			

2.13 SUS_STAT# Enhancement

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PM_IO 0x7C[5]	1 = Enable SUS_STAT# enhancement. 0 = Disable SUS_STAT# enhancement. If enabled SUS_STAT# assertion will be extended until after the SB has fully resumed from the S3/4/5 state.

Note: This is a precautionary measure to suppress a glitch on the CKE pin for some early NB revisions on the P4 platform. Enable it only if the NB requires.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	**ACPI**	**PM REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			
		X						

2.14 Interrupt Routing/Filtering

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Smbus_PCI_config 0x62 [1:0]	The filtering for IRQ1 and IRQ12 should be enabled only when USB legacy support is enabled in internal USB host controller side.
	Smbus_PCI_config 0x67 [7]	The bit should be set to 1 only when USB legacy support is enabled in internal USB host controller side.. By setting to 1 IRQ1/IRQ12 to PIC and IoApic controller comes from USB legacy block.
	Smbus_PCI_config 0x64 [13] = 1	Delay back to back interrupts to the CPU. The hardware will delay an interrupt for approximately 500ns if there is a pending interrupt. Some applications in PIC mode may not be able to handle back to back interrupts in a short time period. Enabling this bit will prevent the application from encountering back to back interrupts.
	USB HC(bus0, dev 18, fun 0) MMio+160h	Set to 0000_0000h when USB legacy support is disabled in internal USB host controller side. SW has to make sure that the USB Hc memory decoding is enabled in PCIi configuration space command register.

All Revs SP5100	USB HC(bus0, dev 19, fun 0) MMio+160h	Set to 0000_0000h when USB legacy support is disabled in internal USB host controller side. SW has to make sure that the USB Hc memory decoding is enabled in PCI configuration space command register.
	USB HC(bus0, dev 20, fun 5) MMio+160h	Set to 0000_0000h when USB legacy support is disabled in internal USB host controller side. SW has to make sure that the USB Hc memory decoding is enabled in PCI configuration space command register

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
	X	X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

2.15 IO Trap Settings

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PM_IO 0x14 ~ 0x1B, 0xA0 ~ 0xA7	Programmable address ranges for IO trap.
	PM_IO 0x1C ~ 0x1D, 0xA8 ~ 0xA9	IO trap enable/status registers.
	1. ABCFG 0x10090 [16] = 1 2. PM_IO 0x14 ~ 0x1D or 0xA0 ~ 0xA9	ABCFG 0x10090 [16] = 1 ensures the SMI# message to be sent before the IO command is completed.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X	X					

2.16 Enabling ACPI Registers

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	1. Assign the IO base address for the following ACPI registers: - AcpiPm1EvtBlk = PM_IO 0x20, 0x21 - AcpiPm1CntBlk = PM_IO 0x22, 0x23 - AcpiPmTmrBlk = PM_IO 0x24, 0x25 - CpuControl = PM_IO 0x26, 0x27 - AcpiGpe0Blk = PM_IO 0x28, 0x29 - AcpiSmiCmd = PM_IO 0x2A, 0x2B - AcpiPmaCntBlk = PM_IO 0x2C, 0x2D 2. Set AcpiDecodeEnable - PM_IO 0x0E[3] = 1	The BIOS needs to assign the IO base address for each of the ACPI registers before enabling the ACPI decode. The IO base addresses are defined in PM_IO 0x20 ~ 0x2F registers. Note 1: The PM_IO 0x20 ~ 0x2F registers are undefined upon the first system power up and may therefore contain random values. If the BIOS enables the ACPI decode without assigning the proper IO base addresses for the ACPI registers, the SB may decode incorrect IO addresses and cause unexpected system behavior. Note 2: The PM_IO 0x2E/2F registers must be programmed with a valid I/O address. The recommended address is using the AcpiSmiCmd + 8. Leaving this register to a default of 0 will cause a conflict with legacy DMA.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

2.17 Legacy DMA Prefetch Enhancement

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Smbus_PCI_config 0x43 [0] = 1 (only when the system is non-DOS mode)	Enables legacy DMA prefetch enhancement for channel 0, 1, 2, and 3. This bit should be set to improve DMA out (eg memory-to-floppy disk) performance. Note: This bit should only be enabled in the ACPI method (called by the OS). This ensures that it is enabled only when the system is in Window mode. Under DOS mode, this feature may not work properly and may cause the floppy to malfunction.
	Smbus_PCI_config 0x41 [7] = 1 Lpc_PCI_config 0x78 [0] = 0	Set these bits to make LPC DMA work properly.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

2.18 USB Set BM_STS

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PM_IO 0x66 [6] = 0	For balanced power saving and USB performance, allow USB DMA to cause pop-up. Other register settings for C state should be followed for the system to work properly.

Note: Refer to USB register settings section for the corresponding USB register settings that are required to be programmed when the above registers are programmed. For the AMD platform, PM_IO 0x66 [6], and register settings in the USB register settings section should be programmed.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		x						

2.19 Enabling Spread Spectrum

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PM_IO 0x42 [7] = 1	Enables spread spectrum on PCI clocks with -0.5% spread. In external clock mode, the internal SS when enabled will down spread the PCI clocks. The 100 MHz PCIe® clock SB_SRC from the external clock generator should not have spread spectrum enabled if the internal spread is enabled. Refer to PA_SP5100AGx for more information on enabling the spread spectrum.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		x						

2.20 PCIe® Native Mode

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PM_IO 0x55 [3]	Set to 1 to enable PCIe® native mode. If PCIe is in Native mode: set the bit to 1. If PCIe is not in Native mode: set the bit to 0.
	PM_IO 0x10 [6]	Set to 1 to make PCIE_WAK_DIS visible in ACPI Pm1a register group. If PCIe is in Native mode: set the bit to 1. If PCIe is not in Native mode: set the bit to 0.
	PM_IO 0x55 [4]	Set to 0 to enable PCIE_WAK_DIS/PCIE_WAK_STS function. If PCIe is in Native mode: set the bit to 0. If PCIe is not in Native mode: set the bit to 1.
	PM_IO 0x55 [5] = 1	Set to 1 to force the non-generation of SCI when seeing PCIe wake event. Set the bit to 1 all the time.
	PM_IO 0x84 [0] = 0 PM_IO 0x84 [1] = 0	Generate SCI interrupt in PCIe legacy mode when wake# is asserted.
	PM_IO 0xD7 [6] = 1	Mask off the input of PCIE_Wak_Sts if PCIE_WAK_DIS is 1. Set the bit to 1 all the time.
	PM_IO 0xD7 [1] = 1	Routes PME_message from NB to the input of PCIE_Wak_Sts. Set the bit to 1 all the time.

Suggested settings:

	WinXP	Vista (Legacy mode)	Vista (Native mode)
PM_IO 0x55[3]	0	0	1
PM_IO 0x10[6]	0	1	1
PM_IO 0x55[4]	1	0	0
PM_IO 0x55[5]	1	1	1
PM_IO 0x84[0]	1	1	1
PM_IO 0x84[1]	0	0	0
PM_IO 0xD7[6]	1	1	1
PM_IO 0xD7[7]	1	1	1

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

2.21 Hardware Monitor

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PM_IO 0xD7 [7] = 7	Set only if Hardware monitor is used for temperature reading

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

2.22 Cir Interrupt Config

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Smbus_PCI_config 0xE1[6]	Set to 1 to treat Cir interrupt as level signal; otherwise it is edge.trigger:

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

2.23 SMBUS PCI Config

ASIC Rev	Register Settings	Function/Comment
A11 and A12	Smbus_PCI_config 0xE1[0] = 1	Forces Smbus controller to be enabled all the time, even if Io/Mem decoding bit is set to 0.
A11 and A12	Smbus_PCI_config 0xE1[1]	Mmio decoding required setting
All Revs SP5100	Smbus_PCI_config 0xE1[2]	Set to 1 to enable Io port 60h read/write SMi trapping and Io port 64h write Smi trapping.
	Smbus_PCI_config 0xE1[3] = 1	Required for INTA message decoding.
	Smbus_PCI_config 0xE1[4] = 1	Smbus0 busy bit enhancement

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

2.24 IMC Access Control

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Smbus_PCI_config 0xE1[7] = 1 Smbus_PCI_config 0xAF[1] = 0	Required for proper function of the IMC shared access.
	The following register should only be programmed if IMC is enabled	
	Smbus_PCI_config 0xE1[5] = 1	Required for proper function of the IMC shared access.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

2.25 CPU Reset

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PM_IO 0xB2[2] = 1	Enables the CPU Reset timing option defined in PM register D5[1:0]. Required only if the default timing needs to be changed.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

2.26 Disabling Legacy USB Fast SMI#

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Smbus_PCI_config 0x62 [5] = 1	Legacy USB can request SMI# to be sent out early before IO completion. Some applications may have problems with this feature. The BIOS should set this bit to 1 to disable the feature.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
		x						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

2.27 SMBUS1 Programming Sequence

ASF SMBUS 1 interface incorporates ASF and SMBUS1 controllers. ASF features (capability of using ACPI services by ASF master) are not supported on SP5100. However, the SMBUS1 controller can be used as a generic SMBUS interface with SMBUS1 controller operating as master to communicate to SMBUS slave devices that need to be on S5 power domain. The ASF slave controller in SP5100 is disabled but some registers belonging to ASF controller will need to be programmed to support SMBUS1 controller in Master mode.

- Step 1: Set the base address of ASF IO space by programming bits [15:4] of Sm cfg space reg 58h:

ASFSMbusIoBase- RW - 16 bits - [PCI_Reg: 58h]			
Field Name	**Bits**	**Default**	**Description**
ASFSMBusEnable	0	0h	0: Disable ASF controller 1: Enable ASF controller
Reserved	3:1	000b	
ASFSMBase	15:4	FFFh	ASF SM bus controller Io base address

- Step 2: Enable the ASF controller by programming bit[0] of Sm cfg space reg 58h:

ASFSMbusIoBase- RW - 16 bits - [PCI_Reg: 58h]			
Field Name	**Bits**	**Default**	**Description**
ASFSMBusEnable	0	0h	0: Disable ASF controller 1: Enable ASF controller

ASFSMbusIoBase- RW - 16 bits - [PCI_Reg: 58h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:1	000b	
ASFSMBase	15:4	FFFh	ASF SM bus controller Io base address

- Step 3: Disable Legacy Sensor support by programming bit[6] of ASF I/O 0Dh to 1

SlaveMisc- RW - 8 bits - [ASF_IO: 0Dh]			
Field Name	**Bits**	**Default**	**Description**
SlavePECError	0	0b	RO 0: No PEC error 1: PEC error
SlaveBusCollision	1	0b	RO 0: No BusCollision 1: BusCollision happens
SlaveDevError	2	0b	RO 0: Expected response 1: Unexpected response
WrongSP	3	0b	RO 0: No SP error 1: No SP when turn to read
Reserved	4	0b	
SuspendSlave	5	0b	RW Write 1 to Suspend (stop) ASF Slave state machine
KillSlave	6	0b	RW Write 1 to reset Slave ASF Slave state machine
LegacySensorEn	7	0b	RW 0: Disable Legacy Sensor 1: Enable Legacy Sensor

- Step 4: Enable PEC if SMBUS device supports PEC:

HostControl – RW - 8 bits - [ASF_IO: 02h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	
KillHost	1	0b	0: Enable SM master 1: Reset SM master
Protocol	4:2	000b	000: Quick 001: Byte 010: Byte Data 011: Word Data 100: Process call 101: Block
PECAppend	5	0b	0: No PEC append 1: Automatic PEC append. ASF HC calculates CRC code and append to the tail of the data packets.
Start	6	0b	WO: 0: Always read 0 on reads 1: Writing 1 to initiate the command
PECEnable	7	0b	0: PEC disable 1: PEC enable, enable CRC checking when ASF HC presents as SM master and SM slave.

2.28 ACPI System Clock Setting

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PMIO 0x53 [6] = 1	Enables the internally generated 14.318Mhz clock to the ACPI logic.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		x						

2.29 Integrated Pull-up and Pull-down Settings

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PMIO2_F3, PMIO2_F4, PMIO2_F5, PMIO2_F6, PMIO2_F7, PMIO2_F8	The BIOS needs to set pull-up/down settings for GEVENT/GPM platform specifically. These pins have integrated pull-up/down enabled by default and they are powered by the S5 power. If they are to be connected to a device that will be powered down during sleep state, the BIOS should disable the pull-up/down and use external pull-up/down to avoid leakage.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM2 REG	A-LINK	I/O REG	XIOAPIC			
		x						

2.30 Revision ID

ASIC Rev	Register Settings	Function/Comment
SP5100 A12	Smbus_PCI_config 0x08 PMIO_53[6] Smbus_PCI_config 0x40 [0] Notes: A12 revision ID – 0x3A. Smbus PCI config space 0x08 will show 3Ah after BIOS is initialized.	In order to determine and set the correct revision ID for SP5100, BIOS needs to perform the following sequence: (1) During early post, read Smbus_PCI_config 0x08 and PMIO_53[6] to determine if the ASIC is A11 or A12. The ASIC is A11 if the return values are 39h and 0b respectively. If Smbus_PCI_config 0x08 returns 3Ah, or Smbus_PCI_config 0x08 is 39h and PMIO_53[6] is 1b, then the ASIC is A12. (2) If Smbus_PCI_config 0x08 is 39h and PMIO_53[6] is 1b, BIOS should write to Smbus_PCI_config, 0x40[0] = 1, follow by writing to Smbus_PCI_config, 0x08 with a value of 3Ah. Afterward, BIOS should clear Smbus_PCI_config, 0x40[0] back to 0.
SP5100 A14	Smbus_PCI_Config 0x08	This register will show 0x3C as revision ID for SP5100 A14.
SP5100 A15	Smbus_PCI_Config 0x08	This register will show 0x3D as revision ID for SP5100 A15.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
		x						
RTC	ACPI	PM_REG	A-LINK	I/O REG	XIOAPIC			
		x						

2.31 Alternate Pin for 14 MHz Clock Input

ASIC Rev	Register Settings	Function/Comment
The following change is required for SP5100 revision A14 and above and if the 14 MHz clock is connected to the SB on to 25M_48M_66M_OSC. This reference clock is required to resolve the revision A12 Errata item #5 in hardware instead of using the BIOS workaround. If external 14 MHz clock is not used on SP5100 rev A14 and above, then the BIOS workaround described in erratum #5 should be implemented.		
SP5100 A14 and above	PMIO 0xD4[6] = 1	Program this register to '1' if the system supports 14.318 MHz reference clock connected to 25M_48M_66M_OSC. This reference clock is required to resolve the revision A12 Errata item #5 in hardware instead of using the BIOS workaround. This register bit is not supported on A12 and should not be programmed by the BIOS.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the ***SP5100 Register Reference Guide.***
RTC	ACPI	PM_REG	A-LINK	I/O REG	XIOAPIC			
		x						

2.32 Gevent5 as GPIO

ASIC Rev	Register Settings	Function/Comment
SP5100 A14 and above	PMIO 0xD7[2] = 1	This bit should be programmed if the Gevent5 needs to be used as for GPIO function on revision A14. Revision A12 does not support GPIO function on the GEVENT pin. Programming this register for A14 will make this pin on A14 function as GPIO. (Note that the GEVENT pin still needs to be programmed for GPIO as any other pins. The programming of this bit is in addition to the normal programming procedure of GPIO/ GEVENT pins.) If this bit is cleared, the function of this pin is same as in revision A12. The power up default of this bit is '0'. 0 (default) : Disable 1 : Enable This register bit is not supported on A12 and should not be programmed by the BIOS for A12.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the ***SP5100 Register Reference Guide.***
RTC	ACPI	PM_REG	A-LINK	I/O REG	XIOAPIC			
		x						

These registers should be programmed by Platform System BIOS if Gevent5 functionality is required.

2.33 SMBUS Block Write Filtering

ASIC Rev	Register Settings	Function/Comment
SP5100 A14 and above	Smbus_PCI_config 0x38 [7]=0	Enable SMBUS filtering circuit. Setting this bit to 0 to enable SMBUS filtering (1194). THIS FEATURE WILL RESOLVE THE ISSUE DESCRIBED IN REVISION A12 ERRATA ITEM # 13.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the ***SP5100 Register Reference Guide.***
		x						
RTC	**ACPI**	**PM_REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			

2.34 SMBUS Sequence

The following programming sequence should be followed when reading or writing to the SMBUS 0:

1. read HostBusy bit
2. if not zero
   if time out (recommended time out == 1ms or greater)
   set kill bit
   go back step 1.
   else
   go to step 3
3. read SlaveBusy
4. if not zero
   if time out
   set reset bit
   go back step 3.
   else
   go to step 5
5. clear HostStatus register, program Slave Address register/Command register/ Data0/Data1/Data
6. read HostControl register
7. write HostControl register to start the transaction.
8. wait HostBusy bit to be 1
9. wait HostBusy bit to be 0
10. wait one SMBUS clock period.
11. wait HostBusy bit to 0.

2.35 Software Clock Throttle Period

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PMIO 0x68[7:6] = 10	Set AcpiThrotPeriod field in MiscEnable68 to 244 µS (Hardware default is set to 15 µS)

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the *SP5100 Register Reference Guide.*
RTC	ACPI	PM_REG	A-LINK	I/O REG	XIOAPIC			
		X						

2.36 Unconditional Shutdown

ASIC Rev	Register Settings	Function/Comment
SP5100 A15	Smbus_PCI_config 0x38[12] = 1	Enable the enhancement for unconditional shutdown Set sm cfg 43 bit 3 to 0 first before programming this bit, then set 43h bit 3 back to 1 after programming.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the *SP5100 Register Reference Guide.*
		x						
RTC	ACPI	PM_REG	A-LINK	I/O REG	XIOAPIC			

2.37 Watchdog Timer Resolution

The register below should be programmed by SW before WDT is programmed.

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PMIO 0x69[0] = 0 PMIO 0x69[2:1] = 01	Enable WDT function (0: Enable; 1: Disable) 00: Set resolution for 32 us 01: Set resolution for 10ms 10: Set resolution for 100ms 11: Set resolution for 1s 10ms resolution is recommended.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the *SP5100 Register Reference Guide.*
RTC	ACPI	PM_REG	A-LINK	I/O REG	XIOAPIC			
		x						

2.38 Supporting IDLE_EXIT# from CPU

ASIC Rev	Register Settings	Function/Comment
The following register should be programmed to support IDLE_EXIT# from CPU to wake C1e state		
SP5100 revision A14 and above	SMBUS PCI 0x64[5]=1 PMIO 0x61[2]=1 PMIO_0x9A[5:4]=11	Enable BM_STS# pin Enable BM_STS# to break C1e Enable automatic BM_STS clearing upon C1e entry

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the *SP5100 Register Reference Guide.*
		x						
RTC	**ACPI**	**PM_REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			
		x						

This part of logic borrows the existing legacy ACPI BM_STS and BM_RLD bits as a mechanism to break out from C1e under a non-OS controlled C3 state. Under this scheme, the logic will automatically clears the BM_STS bit whenever it enters C1e state. Whenever BM_REQ#/IDLE_EXIT# is detected, it will cause the BM_STS bit to be set and thereby causing the C state logic to exit. BIOS should clear the BM_STS bit on every post.

2.39 Supporting HALT Message to Generate C1e

ASIC Rev	Register Settings	Function/Comment
The following register should be programmed to support HALT message to C1e function		
SP5100 A14 and above	PMIO 0xBB[7]=1 PMIO_0xC9[4]=1 PMIO 0xC9[3:0] = Number of Halt Enter messages to trigger C1e	Enable HALT message to C1e function Enable counting of HALT message Setting number of HALT messages to generate C1e

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the *SP5100 Register Reference Guide.*
RTC	**ACPI**	**PM_REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			
		x						

This part of logic basically counts the number of HALT_ENTER messages. When it has received the number of HALT_ENTER messages equal to NumOfHalt (PMIO_C9[3:0]), it will generate an internal C1e command to the C state logic.
This count will increment when it sees HALT_ENTER and decrement when it sees HALT_EXIT. If it receives a HALT_EXIT message after it has generated the C1e command, it will treat the HALT_EXIT as a break event.

2.40 LDT_PWRGD De-assertion with SLP_S3#

ASIC Rev	Register Settings	Function/Comment
SP5100 A15	Smbus_PCI_config 0x41 [3]=1	Set this bit to 1 to force LDT_PWRGD to be de-asserted at the same time as SLP_S3#.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the ***SP5100 Register Reference Guide.***
		x						
RTC	**ACPI**	**PM_REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			

2.41 Programmable Interrupt Controller Arbitration

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Smbus_PCI_config 0xAE [6]=1	Set this bit to 1 to allow the arbiter proper operation in cases where both the PIC and APIC are enabled.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the ***SP5100 Register Reference Guide.***
		x						
RTC	**ACPI**	**PM_REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			

2.42 HPET MSI Setting

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Smbus_PCI_config 0x40 [31:29]= 000b	Program these register bits ONLY if the following are true in the platform configuration: 1. Legacy Floppy Drive interface supported 2. Legacy FIR device supported

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the ***SP5100 Register Reference Guide.***
		x						
RTC	**ACPI**	**PM_REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			

2.43 SMAF Matching Setting

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Smbus_PCI_config 0x60 [22] = 1b	This bit is required to be set to cover a corner case of concurrent throttling and C1e

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the *SP5100 Register Reference Guide.*
		x						
RTC	**ACPI**	**PM_REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			

3 LPC Controller (bus-0, dev-20, fun-3)

3.1 IO / Mem Decoding

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Lpc_PCI_config 0xBB[7] = 1 Lpc_PCI_config 0xBB[6] = 1 Lpc_PCI_config 0xBB[3] = 1	These bits are required to be set for LPC PCI slave interface.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
						X		
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

3.2 SPI Bus

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Lpc_PCI_config 0xBB[5] = 1	Set to 1 to allow SPI Op code to execute even though it is now strapped as LPC Rom. Some BIOS code may want to send SPI opcodes to check if SMI Rom is present. If the system configuration is set for LPC, then the SPI opcode will not be passed to SPI if this bit is not set.
	Spi_mmio 0x00[28] = 1	Allows the software to read the status number of the SPI read cycles completed – 1. Eliminates the last count.
	Lpc_PCI_config 0xBB[0] = 1	Set to 1 to improve SPI read performance. The bit should be set after programming the I/O modes and SPI speed.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
						X		
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

4 A-Link Express Settings - Indirect I/O Access

4.1 Defining AB_REG_BAR

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Smbus_PCI_config 0xF0 [31:0] = AB_REG_BAR	Defines the AB I/O base address. Refer to *AMD SP5100 Register Reference Guide, chapter 4: A-Link Express/A-Link Bridge Registers* for more information.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
		X						
RTC	**ACPI**	**PM REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			

4.2 Clearing AB_INDX

The programming procedure for the ABCFG registers, as specified in the register reference guide, is to first load AB_INDX with a register's RegSpace and RegAddr; and then access the specified register through AB_DATA. The example below demonstrates how to read ABCFG:10058h:

```
OUT AB_INDX, 0xC0010058    // Set AB_INDX RegSpace=11 RegAddr=0x10058
IN  AB_DATA, TMP
```

For certain revisions of the chip, the ABCFG registers, with an address of 0x100NN (where 'N' is any hexadecimal number), require an extra programming step. This required step is defined in the following table:

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	AB_INDX = 0x00000000	Clears AB_INDX after reading or writing an ABCFG register with an address 0x100NN.

Example Programming Sequence:

```
OUT AB_INDX, 0xC00100NN    // Load AB_INDX with pointer to ABCFG:0x100NN
IN  AB_DATA, TMP           // Read ABCFG 0x100NN
OUT AB_INDX, 0x00000000    // Clear AB_INDX
```

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	**ACPI**	**PM REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			
			X					

4.3 Enabling Upstream DMA Access

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	AXCFG: 0x04 [2] = 1	Enables the SP5100 to issue memory read/write requests in the upstream direction.

Programming Sequence:

```
OUT AB_INDX, 0x80000004    // Load AB_INDX with pointer to AXCFG:0x04
IN  AB_DATA, TMP           // Read COMMAND register (AXCFG:0x04)
OR  TMP,     0x00000004    // Set bit 4
OUT AB_DATA, TMP           // Set BUS_MASTER_EN
```

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	**ACPI**	**PM REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			
			X					

4.4 IDE/PCIB Prefetch Settings

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	IDE prefetch ABCFG 0x10060 [17] = 1 ABCFG 0x10064 [17] = 1 PCIB prefetch ABCFG 0x10060 [20] = 1 ABCFG 0x10064 [20] = 1	The settings on AB control the IDE and PCIB prefetch. For all revisions the pre-fetch needs to be enabled for performance enhancement.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	**ACPI**	**PM REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			
			X					

4.5 OHCI Prefetch Settings

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	ABCFG 0x80 [0] = 1	This register in AB controls the USB OHCI controller prefetch used for enhancing performance of ISO out devices.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	**ACPI**	**PM REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			
			X					

4.6 B-Link Client's Credit Variable Settings for the Downstream Arbitration Equation

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	ABCFG 0x9C [0] = 1	Disables the credit variable in the downstream arbitration equation.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

4.7 Enabling Additional Address Bits Checking in Downstream Register Programming

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	ABCFG 0x9C [1] = 1	Register bit to qualify additional address bits into downstream register programming.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

4.8 Set B-Link Prefetch Mode

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	ABCFG 0x80 [17] = 1 ABCFG 0x80 [18] = 1	Sets B-Link prefetch mode.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

4.9 Enabling Detection of Upstream Interrupts

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	ABCFG 0x94 [20] = 1 ABCFG 0x94 [19:0] = CPU interrupt delivery address [39:20].	Enables A-Link Express logic to detect upstream interrupts for the purposes of system management.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

4.10 Enabling Downstream Posted Transactions to Pass Non-Posted Transactions

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	ABCFG 0x10090 [8] = 1	Enables downstream posted transactions to pass non-posted transactions.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

4.11 Programming Cycle Delay for AB and BIF Clock Gating

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	ABCFG 0x54 [23:16] = 0x4 ABCFG 0x10054 [23:16] = 0x4 ABCFG 0x98 [15:12] = 0x4	Program # of cycles to delay before gating AB and BIF clocks after idle condition.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

4.12 Enabling AB and BIF Clock Gating

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	ABCFG 0x54[24] = 0 ABCFG 0x10054[24] = 1 ABCFG 0x98[11:8] = 0x7	Enables the AB and BIF clock-gating logic.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

4.13 Enabling AB Int_Arbiter Enhancement

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	ABCFG 0x10054[15:0] = 0x07FF	Enables the A-Link int_arbiter enhancement to allow A-Link bandwidth to be used more efficiently

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

4.14 Enabling Requester ID

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	ABCFG 0x98[16] = 1	Enables the requester ID for upstream traffic

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

4.15 Selecting the LPC FRAME# Assertion Timing on Power-up

ASIC Rev	Register Settings	Function/Comment
SP5100 A14 and above	Lpc_PCI_config 0x8C [17] = 0	Set the bit to 0 for revision A14 to assert LFRAME# signals on SB Power good assertion. Setting the bit to 1 will configure LPC to assert the LFRAME# signal on de-assertion of SLP_S3# signal on power up. This register bit is not supported on A12 and should not be programmed by the BIOS.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the ***SP5100 Register Reference Guide.***
						x		
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

4.16 SMI IO Write

ASIC Rev	Register Settings	Function/Comment
SP5100 A12	ABCFG 0x9C[8] = 1	IO write and SMI ordering enhancement enabled
SP5100 A14 and above	ABCFG 0x9C[8] = 0	IO write and SMI ordering enhancement disabled
SP5100 A15	ABCFG 0x90[21] = 1 ABCFG 0x9C[5] = 1 ABCFG 0x9C[9] = 1 ABCFG 0x9C[15] = 1	SMI ordering enhancement enabled

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

4.17 Reset CPU on Sync Flood

ASIC Rev	Register Settings	Function/Comment
SP5100 All Revs	ABCFG 0x10050[2] = 1	Enable SP5100 to initiate a CPU Reset on sync_flood. This bit should be enabled in very early post.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the *SP5100 Register Reference Guide.*
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

4.18 Enabling Posted Pass Non-Posted Downstream

ASIC Rev	Register Settings	Function/Comment
SP5100 A15	AX_INDXC 0x2[9] = 1 ABCFG 0x9C[6] = 1 ABCFG 0x9C[7] = 1 ABCFG 0x9C[10] = 1 ABCFG 0x9C[11] = 1 ABCFG 0x9C[12] = 1 ABCFG 0x9C[13] = 1 ABCFG 0x9C[14] = 1 ABCFG 0x1009C [4] = 1 ABCFG 0x1009C [5] = 1 ABCFG 0x10090 [9] = 1 ABCFG 0x10090 [10] = 1 ABCFG 0x10090 [11] = 1 ABCFG 0x10090 [12] = 1	Posted pass non-posted downstream direction feature enable.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the *SP5100 Register Reference Guide.*
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

4.19 Enabling Posted Pass Non-Posted Upstream

ASIC Rev	Register Settings	Function/Comment
SP5100 A15	ABCFG 0x58[11] = 1 ABCFG 0x58[15:12] = 0xE	Posted pass non-posted upstream direction feature enable.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the *SP5100 Register Reference Guide.*
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

4.20 64 bit Non-Posted Memory Write Support

ASIC Rev	Register Settings	Function/Comment
SP5100 A15	AX_INDXC 0x2[10] = 1	Enable support of 64-bit Non-Posted Memory Writes.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the *S SP5100 Register Reference Guide.*
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

5 PCIB (PCI-bridge, bus-0, dev-20, fun-04)

5.1 Enabling PCI-bridge Subtractive Decode

ASIC REV	Register Settings	Function/Comment
All Revs SP5100	PCIB_PCI_config 0x40 [5] = 1 PCIB_PCI_config 0x4B [7]= 1	Enables the PCI-bridge subtractive decode. This setting is strongly recommended since it supports some legacy PCI add-on cards.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.2 PCI-bridge Upstream Dual Address Window

ASIC REV	Register Settings	Function/Comment
All Revs SP5100	PCIB_PCI_config 0x50 [0] = 1	PCI-bridge upstream dual address window. This setting is applicable if the system memory is more than 4GB, and the PCI devices can support dual address access.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.3 PCI Bus 64-byte DMA Read Access

ASIC REV	Register Settings	Function/Comment
All Revs SP5100	PCIB_PCI_config 0x4B [4] = 1 (default)	PCI bus 64-byte DMA read access. Enhances the PCI bus DMA performance.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.4 PCI Bus DMA Write Cacheline Alignment

ASIC REV	Register Settings	Function/Comment
All Revs SP5100	PCIB_PCI_config 0x40 [1] = 1 (default)	Enables the PCIB writes to be cacheline aligned. The size of the writes will be set in the Cacheline Register (PCIB_PCI_config 0x4B[4:0]). Refer to section *5.3* for more information.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.5 Master Latency Timer

ASIC REV	Register Settings	Function/Comment
All Revs SP5100	PCIB_PCI_config 0x0D = 0x40 (default) PCIB_PCI_config 0x1B = 0x40 (default)	Enables the PCIB to retain ownership of the bus on the Primary side and on the Secondary side when GNT# is de-asserted. Note: This setting is mandatory.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.6 DMA Read Command Match

ASIC REV	Register Settings	Function/Comment
All Revs SP5100	PCIB_PCI_config 0x4B[6] = 1 (default)	Enables the command matching checking function on "Memory Read" & "Memory Read Line" commands. Some PCI devices may change the "Memory read command" to "Memory read line" command before the data is completed. This bit enables the command matching checking inside the PCIB to work with this kind of device. Note: This setting is mandatory.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.7 Enabling Idle To Gnt# Check

ASIC REV	Register Settings	Function/Comment
All Revs SP5100	PCIB_PCI_config 0x4B [0] = 1 (default)	When enabled, the PCI arbiter checks for the Bus Idle before asserting GNT#. Note: This setting is recommended.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.8 GNT# Timing Adjustment

ASIC REV	Register Settings	Function/Comment
All Revs SP5100	PCIB_PCI_config 0x64 [12] = 1 (default)	Adjusts the GNT# de-assertion time. Note: This setting is recommended.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.9 Enabling Fast Back to Back Retry

ASIC REV	Register Settings	Function/Comment
All Revs SP5100	PCIB_PCI_config 0x48 [2] = 1 (default)	Enables Fast Back to Back transactions support. Note: This setting is recommended

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.10 Enabling Lock Operation

ASIC REV	Register Settings	Function/Comment
All Revs SP5100	PCIB_PCI_config 0x48 [3] = 1 (default)	This bit should be set to 1 when PCI configuration space PCIB_PCI config 0x40 [2] = 1 for the proper operation of the PCI LOCK# function.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.11 Enabling Additional Optional PCI Clock (PCICLK5)

ASIC REV	Register Settings	Function/Comment
All Revs SP5100	PCIB_PCI_config 0x64 [8] = 1	This only applies when PCICLK5/PCIREQ5#/PCIGNT5# are enabled: When this bit is set, PCICLK5, PCIREQ#5, and PCIGNT5# are enabled for PCI use. Since PCICLK5 is not enabled by default (the clock is off), the PCI device which uses this clock may not see the system reset during power-up. To correct this, the BIOS should write to PCIB config 3Eh, bit [6] to assert the additional PCI reset so the device will see a proper reset, as well as to provide the time for its internal PLL to lock. The recommended duration time is at least a few milliseconds. Note: These three pins are enabled as a group, therefore, care should be taken to make sure they are used properly.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.12 Enabling One-Prefetch-Channel Mode

ASIC REV	Register Settings	Function/Comment
All Revs SP5100	PCIB_PCI_config 0x64 [20] = 0x1	Enables One-Prefetch-Channel Mode. Note: This setting is mandatory.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.13 Disabling PCIB MSI Capability

ASIC REV	Register Settings	Function/Comment
All Revs SP5100	PCIB_PCI_config 0x40 [3] = 0x0 (default)	Disables MSI capability.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.14 Adjusting CLKRUN#

ASIC REV	Register Settings	Function/Comment
All Revs SP5100	PCIB_PCI_config 0x64 [15] = 0x1	This bit should be set to 1 for the proper operation of CLKRUN#. Note: This setting is mandatory.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6 USB – OHCI & EHCI controllers (bus-0, dev-18/19, fun-00 ~02/ bus-0, dev-20, fun-05)

Please note the following information for this section:

- EHCI BAR address = EHCI_PCI_config 0x10[31:8]
- EHCI_EOR is the EHCI operation register = EHCI_BAR + 0x20
- The device list for all USB Controllers is as follows:

Device List	Function/Comment
Bus-0, dev-18, fun-0	USB1, OHCI0
Bus-0, dev-18, fun-1	USB1, OHCI1
Bus-0, dev-18, fun-1	USB1, EHCI
Bus-0, dev-19, fun-0	USB2, OHCI0
Bus-0, dev-19, fun-1	USB2, OHCI1
Bus-0, dev-19, fun-1	USB2, EHCI
Bus-0, dev-20, fun-5	USB3, OHCI

6.1 Enabling/Disabling OHCI and EHCI Controllers

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Smbus_PCI_config 0x68 [2] = 1 (default)	Enables the USB1 (bus-0, dev-18) EHCI controller.
	Smbus_PCI_config 0x68 [0] = 1 (default)	Enables the USB1 (bus-0, dev-18) OHCI controller 1 (OHCI0).
	Smbus_PCI_config 0x68 [1] = 1 (default)	Enables the USB1 (bus-0, dev-18) OHCI controller 2 (OHCI1).
	Smbus_PCI_config 0x68 [6] = 1 (default)	Enables the USB2 (bus-0, dev-19) EHCI controller.
	Smbus_PCI_config 0x68 [4] = 1 (default)	Enables the USB2 (bus-0, dev-19) OHCI controller 1 (OHCI0).
	Smbus_PCI_config 0x68 [5] = 1 (default)	Enables the USB2 (bus-0, dev-19) OHCI controller 2 (OHCI1).
	Smbus_PCI_config 0x68 [7] = 1 (default)	Enables the USB3 (bus-0, dev-20, fun-5) OHCI controller.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	**For register details, refer to the sections check-marked in the *SP5100 Register Reference Guide.***
		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.2 USB Device Support to Wake Up System from S3/S4 State

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PM_IO 0x61 [6] = 1 PM_IO 0x65 [2] = 1 (default)	Enables the USB PME event. Enables USB resume support.
	PM_IO 0x65 [6] = 1	Enable PME generation for USB Wake event from connect and disconnect of USB devices. Note: BIOS workaround A2 described in Appendix A must be implemented for this feature to work reliably. Without the workaround PME Wake for Connect/Disconnect of USB 1.1 devices will not be supported.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

6.3 USB S4/S5 Wakeup or PHY Power Down Support

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PM_IO 0x65 [0] = 0 (default)	This bit = 0 (default) supports USB device wakeup from the S4/S5 state. Set the bit to 1 to disable the USB S4/S5 wakeup function. The analog power supply to USB PHY on the motherboard can be OFF in this case to save S4/S5 power.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

6.4 USB PHY Auto Calibration Setting

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	EHCI_BAR 0xC0 = 0x00020F00	Enables the USB PHY auto calibration resistor to match 45ohm resistance.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.5 USB Reset Sequence

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PM_IO 0x65 [4] = 1	Enables the USB controller to get reset by any software that generates a PCIRst# condition. However, this bit should be cleared before a software generated reset condition occurs during S3 resume so the USB controller will not lose the connection status during the S3 resume procedure. The software generated PCIRst# conditions include Keyboard Reset, or write to the IO-CF9 register.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

6.6 USB Advanced Sleep Control

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PM_IO 0x95 [2:0] = 110b	Enables the USB EHCI controller advance sleep mode function to improve power saving.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

6.7 USB 48 MHz Clock Source Settings

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PM_IO 0xD0 [0] = 0 (default)	Enables PLL “CG_PLL2” to generate 48Mhz clock internally.
	PM_IO 0xBD [4] = 1	Enables the internal 48Mhz as the clock source to USBPHY
	PM_IO 0xBD [6] = 1 (optional)	Enables the IO pad “USBCLK/14M_25M_48M” as clock output pad that it can be used for on board devices. This is optional (depending on board requirement).

Note: To use internal 48 MHz clock, the 100 MHz PCIe® clock sourced from the external clock chip must not have spread spectrum enabled.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.8 Adjusting USB 2.0 Ports Driving Strength

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Step 1: EHCI_BAR 0xB4 [2:0] = “HSADJ” EHCI_BAR 0xB4[12] = 0 EHCI_BAR 0xB4 [16:13] = “port#” Step 2: EHCI_BAR 0xB4[12] = 1	Adjusts the USB2.0 ports driving strength. HSADJ to set the driving strength value VLoadB to load the value to the PHY for selected port The selected port# The SBIOS can repeat step-1 for those ports with less margin on HS eye diagram. Set to ‘1’ to lock PHY UTMI Control interface.

Note:

1. Different board designs may require different settings for different ports depending on trace length and routing.

2. Only apply the setting to the ports that have longer USB trace lengths (> 12 inches) to the connector, and if the eye diagram margin is not enough. There is no need to apply these setting to the ports with shorter trace lengths or close to the USB connectors.

3. EHCI_BAR 0xB4 = EHCI_EOR 0x94 (UTMI Control Register)

4. EHCI_BAR 0xB4[2:0] (HSADJ)
   “000” = -10% , “001” = -5%, “100” = 0%, “101” = +5%, “110” = +10%
   EHCI_BAR 0xB4[16:13] (port#)
   “0000” = port0 , “0001” = port1, …… “0101” = port5, 0110 ~ 1110: reserved.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.9 In and Out Data Packet FIFO Threshold

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	EHCI_BAR 0xA4 = 0x00400040	IN/OUT data packet FIFO threshold for EHCI controllers. Normal operation the FIFO threshold settings **FIFO threshold setting must be programmed in both the EHCI host controllers,** **Bus-0, dev-18 fun 2 and Bus 0 dev-19 fun-2**

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.10 OHCI MSI Function Setting

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	OHCI0_PCI_Config 0x40[9:8] = ”11”	OHCI MSI function For normal operation the MSI function must be disabled by setting bits [9:8] on dev-18, fun-0, and dev-19, fun-0, OHCI controllers and bit [8] on dev-20, fun-5, OHCI controller. **bus-0, dev-18 fun 0 / bus-0, dev-19 fun 0** **bus-0, dev-20, fun-5.**

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.11 EHCI Advance Asynchronous Enhancement

See section 6.22

6.12 EHCI Advance PHY Power Savings

ASIC Rev	Register Settings	Function/Comment
SP5100 A11	EHCI_PCI_Config 0x50[31] = 0	Disables Advance PHy power saving for normal operation. This register bit defaults to ‘0’ on power up. The BIOS should not program this register bit to 1 in both EHCI controllers. **Bus-0, dev-18 fun 2 and Bus 0 dev-19 fun-2**
SP5100 A12	EHCI_PCI_Config 0x50[31] = 1	Enables Advance PHY power saving feature. The BIOS should program this register bit to 1 in both EHCI controllers. **Bus-0, dev-18 fun 2 and Bus 0 dev-19 fun-2**

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.13 Enabling Fix for EHCI Controller Driver Yellow Sign Issue

ASIC Rev	Register Settings	Function/Comment
SP5100 A12	EHCI_PCI_Config 0x50[20] = 1	Enables the fix for the yellow sign issue observed when the HSET driver gets unloaded and the in box EHCI driver gets loaded.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.14 Enabling Fix to Cover the Corner Case S3 Wake Up Issue

ASIC Rev	Register Settings	Function/Comment
SP5100 A12	OHCI 0_PCI_Config 0x50[16] = 1	Enables the fix to cover the corner case S3 wake up issue seen with some specific USB 1.1 keyboards.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.15 EHCI Async Park Mode

See section 6.20

6.16 MSI Feature in USB 2.0 Controller

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	EHCI_PCI_Config 0x50[6] = 1	MSI function For normal operation the MSI function should be disabled by setting the bit in both EHCI controllers. **Bus-0, dev-18 fun 2 and Bus 0 dev-19 fun-2**

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.17 EHCI Dynamic Clock Gating Feature

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	EHCI_BAR 0xBC Bit[12] = 0	For normal operation, the clock gating feature must be disabled. At system reset, this bit is set to "1". So, BIOS needs to program this bit to "0". EHCI clock gating setting must be programmed in both the EHCI host controllers. **Bus-0, dev-18 fun 2 and Bus 0 dev-19 fun-2**

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.18 USB 1.1 ISO OUT Devices/Speaker Noise

ASIC Rev	Register Settings	Function/Comment
SP5100 A14 and above	a. ABCFG 0x90[17] = 1 b. OHCI0 PCI_Config 0x50[25] = 1	Settings a and b are required for revision A14 and above to resolve the USB 1.1 speaker noise issue as described in A12 Errata item #8. The bits must be programmed in all three OHCI controllers: Bus-0 Dev-18 Func-0, Bus-0 Dev-19 Func-0, and Bus-0 Dev-20 Func-5.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the *SP5100 Register Reference Guide.*
	x							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

6.19 USB Controller DMA Read Delay Tolerant

ASIC Rev	Register Settings	Function/Comment
SP5100 A14 and above	EHCI_PCI_Config 0x50[7] =0	This bit should not be programmed by software. It should be left at hardware default setting of '0'. Setting this bit to 1 may cause system hang due to long memory read delays that can occur when the system is in PM states or when other clients, such as integrated GFX, get higher priority to memory. Note: Bit 7 of both EHCI host controllers (Bus-0 Dev-18 Func-2, and Bus-0 Dev-19 Func-2) should be left at '0'.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the *SP5100 Register Reference Guide.*
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.20 Async Park Mode

ASIC Rev	Register Settings	Function/Comment
SP5100 All Revs	EHCI PCI_Config 0x50[23] = 1	Async Park Mode function. For normal operation, the APM function should be disabled by setting the bit in both EHCI controllers: Bus-0 Dev-18 Func-2 and Bus 0 Dev-19 Func-2 If EHCI APM is enabled, some USB card reader devices may not work properly. The USB controller used on these devices may not be able to handle the short delay time between the data packets.
SP5100 A14 and above	EHCI PCI_Config 0x50[2] = 0	Disable Async Park Extra Mode function. This is hardware default; BIOS should not program the register. This bit should be disabled in USB1 EHCI controller only. Bus-0 Dev-18 Func-2. The bit in Bus-0 Dev-19 Func-2 is reserved and should not be programmed.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the *SP5100 Register Reference Guide.*
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.21 Resume Reset Timing

ASIC Rev	Register Settings	Function/Comment
SP5100 A14 and above	OHCI 0 PCI_Config 0x50[17] = 1	Set this bit to 1 on revision A14. This register setting is required to enable the Reset Timing feature. This feature will resolve the issue listed in A12 Errata (item #7). The bit must be programmed in both of the OHCI0 controllers: Bus-0 Dev-18 Func- 0 and Bus 0 Dev-19 Func-0

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the *SP5100 Register Reference Guide.*
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.22 Disable Async QH Cache

ASIC Rev	Register Settings	Function/Comment
SP5100 A15	EHCI PCI Config 0x50[25] = 1	Disable Async QH/QTD Cache

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the *SP5100 Register Reference Guide.*
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.23 Advance Async Enhancement

ASIC Rev	Register Settings	Function/Comment
SP5100 A12	EHCI PCI Config 0x50[28] = 1	Advance asynchronous enhancement function. For normal operation, the AAE function should be disabled by setting the bit in both EHCI controllers: Bus-0 Dev-18 Func-2 and Bus-0 Dev-19 Func-2 Enabling this function may cause USB 2.0 device to malfunction or be undetected.
SP5100 A14 and above	EHCI_PCI_Config 0x50[3] =1 EHCI PCI Config 0x50[28] = 0	Set this bit 3 to 1 Clear this bit 28 This enhancement on A14 and above will improve the USB performance when more than one USB device is connected. The bits must be programmed in both of the EHCI host controllers: Bus-0 Dev-18 Func-2 and Bus-0 Dev-19 Func-2

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the ***SP5100 Register Reference Guide.***
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.24 USB Periodic Cache Setting

ASIC Rev	Register Settings	Function/Comment
SP5100 A12	EHCI_PCI_Config 0x50[27] =1	Set this bit to 1 on revision A12 Should be done for non Windows OS only. The bit must be programmed in both of the EHCI host controllers: Bus-0 Dev-18 Func-2 and Bus 0 Dev-19 Func-2
SP5100 A14 and above	EHCI_PCI_Config 0x50[8] =1 EHCI_PCI_Config 0x50[27] =0	Set bit 8 to 1 on revision A14 and above Clear bit 8 or do not program if untouched after power up. The bits must be programmed in both of the EHCI host controllers: Bus-0, Dev-18 Func-2 and Bus 0 Dev-19 Func-2

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the ***SP5100 Register Reference Guide.***
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.25 USB PID_ERROR_CHECKING

ASIC Rev	Register Settings	Function/Comment
SP5100 A15	EHCI_PCI_Config 0x50[9] =1	Set this bit to enable the Error checking on PID Bus-0 Dev-18 Func-2 and Bus 0 Dev-19 Func-2

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the ***SP5100 Register Reference Guide.***
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

7 SATA: dev-17, func-0

7.1 Enabling SATA

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Smbus_PCI_config 0xAC [8] = 1	Enables the SATA controller.

7.2 SATA Initialization

<table>
<tr><th>ASIC Rev</th><th>Register Settings</th><th>Function/Comment</th></tr>
<tr><td rowspan="3">All Revs SP5100</td><td>Smbus_PCI_config 0xAC [28:26]</td><td>SATA interrupt mapping to PCI interrupt pins. These bits should be programmed by the BIOS for correct assignment of SATA interrupt mapping/</td></tr>
<tr><td>SATA_PCI_config 0x40 [0] = 0</td><td>This bit needs to be cleared to convert the subclass code register to read-only. Refer to section 7.6 for the SATA subclass programming sequence.</td></tr>
<tr><td>SATA_PCI_config 0x44 [0] = 1</td><td>Enables the SATA watchdog timer register prior to the SATA BIOS post. See Note.</td></tr>
<tr><td>SP5100 A12</td><td>SATA_PCI_config 0x40 [29] = 1
SATA_PCI_config 0x48 [24] = 1</td><td rowspan="3">Set bit 29 and 24 for A12.
Bit 29 and 24 on A14 are cleared on power-up. These bits can be set to 0 or not programmed.

Clearing bit 29 and 24 will enable the hardware to send the byte count updates during the AHCI mode PIO transfers to meet the SATA Specification. On A12, the byte count updates are not sent and the bit should be left as 0. The feature is required only for certain vendor-specific diagnostics that check the updated byte counts status. There is no functional impact as the OS drivers do not check for the byte count during the PIO transfer but only after the transfer is completed. On both A12 and A14, the byte count is updated after the transfer is completed, even without this feature enabled.</td></tr>
<tr><td>SP5100 A14 and above</td><td>SATA_PCI_config 0x40 [29] = 0
SATA_PCI_config 0x48 [24] = 0</td></tr>
<tr><td colspan="2">Restore the registers on the following conditions:
<table><tr><th></th><th colspan="2">ASIC Revision</th></tr><tr><th>Restore after</th><th>A12</th><th>A14, A15</th></tr><tr><td>S3</td><td>Yes</td><td>Yes</td></tr><tr><td>S4</td><td>Yes</td><td>No</td></tr><tr><td>Warm boot</td><td>Yes</td><td>No</td></tr></table></td></tr>
<tr><td>SP5100 A12</td><td>SATA_PCI_config 0x48 [21] = 1</td><td rowspan="3">Set bit 21 for A12

Bit 21 on A14 and above is cleared on power up. This bit can be set to 0 or not programmed.

Clearing the bit will enable the compatibility feature. It allows the SATA controller to be able to handle the case where the device might follow COMWAKE with one Align instead of multiple Aligns as required normally. This is not a normal case for the devices, but was observed on one of the SATA devices during qualification.</td></tr>
<tr><td>SP5100 A14 and above</td><td>SATA_PCI_config 0x48 [21] = 0</td></tr>
<tr><td colspan="2">Restore the registers on the following conditions
<table><tr><th></th><th colspan="2">ASIC Revision</th></tr><tr><th>Restore after</th><th>A12</th><th>A14, A15</th></tr><tr><td>S3</td><td>Yes</td><td>Yes</td></tr><tr><td>S4</td><td>Yes</td><td>No</td></tr><tr><td>Warm boot</td><td>Yes</td><td>No</td></tr></table></td></tr>
</table>

SP5100 A14 and above	SATA_PCI_config 0x48 [13:7] = 7'h7F SATA_PCI_config 0x48 [14] = 0 (default) SATA_PCI_config 0x48 [15] = 1 The setting to these register bits should be restored to 1 for A14 1. On resume from S3 and S4. 2. After warm boot reset.	The registers listed here apply only to revision A14 and above. These bits enable enhancements made in the A14 and above to address compatibility or minor spec violation issues seen in simulation. The SATA test/enhancement mode should be enabled by programming these registers to 1s. The default power-up setting for these registers are 0s.
SP5100 A14 and above	SATA_PCI_config 0x48 [6] = 1	Setting this bit to 1 will allow the Activity LED to go off when there is no activity and the driver does not send additional commands due to user intervention of the Vista OS boot process (by pressing the F8 key). Applies to configuration in which the ODD is attached to Slave Port in IDE mode.
SP5100 A14 and above	Smbus_PCI_config 0xAC [13] = 0	The SATA test/enhancement mode should be enabled by programming this register to 0. The default power-up setting for this register is 1. The setting to this register bit should be restored to 0 for A14 and above. 1. On resume from S3 and S4 2. After warm boot reset
All Revs SP5100	SATA_BAR5 + Port offset + 0x10 = FFFFh	This setting applies only when BIOS is using IDE to AHCI or AMD IDE to AHCI modes. To clear the error status, software needs to write 1 to this register. For all SATA ports that are going to be visible to the OS, BIOS should write 1 to bits [31:00] of the corresponding port register just before passing the control to the OS.
All Revs SP5100	SATA_PCI_config 0x40 [23] = 1	Disable AHCI enhancement. This feature is not supported. For proper operation, this feature should be disabled
Note: The system may hang during post if this register is not set correctly.		

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the ***SP5100 Register Reference Guide.***
X		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

7.3 Disabling SATA

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Smbus_PCI_config 0xAC [8] = 0	Disables the SATA controller. This shuts down most clocks in the SATA controller.
	Smbus_PCI_config 0xAC [9] = 1	Disables the SATA PHY I2C interface. This setting is mandatory to prevent un-powered SATA from corrupting SMbus controller protocol.
Note: Some board designs may choose to disable the SATA controllers to reduce power consumption.		

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

7.4 Disabling Unused SATA Ports

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	SATA_PCI_config 0x40 [16] = 1	When set, SATA port0 is disabled, and port0 clock is shut down.
	SATA_PCI_config 0x40 [17] = 1	When set, SATA port1 is disabled, and port1 clock is shut down.
	SATA_PCI_config 0x40 [18] = 1	When set, SATA port2 is disabled, and port2 clock is shut down.
	SATA_PCI_config 0x40 [19] = 1	When set, SATA port3 is disabled, and port3 clock is shut down.
	SATA_PCI_config 0x40 [20] = 1	When set, SATA port4 is disabled, and port4 clock is shut down.
	SATA_PCI_config 0x40 [21] = 1	When set, SATA port5 is disabled, and port5 clock is shut down.
Note: Some board designs may choose to disable unused SATA ports to reduce power consumption.		

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
X								
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

7.5 SATA Subclass Programming Sequence

The SATA controller supports the following modes:

- IDE mode
- AHCI mode
- Raid mode

The SBIOS programs the subclass code and the interface register to enable the SATA controller to be represented as the IDE controller, the AHCI controller, or the Raid controller.

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	1. SATA_PCI_config 0x40 [0] = 1	Enables the subclass code register (PCI config register 0Ah) and the program interface register (PCI config register 09h) to be programmable.
	2. Program SATA Controller mode in a) IDE mode, or SATA_PCI_config 0x09 = 0x8f (default) SATA_PCI_config 0x0A = 0x01 b) AHCI mode, or SATA_PCI_config 0x09 = 0x01 SATA_PCI_config 0x0A = 0x06 c) RAID mode SATA_PCI_config 0x09 = 0x00 SATA_PCI_config 0x0A = 0x04	The SBIOS is required to program the subclass code register of the SATA controller to be represented as the IDE, AHCI, or the RAID controller.
	3. SATA_PCI_config 0x40 [0]= 0	Clears the bit to convert the subclass code register to be a read-only register. The SBIOS is required to complete this step to ensure that the subclass code register be read-only (in order to be PCI compliant).

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
X								
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

7.6 SATA PHY Programming Sequence

The SBIOS needs to program the SATA controllers in the following sequence. Performing this procedure gives enough time for the SATA controllers to correctly complete SATA drive detection. The SBIOS needs to do the same procedure after the system resumes back from the S3 state.

Note: This will be added once the silicon comes back for PHY fine tune value.

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	1. SATA_PCI_config 0x86 [15:0] = 0x2C00	SATA PHY global setting.
	2. SATA_PCI_config 0x88 [31:0] = 0x01B48017 SATA_PCI_config 0x8C [31:0]= 0x01B48019 SATA_PCI_config 0x90 [31:0] = 0x01B48016 SATA_PCI_config 0x94 [31:0] = 0x01B48016 SATA_PCI_config 0x98 [31:0] = 0x01B48016 SATA_PCI_config 0x9C [31:0] = 0x01B48016	SATA GENI PHY ports setting, pre-emphasis setting, and GENII PHY setting enable setup for port [0~5] This setting is for the Travelly board. Since its port0 and port1are eSATA ports, PCI_config 0x88 and 0x8C have different settings than the rest of the ports. For non-eSATA port, the setting should be 0x01B48016. For the Shinner board, SATA_PCI_config 0x88/8C/90/94/98/9C [31:0] = 0x01B48016.
	3.SATA_PCI_config 0xA0 [15:0] = 0xA09A SATA_PCI_config 0xA2 [15:0] = 0xA09F SATA_PCI_config 0xA4 [15:0] = 0xA07A SATA_PCI_config 0xA6 [15:0] = 0xA07A SATA_PCI_config 0xA8 [15:0] = 0xA07A SATA_PCI_config 0xAA [15:0] = 0xA07A	SATA GEN II PHY port setting for port [0~5]. This setting is for the Travelly board. Since its port0 and port1 are eSATA ports, PCI_config 0xA0 and 0xA2 have different settings than the rest of the ports. For non-esata port, the setting should be 0xA07A. For the Shinner board, SATA_PCI_config 0xA0/A2/A4/A6/A8/AA [15:0] = 0xA07A.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
X								
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

7.7 SATA Identification Programming Sequence for IDE Mode

7.7.1 SATA Drive Detection

The following sequence should be included in the SBIOS drive identification loop for SATA drives detection.

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	1. If any of the SATA port status register SATA_BAR5 + 0x128 [3:0] = 0x3 SATA_BAR5 + 0x1A8 [3:0] = 0x3 SATA_BAR5 + 0x228 [3:0] = 0x3 SATA_BAR5 + 0x2A8 [3:0] = 0x3 SATA_BAR5 + 0x328 [3:0] = 0x3 SATA_BAR5 + 0x3A8 [3:0] = 0x3 Then set SATA_BAR0 + 0x6 = 0xA0 or SATA_BAR0 + 0x6 = 0xB0 or SATA_BAR2 + 0x6 = 0xA0 or SATA_BAR2 + 0x6 = 0xB0 or PATA_BAR0/2 + 0x6 = 0xA0 or PATA_BAR0/2 + 0x6 = 0xB0 or Go to step (2). Else No drive is attached, exit the detection loop.	SATA_BAR5 + 0x128h : port 0 status register SATA_BAR5 + 0x1A8h : port 1 status register SATA_BAR5 + 0x228h : port 2 status register SATA_BAR5 + 0x2A8h : port 3 status register SATA_BAR5 + 0x328h : port 4 status register SATA_BAR5 + 0x3A8h : port 5 status register SATA host and device serial interface communication is done and ready if the SATA port status register = 0x3. for SATA controller primary master emulation for SATA controller primary slave emulation for SATA controller secondary master emulation for SATA controller secondary slave emulation for PATA controller primary/secondary master emulation for PATA controller primary/secondary slave emulation Otherwise, No SATA drive attached or SATA drive is not ready.
	2. If SATA_BAR0 + 0x6 = 0xA0 and SATA_BAR0 + 0x7 [7] & [3] = 0 Or SATA_BAR0 + 0x6 = 0xB0 and SATA_BAR0 + 0x7[7] & [3] = 0 Or SATA_BAR2 + 0x6 = 0xA0 and SATA_BAR2 + 0x7[7] & [3] = 0 Or SATA_BAR2 + 0x6 = 0xB0 and SATA_BAR2 + 0x7[7] & [3] = 0 Or PATA_BAR0/2 + 0x6 = 0xA0 and PATA_BAR0/2 + 0x7[7] & [3] = 0 Or PATA_BAR0/2 + 0x6 = 0xB0 and PATA_BAR0/2 + 0x7[7] & [3] = 0 then the drive detection is completed Else loop until 30s time out, drive detection fail	SATA_BAR0 + 0x7[7] & [3] = 0 means primary master device ready SATA_BAR0 + 0x7[7] & [3] = 0 means primary slave device ready SATA_BAR2 + 0x7[7] & [3] = 0 means secondary master device ready SATA_BAR2 + 0x7[7] & [3] = 0 means secondary slave device ready PATA_BAR0/2 + 0x7[7] & [3] = 0 means primary /secondary master device ready PATA_BAR0/2 + 0x7[7] & [3] = 0 means primary /secondary slave device ready There is no SATA device attached on the port if time out occurs (see Note).
Note: Most drives do not need 10s timeout. The 10s timeout is only needed for some particularly large capacity SATA drives, which require a longer spin-up time during a cold boot.		

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
X								
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

7.8 Restoring SATA Registers after S3 Resume State

The following registers need to be restored by the SBIOS after S3 resume for the SATA controller.

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	SATA_PCI_config 0x09 [7:0] SATA_PCI_config 0x0A [7:0]	Programmable interface and Subclass code. To program the subclass code register, SATA_PCI_config x40[0] needs to be set. After the subclass is programmed, SATA_PCI_config 0x40[0] needs to be reset.
	SATA_PCI_config 0x44 [0]	Enables the Watch-dog timer for the all ports.
SP5100 A12	SATA_PCI_config 0x40 [29]	Disables the testing/enhancement mode.
SP5100 A12	SATA_PCI_config 0x48 [24]	Disables the testing/enhancement mode.
SP5100 A12	SATA_PCI_config 0x48 [21]	Disables the testing/enhancement mode.
SP5100 A14 and above	SATA_PCI_config 0x40 [29] SATA_PCI_config 0x48 [24] SATA_PCI_config 0x48 [21] SATA_PCI_config 0x48 [15:9] Smbus_PCI_config 0xAC [13]	Enables the testing/enhancement mode.
All Revs SP5100	SATA_PCI_config 0x86 [15:0] SATA_PCI_config 0x88 [24:0] SATA_PCI_config 0x8C [24:0] SATA_PCI_config 0x90 [24:0] SATA_PCI_config 0x94 [24:0] SATA_PCI_config 0x98 [24:0] SATA_PCI_config 0x9C [24:0] SATA_PCI_config 0xA0 [15:0] SATA_PCI_config 0xA2 [15:0] SATA_PCI_config 0xA4 [15:0] SATA_PCI_config 0xA6 [15:0] SATA_PCI_config 0xA8 [15:0] SATA_PCI_config 0xAA [15:0]	SATA PHY setting.
All Revs SP5100	SATA_PCI_config 0x34 [7:0] SATA_PCI_config 0x61 [7:0]	SATA Capability
All Revs SP5100	SATA BAR5 + 0xF8[17:0]	SATA ports indication registers.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
X								
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

7.9 Internal and External SATA Ports Indication Registers

The following registers need to be programmed for eSATA ports

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	For the ports which are configured as iSATA ports. 1.PxCMD.ESP should leave as reset default (logic 0). 2.PxCMD.HPCP should be cleared. To clear the register, write: Port0: SATA BAR5 + 0xF8[0]=0 Port1: SATA BAR5 + 0xF8[1]=0 Port2: SATA BAR5 + 0xF8[2]=0 Port3: SATA BAR5 + 0xF8[3]=0 Port4: SATA BAR5 + 0xF8[4]=0 Port5: SATA BAR5 + 0xF8[5]=0 For the ports which configured as eSATA. 1.PxCMD.ESP should be set. To set the register, write: Port0: SATA BAR5 + 0xF8[12]=1 Port1: SATA BAR5 + 0xF8[13]=1 Port2: SATA BAR5 + 0xF8[14]=1 Port3: SATA BAR5 + 0xF8[15]=1 Port4: SATA BAR5 + 0xF8[16]=1 Port5: SATA BAR5 + 0xF8[17]=1 2.PxCMD.HPCP should be cleared. To clear the register, write: Port0: SATA BAR5 + 0xF8[0]=0 Port1: SATA BAR5 + 0xF8[1]=0 Port2: SATA BAR5 + 0xF8[2]=0 Port3: SATA BAR5 + 0xF8[3]=0 Port4: SATA BAR5 + 0xF8[4]=0 Port5: SATA BAR5 + 0xF8[5]=0 3. If any of the ports is programmed as External Port, HCAP.SXS should also be set. To set the register, write: SATA BAR5 + 0xFC[20]=1	PxCMD.ESP (External SATA Port) and PxCMD.HPCP (Hot Plug Capable Port) registers should be programmed to indicate if the port is used for External SATA and if it requires hot Plug capability. For iSATA (internal SATA) port(s), Px.CMD.HPCP and Px.CMD.ESP should be logic 0. To program these registers, SATA_PCI_config x40[0] needs to be set. After the subclass is programmed, SATA_PCI_config 0x40[0] needs to be reset. For example, if port 0 was configured as eSATA, other Ports are iSATA. SATA BAR5 + F8[17:12]= 000001(b) SATA BAR5 + F8[5:0] = 000000(b) PxCMD.ESP bit is mutually exclusive with PxCMD.HPCP bit in the same port. In general: If no E-SATA ports in system then HCAP.SXS=0 else HCAP.SXS=1. ESP HPCP eSATA (signal only connector) 1 0 iSATA 0 0 PxCMD ESP located at: SATA BAR5+ port offset + 0x18[21] PxCMD HPCP located at: SATA BAR5+ port offset + 0x18[18]

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
X								
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

7.10 Aggressive Link Power Management

ALPM controls the HIPM functionality. The ALPM bit is also used by the SATA driver to enable HIPM and DIPM. Customers should check with the drive vendor to confirm if the SATA device being used is compatible and functional with HIPM and DIPM capability before enabling the ALPM.

HIPM and DIPM are supported in the SP5100. If the customer requires HIPM / DIPM support and gets confirmation from the drive vendors that the drivers they are supporting will enable HIPM, then this feature can be enabled. The following registers need to be programmed to disable the ALPM. **Note**: If the ALPM needs to be enabled, the following sequence should **NOT** be programmed.

Sequence to disable ALPM:

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	1. SATA_PCI_config 0x40 [0] = 1	Unlocks the configuration register so that HBA AHCI Capabilities Register can be modified.
	2. SATA_BAR5 + 0xFC [11] = 0	Clearing this bit has the following effects. The Support-Aggressive-Link-Power-Management Capability is hidden from software in AHCI HBA Capabilities Register. As a result, software will not enable the HBA to aggressively enter power-saving (Partial/Slumber) mode. Once this bit is cleared, SATA BAR5 + 0x00[26] will be 0
	3. SATA_PCI_config 0x40 [0]= 0	Clears the bit to lock configuration registers so that AHCI HBA Capabilities register is read-only.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
X								
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

7.11 SATA MSI and D3 Power State Capability

7.11.1 SATA MSI Settings

SATA controller does not support message based interrupts. The capability pointer offset needs to be re-programmed from its default setting to prevent the driver from enabling this feature.

7.11.2 D3 Power State Settings

SATA controller does not support D3 Power State if S1 is supported. The capability pointer offset needs to be re-programmed from its default setting to prevent the driver from enabling this feature.

7.11.3 Capability Pointer Settings

The following settings re-program the capability pointer to the recommended start of the capabilities table of supported features (hide MSI, and if S1 is supported, hide D3 state capability from driver/OS).

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	1. SATA_PCI_config 0x40 [0] = 1 2. SATA_PCI_config 0x61[7:0]=0x70 3. SATA_PCI_config 0x40 [0] = 0	D3 power state is visible. (If S1 is not supported) MSI capability for SATA is hidden.
All Revs SP5100	1. SATA_PCI_config 0x40 [0] = 1 2. SATA_PCI_config 0x34[7:0]=0x70 3. SATA_PCI_config 0x40 [0] = 0	D3 power state is hidden. (If S1 is supported) MSI capability for SATA is hidden.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the ***SP5100 Register Reference Guide.***
x								
RTC	**ACPI**	**PM REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			

7.12 Disabling CCC (Command Completion Coalescing) Support

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	1. SATA_PCI_config 0x40 [0] = 1	Unlocks the configuration register so that HBA AHCI Capabilities register can be modified.
	2. SATA_BAR5 + 0xFC [19] = 0	Clearing this bit has the following effects: Once this bit is cleared, SATA BAR5 + 0x00[7] will be 0 Command Completion Coalescing function will not be supported.
	3. SATA_PCI_config 0x40 [0] = 0	Clears the bit to lock configuration registers so that AHCI HBA Capabilities register is read-only.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details, refer to the sections check-marked in the ***SP5100 Register Reference Guide.***
X								
RTC	**ACPI**	**PM REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			

Register 0xFC[19] controls the CCC capability setting in register BAR5, offset 0 bit 7. Setting it to 0 will make CCC not visible to software. CCC is enabled by default, on power up. Default. BIOS should leave 0xFC[19] untouched for normal operation. The setting to disable should only be used if CCC needs to be disabled for specific platform configuration.

8 LPC (bus-0, dev-20, fun-03)

8.1 Enabling/Disabling LPC Controller

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Smbus_PCI_config 0x64 [20] = 1 (default)	Enables the LPC controller.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

8.2 Parallel Port ECP Mode Support

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	If IO 0x378 & IO 0x778 as ECP (or ECP+EPP) address port is used: LPC_PCI_config 0x44 [0] = 1 LPC_PCI_config 0x44 [1] = 1 If IO 0x278 & IO 0x678 as ECP (or ECP+EPP) address port is used: LPC_PCI_config 0x44 [2] = 1 LPC_PCI_config 0x44 [3] = 1 If IO 0x3BC & IO 0x7BC as ECP (or ECP+EPP) address port is used: LPC_PCI_config 0x44 [4] = 1 LPC_PCI_config 0x44 [5] = 1	For the parallel port to support ECP mode, or ECP+EPP mode, the SBIOS needs to allocate 2 base addresses for the parallel port. base_address_2 = base_address_1 + 0x400 Base_address_1 is controlled by register bit 0, or bit 2, or bit 4. Base address_2 is controlled by register bit 1, or bit 3, or bit 5. The SBIOS needs to enable both base addresses to properly support ECP (or ECP+EPP) mode.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
						X		
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

9 IDE Controller (bus-0, dev-20, fun-01)

The SP5100 IDE controller supports single primary channel, even though resources of the secondary IDE channel are allocated by the in-box driver from the Microsoft operating system. Therefore the IDE programmable interface (IDE PCI config 0x09 bits [3:2]) is not recommended for modification.

9.1 Disable Second IDE MSI Capability

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	IDE PCI_config 0x63 [5]=0	Hide MSI capability pointer.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
			X					
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

9.2 Enable IDE Data Bus DD7 Pull-Down Resistor

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	ACPI PMIO2 0xE5 [2] = 1	Enables IDE data bus DD7 internal pull down resistor at IO pad. This PD should be enabled whenever IDE controller enabled. Note: If the FLASH controller is enabled or IDE DD& has external PD, then this register should not be set. Resume from S3 does not require to reset this bit.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
			X					
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

10 HD Audio (bus-0, dev-20, fun-02)

10.1 Enabling/Disabling HD Audio

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	PM_IO 0x59[3] = 1 (default)	0 = Disables the HD Audio controller 1 = Enables the HD Audio controller

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		x						

10.2 HD Audio Interrupt Routing Table

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Smbus_PCI_config 0x63[2:0] = 110 (default)	Interrupt routing table for HD Audio: 000 = INTA# 001 = INTB# 010 = INTC# 011 = INTD# 100 = INTE# 101 = INTF# 110 = INTG# 111 = INTH#

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

10.3 Audio Port Configuration

This register controls the selection of ACZ_SDIN0/GPIO42, ACZ_SDIN1/GPIO43, ACZ_SDIN2/GPIO44, and AZ_SDIN3/GPIO46 pins to function as GPIO, AC97, or HD Audio signals.

ASIC Rev	Register Settings	Function/Comment
All Revs SP5100	Smbus_PCI_Config_Extend_Reg 0x00[1:0] = 01 (default)	Port 0 configuration for HD Audio/AC97/GPIO: 00 or 11 = GPIO 01 = no function 10 = HD Audio Note: Port 0 refers to the ACZ_SDIN0/GPIO42 pin.
All Revs SP5100	SMbus_PCI_config_Extend_Reg 0x00[3:2] = 01 (default)	Port 1 configuration for HD Audio/AC97/GPIO: 00 or 11 = GPIO 01 = no function 10 = HD Audio Note: Port 1 refers to the ACZ_SDIN1/GPIO43 pin.

All Revs SP5100	Smbus_PCI_Config_Extend_Reg 0x00[5:4] = 10 (default)	Port 2 configuration for HD Audio/AC97/GPIO: 00 or 11 = GPIO 01 = no function 10 = HD Audio Note: Port 2 refers to the ACZ_SDIN2/GPIO44 pin.
All Revs SP5100	Smbus_PCI_Config_Extend_Reg 0x00[7:6] = 10 (default)	Port 3 configuration for HD Audio/AC97/GPIO: 00 or 11 = GPIO 01 = no function 10 = HD Audio Note: Port 3 is the AZ_SDIN3/GPIO46 pin.

Note: The Smbus_PCI_Config_Extend_Reg are indirectly accessed registers that are accessed through Smbus_PCI_config xF8 (ExtendedAddrPort) and Smbus_PCI_config xFC (ExtendedDataPort). Refer to the *AMD SP5100 Register Reference Guide*, SMBUS section describing the PCI config xF8/FC details.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the SP5100 Register Reference Guide
		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

Appendix A: Sample Codes for BIOS Workarounds

A1. Sample Code for SP5100 Erratum #11: “Enabling EHCI Dynamic Clock Gating May Cause Bug Code 0xFE System Error”.

(Refer to section *6.17 “EHCI Dynamic Clock Gating Feature”*)

Note: This code is found in the SP5100 BIOS because SP5100 shares the same CIMx as the SB7xx. It has no relevance for the SP5100 but is included in case it shows up in a software debugging process.

The programming of the registers in this workaround needs to be done only during S5/S4 to S0 transitions. On resume from S3, these registers are not required to be re-programmed.

```
;Description:
; This sample code disables ECHI dynamic clock gating feature by clearing bit 12
; in the EHCI BAR (MMIO) Register Offset 0xBC.
;Requirement:
; 1. USB BARs must be programmed before executing this piece of code
; 2. es segment register should be set to base 0 and limit set to 4GB
 pushad
 ;For EHCI controller 1 (Bus 0 Dev 0x12 Fun 2)
 ;read BAR address
 mov eax, 080009210h
 mov dx, 0CF8h
 out dx, eax
 mov dx, 0CFCh
 in eax, dx
 cmp eax, 0
 je EHCI1_BAR_NOT_SET
 cmp eax, -1
 je EHCI1_BAR_NOT_SET

 ;enable memory access
 mov eax, 080009204h
 mov dx, 0CF8h
 out dx, eax
 mov dx, 0CFCh
 in eax, dx
```

```
or al, 02h
out dx, eax

mov eax, 080009210h
mov dx, 0CF8h
out dx, eax
mov dx, 0CFCh
in eax, dx

mov edi, eax
add edi, 0BCh
mov eax, es:[edi] ;es should be set to 0, and the segment limit should be set 0 to 4GB
and ax, 0EFFFh ;clear BIT12
mov es:[edi], eax

EHCI1_BAR_NOT_SET:
;For EHCI controller 2 (Bus 0 Dev 0x13 Fun 2)
;read BAR address
mov eax, 080009A10h
mov dx, 0CF8h
out dx, eax
mov dx, 0CFCh
in eax, dx
cmp eax, 0
je EHCI2_BAR_NOT_SET
cmp eax, -1
je EHCI2_BAR_NOT_SET

;enable memory access
mov eax, 080009A04h
mov dx, 0CF8h
out dx, eax
mov dx, 0CFCh
in eax, dx
or al, 02h
out dx, eax
```

```
mov eax, 080009A10h
mov dx, 0CF8h
out dx, eax
mov dx, 0CFCh
in eax, dx

mov edi, eax
add edi, 0BCh
mov eax, es:[edi] ;es should be set to 0, and the segment limit should be set 0 to 4GB
and ax, 0EFFFh ;clear BIT12
mov es:[edi], eax

EHCI2_BAR_NOT_SET:
popad
```

End of Sample Code (Erratum # 11)

A2. Sample Code for SP5100 Erratum #23: “USB Wake on Connect/Disconnect with Low Speed Devices”.

(Refer to section *6.2* “*USB Device Support to Wake Up System from S3/S4 State*”)

The following workaround should be implemented in the platform BIOS to resolve the issue as described in the SB7x0 Erratum #23.

This routine has to be put in the Sleep trap function.

```
USBConnectWorkaround PROC NEAR
; testing for EHCI wake event
;jmp $
        pushad

; Enabled Support USB Wake-Up event on Resume only
        mov     dx, 0cd6h
        mov     al, 065h
        out     dx, al
        inc     dx
        in      al, dx
        or      al, BIT6
        out     dx, al

        mov     dx, 824h
        in      ax, dx
        or      ax, bit11
        out     dx, ax

; USB wake-up event.

; Enabled EHCI0 & BAR
        mov     dx, (18 shl 3) + 2              ; EHCI 0
        mov     ah, 0c4h
        call    read_pci_dword_far              ; Set back to D0 state
        and     ebx, 0fffffff0h
        call    write_pci_dword_far

        mov     ah, 004h                        ;
        call    read_pci_dword_far
        or      ebx, 07h                        ; Enabled IO/Memory/Bus
        call    write_pci_dword_far

        mov     dx, (18 shl 3) + 2              ;
        mov     ah, 10h                         ; Get Bar address
        call    read_pci_dword_far              ; in EBX

        call  USBWorkaroundForConnected

        mov     dx, (18 shl 3) + 2              ;
```

```
        mov     ah, 0c4h
        call    read_pci_dword_far
        or      ebx, 03h                        ; Set to D3 state
        call    write_pci_dword_far

; Enabled EHCI1 & BAR
        mov     dx, (19 shl 3) + 2              ; EHCI 1
        mov     ah, 0c4h
        call    read_pci_dword_far              ; Set back to D0 state
        and     ebx, 0fffffff0h
        call    write_pci_dword_far

        mov     ah, 004h                        ;
        call    read_pci_dword_far
        or      ebx, 07h                        ; Enabled IO/Memory/Bus
        call    write_pci_dword_far

        mov     dx, (19 shl 3) + 2              ;
        mov     ah, 10h                         ; Get Bar address
        call    read_pci_dword_far              ; in EBX

        call    USBWorkaroundForConnected

        mov     dx, (19 shl 3) + 2              ;
        mov     ah, 0c4h
        call    read_pci_dword_far
        or      ebx, 03h                        ; Set to D3 state
        call    write_pci_dword_far

        popad
        ret
USBConnectWorkaround ENDP

USBWorkaroundForConnected PROC NEAR
        push    es
        push    0
        pop     es
        add     ebx, 64h                        ; Get first USB port
        mov     cx, 6
@@:
        mov     eax, es:[ebx]
        test    eax, BIT13 + BIT0               ; Check port empty or not
        jnz     SkipWR
        or      eax, BIT13                      ; Set to OHCI
SkipWR:
        or      eax, BIT21+ BIT22               ; Enabled wake by connected/disconnect
        or      es:[ebx], eax

        add     ebx, 4
        loop    @b
        pop     es
        ret
USBWorkaroundForConnected ENDP
```

End of Sample code (Erratum # 23)

Appendix B: Revision History

Date	Revisions	Description
July, 2012	3.02	• Added new section 6.22 Disable Async QH Cache.
Dec 22, 2011	3.01	• Updated section 2.4 C-State and VID/FID Change. • Added new section 2.6 MTC1e and FID VID Setting. • Updated section 3.2 SPI Bus.
Nov, 2010	3.00	• Released as public version. • Updated section 2.4 C-State and VID/FID Change: Added stutter time info for different conditions. • Modified/combined previous section 2.26 and 2.27 to remove support for ASF, but indicating that SMBUS 1 can still be used as a master for SMBUS devices. • Removed previous section 2.34 PM_TURN_OFF_MSG during ASF Shutdown. • Merged previous section 2.42 Automatic Stutter Timer into section 2.5 Enable C1e Stutter Timer and Limit Link Disconnect to < 20 ms. • Added section 2.40 Programmable Interrupt Controller Arbitration. • Added section 2.41 HPET MSI Setting. • Added section 2.42 SMAF Matching Setting. • Updated section 6.19 USB Controller DMA Read Delay Tolerant. • Added Disable AHCI enhancement to section 7.2 SATA Initialization. • Updated section 7.11 SATA MSI and D3 Power State Capability to include that SATA MSI capability is not supported. • Update section 9.1 Disable Second IDE MSI Capability.
Sep 11, 2009	2.13	• Changed heading of section 2.36 from “SMBUS Write Sequence” to “SMBUS Sequence” implying it now applies to both Read and Write. Also added recommended time out of 1 ms or greater. • Updated section 2.38 Unconditional Shutdown - clarified how to write to register • Added new section 2.43 LDT_PWRGD De-assertion with SLP_S3#.
July15, 2009	2.12	• Removed section 1.2 “Feature List”. • Updated section 2.5 “Enable C1e Stutter Timer and Limit Link Disconnect to < 20 ms” • Added section 2.6 “C1e Exit on Assertion of IDLE Exit# (for A15 Only)”. • Added section 2.7 “Support for Entering C1e on HALT# Message (for a15 Only)”. • Updated section 2.32 “Alternate Pin for 14 MHz Clock Input”. • Added section 2.40 “Supporting IDLE_EXIT# from CPU”. • Added section 2.41 “Supporting HALT Message to Generate C1e”. • Added section 2.42 “Automatic Stutter Timer”. • Removed previous section 7.12 “Flash Controller” and section 7.13 “Restoring FC Registers after S3 Resume State”.
June 04, 2009	2.11	• Updated section 2.4“C-State and VID/FID Change” to cover new generation CPU. • Added new section 2.5 “Enable C1e Stutter Timer to Limit Link Disconnect to < 16 ms” • Updated section 6.2 “USB Device Support to Wake Up System from S3/S4 State”. • Moved section 6.17.1 “Sample Code for the Workaround Described in SB7xx Erratum #11” into new Appendix A. • Section 7.2 “SATA Initialization”: Added a new setting to the end of the table. • Removed original section 7.4 “SATA Power Saving” since the block level power saving function in SB7x0 is built-in and the register SMBUS_0xAC[13] is not for this purpose. • Updated section 7.9 “Internal and External SATA Ports Indication Registers”: Added description of internal SATA (iSATA) port(s). • Added new Appendix A: Sample Codes for BIOS Workarounds.
April 29, 2009	2.10	• General edits. • Corrected section 7.4 “SATA Power Saving”

April 27, 2009	2.09	• Added ASIC revision A15 settings. • General replacement of “A14” with “A14 and above”. • Section 2.4 “C-State and VID/FID Change “: Updated description for PM_IO 0x8B. • Section 2.16 ”PCIe® Native Mode”: Changed setting from 1 to 0 for PM_IO 0x84[1]; added suggested settings. • Updated section 2.20 “IMC Access Control” • Updated section 2.28 “Revision ID”. • Added new section 2.34 “Software Clock Throttle Period”. • Added new section 2.35 “Unconditional Shutdown”. • Added new section 2.36 “Watchdog Timer Resolution” • Updated section 4.16 “SMI IO Write”. • Added new section 4.17 “Reset CPU on Sync Flood”. • Added new section 4.18 “Enabling Posted Pass Non-Posted Downstream”. • Added new section 4.19 “Enabling Posted Pass Non-Posted Upstream”. • Added new section 4.20 “64-bit Non-posted Memory Write”. • Updated new section 6.20 “Async Park Mode”. • Added new section 6.24 “USB PID_Error_Checking”. • Updated section 7.9 “Restoring SATA Registers after S3 Resume State” with 2 new settings for SATA Capability. • Section 7.10 “External SATA Ports Indication Registers”: Added definition of HCAP.SXS and Set Px.CMD.HPCP=0 for iSATA. • Changed title of section 7.12 from “SATA MSI Capability” to “SATA MSI and D3 Power State Capability” and updated the section.
Feb 09, 2009	2.08	• Updated section 2.4, “C-State and VID/FID Change”: Distinguished StutterTime for Family 10h and non-10h CPUs. • Updated section 2.13, “Legacy DMA Pre-fetch Enhancement”: Added 2 new settings. • Updated section 2.16, “PCIE Native Mode”: Changed setting for PM_IO 0x84 [1] from 0 to 1. • Updated section 2.28, “Revision ID”: Corrected applicable ASIC revision to A12 and added Rev ID for A14. • Added section 2.29, “Alternate Pin for 14 MHz Clock Input”. • Added section 2.30, “Gevent2 as GPIO.” • Added section 2.31, “PM_TURN_OFF_MSG during ASF Shutdown.” • Added section 2.32, “SMBUS Block Write Filtering.” • Added section 4.15, “Selecting LPC FRAME# Assertion Timing Power-up.” • Updated section 4.5, “OHCI Prefectch Settings.” • Updated section 6.1, “Enabling/Disabling OHCI and EHCI Controllers“ to correct the ECHI Enable bit assignments. • Updated section 6.10, “OHCI MSI Function Setting”: Corrected heading, and corrected applicable ASIC Revision to “All Revs SP5100” • Updated section 6.11: “EHCI Advance Asynchronous Enhancement”: Added A14 setting for enabling AEE function. • Updated section 6.15, “EHCI Async Park Mode”: Added settings for enabling async park mode for A14. • Added section 6.17.1”Sample Code for the Workaround Described in SB7xx Erratum #11 (ERN # ERA12011). • Added sections 6.18-6.23. • Updated section 7.1, “Enabling SATA.” • Added section 7.2, “SATA Initialization.” • Updated section 7.3, “Disabling SATA.” • Added section 7.4, “SATA Power Saving.” • Updated section 7.9, “Restoring SATA Registers after S3 Resume State”: Updated applicable ASIC revisions for various register settings. • Updated section 7.11, “Aggressive Link Power Management.” • Updated section 7.12, “SATA MSI Capability”: • Updated section 7.13, “Flash Controller” by adding a note to indicate FC is not supported at platform level. • Added section 7.15, “Disabling CCC (Command Completion Coalescing) Support”: • Updated section 9.1, “Disabling IDE MSI Capability”: Added setting for making MSI capability visible.

September 11, 2008	2.07	• Replaced codename SB700S with SP5100 throughout the document. • Added section 2.2: Unblocked SMI command port. • Replaced previous section 2.9: Enabling IRQ1/12 Filtering with new section 2.10: Interrupt Routing/Filtering. • Removed previous section 2.28: Reverting USBCLK/14M_25M_48M_OSC Back to A11 Mode. • Added new section 2.29: SMBus Write Sequence. • Updated section 4.12: Enabling AB and BIF Clock Gating. Changed setting for ABCFG 0x54[24] to 0. • Added section 6.16: MSI Feature in USB 2.0 Controller. • Added section 6.17, EHCI Dynamic Clock Gating Feature. • Added section 7.9: Disabling Aggressive Link Power Management. • Added section 7.10: Disabling SATA MSI Capability.
March 05, 2008	1.02	• Updated section 2.9: Enabling IRQ1/12 Filtering by updating the description for register setting Smbus_PCI_config 0x62 [1:0]. • Added section 6.15: EHCI Async Park Mode.
February 08, 2008	1.01	• Updated section 2.15: PCIe Native Mode by updating the descriptions and adding registers to the PCIe Native Mode table. • Added section 2.16: Hardware Monitor. • Added section 2.17: Cir Interrupt Config. • Added section 2.18: SM Pci Config. • Added section 2.19: IMC Access Control • Added section 2.20: CPU Reset. • Added section 3: LPC Controller (bus-0, dev-20, fun-3). • Updated section 4.15: SMI IO Write by changing the title of this section and by updating the register description. • Added section 7.8: External SATA Ports Indication Registers.
May 07, 2007	1.00	• Initial OEM release.