TYAN®

S8230

Version 1.0

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Notice

Contents

Before you begin…

Check the box contents!

The retail motherboard package should contain the following:

	1x S8230 Motherboard
	6 x Serial ATA Cable
	1 x USB2.0 cable
	1 x S8230 User's manual
	1 x S8230 Quick reference guide
	1 x TYAN® Driver CD
	1 x I/O shield
	2 x mini SAS Cable

Chapter 1: Instruction

1.1 Congratulations

You have purchased the powerful TYAN® S8230 motherboard, based on the AMD® SP5100 chipset. The S8230 is designed to support dual AMD® 45nm 8-Core/12-Core Opteron 6100 Series Processors and up to 256GB of 800, 1066 and 1333MHz UNB or REG/ECC DDR3 memory, as well as low-voltage DDR3 memory modules. Leveraging advanced technology from AMD®, the S8230 is capable of offering scalable 32 and 64-bit computing, high-bandwidth memory design, and lightning-fast PCI-E bus implementation.

The S8230 not only empowers you in today's demanding IT environment but also offers a smooth path for future application upgradeability. All of these rich feature sets provides the S8230 with the power and flexibility to meet demanding requirements for today's IT environments.

Remember to visit the TYAN® website at **http://www.tyan.com**. There you can find all the information on all TYAN® products as well as all the supporting documentation, FAQs, Drivers and BIOS upgrades.

1.2 Hardware Specifications

Processor	**Supported CPU Series**	AMD 45nm 8-Core/12-Core Opteron 6100 Series Processors (Magny-Cours)
	Socket Type / Q'ty	G34 1944-pin / (2)
	Average CPU Power (ACP) wattage	Up to 105W
	System Bus	Up to 6.4 GT/s Hyper-Transport link support / (4) HT3; 12MB L3 per socket
Chipset	**Chipset**	AMD SR5690 (5670) + SP5100
	Super I/O	Winbond W83627
Memory	**DIMM slot Qty**	(8)+(8) DIMM slots
	DIMM Type / Speed	U/RDDR3 & LV RDDR3, 800/1066/1333MHz
	Capacity	Up to 256GB
	Memory channel	4 Channels per CPU
	Memory voltage	1.35V/ 1.5V
Expansion Slots	**PCI-E**	(1) PCI-E Gen.2 x8 slot (w/ x4 link) (1) PCI-E Gen.2 x8 slot (1) PCI-E Gen.2 x16 slot (w/ x16 or x8 link) (1) PCI-E Gen.2 x8 slot (w/ x0 or x8 link)
	PCI	(2) PCI 32-bit slots

Recommended Barebones / Chassis	1U Barebones		GT62-B8230-LE
LAN	Port Q'ty		(4)
	Controller		(2) Intel 82574L / (2) Intel 82576EB
Storage	SAS	Connector	(2) Mini-SAS connectors (support 4 HDD's/cable)
		Controller	LSI SAS2008 (for S8230WGM4NR and S8230WGM4NR-LE only)
		Speed	6.0 Gb/s
		RAID	RAID 0/1/1E/10 (LSI Integrated RAID)
	SATA	Connector	(6) SATA
		Controller	AMD SP5100
		Speed	3.0 Gb/s
		RAID	RAID 0/1/10/5 (Promise Integrated RAID)
Graphic	Connector type		D-Sub 15-pin
	Resolution		1600x1200@60Hz
	Chipset		Aspeed AST2050
Input /Output	USB		(6) USB2.0 ports (2 at rear, 2 via cable, 2 Vertical [Type A] onboard)
	COM		(2) ports (1 at rear, 1 via cable)
	SAS		(2) Mini-SAS (4-in-1) connectors
	VGA		(1) D-Sub 15-pin VGA port
	RJ-45		(4) GbE ports
	Power		ATX12V / Universal 24-pin + 8-pin + 8-pin power connectors
	Front Panel		(1) 2x12-pin SSI front panel header
	SATA		(6) SATA-II connectors
System Monitoring	Chipset		Winbond W83793G
	Voltage		Monitors voltage for CPU, memory, chipset & power supply
	Fan		(12) Total ((7) 4-pin headers + (5) 8-pin headers)
	Temperature		Monitors temperature for CPU & system environment
	LED		Fan fail LED indicator / Over temperature warning indicator / Fan & PSU fail LED indicator
	Others		Watchdog timer support
Server Management	Onboard Chipset		Onboard Aspeed AST2050
	AST2050 IPMI Feature		IPMI 2.0 compliant baseboard management controller (BMC) / USB 2.0 virtual hub
	AST2050 iKVM Feature		24-bit high quality video compression / Dual 10/100 Mb/s MAC interfaces
BIOS	Brand / ROM size		AMI / 4MB

	Feature	Plug and Play (PnP) /PCI2.3 /WfM2.0 /SMBIOS2.3 /PXE boot / ACPI 2.0 power management /Power on mode after power recovery / User-configurable H/W monitoring
Physical Dimension	**Form Factor**	E-ATX
	Board Dimension	12"x13" (305x330mm)
Operating System	**OS supported list**	Please visit our web site for the latest update.
Regulation	**FCC (DoC)**	Class B
	CE (DoC)	Yes
Operating Environment	**Operating Temp.**	10° C ~ 35° C (50° F~ 95° F)
	Non-operating Temp.	- 40° C ~ 70° C (-40° F ~ 158° F)
	In/Non-operating Humidity	90%, non-condensing at 35° C
RoHS	**RoHS 6/6 Complaint**	Yes
Package Contains	**Motherboard**	(1) S8230 Motherboard
	Manual	(1) User's manual / (1) Quick Ref. Guide
	Installation CD	(1) TYAN installation CD
	I/O Shield	(1) I/O Shield
	Cable — **SATA**	(6) SATA signal cables
	Cable — **SAS**	(2) mini-SAS cables (for S8230WGM4NR and S8230WGM4NR-LE only)
Optional accessories	**Riser Card**	M2091, PCI-E x16 1U riser card (left)

S8230 SKU Comparison Table

	S8230WGM4NR	S8230GM4NR	S8230WGM4NR-LE	S8230GM4NR-LE
AMD SR5690	Yes	Yes		
AMD SR5670			Yes	Yes
AMD SP5100	Yes	Yes	Yes	Yes
BMC (AST2050)	Yes	Yes	Yes	Yes
LSA2008 SAS	Yes		Yes	
Memory DIMM	16	16	16	16
PCIE Slots	4	4	2	2
VGA	Yes	Yes	Yes	Yes
COM	Yes	Yes	Yes	Yes
SATAII Ports	6	6	6	6

1.3   Software Specifications

For OS (operation system) support, please check with TYAN® support for latest information.

Remember to visit our Web site at http://www.tyan.com for the latest AST2050 User's Guide.

Chapter 2: Board Installation

You are now ready to install your motherboard.

How to install our products right… the first time

The first thing you should do is reading this user's manual. It contains important information that will make configuration and setup much easier. Here are some precautions you should take when installing your motherboard:

(1) Ground yourself properly before removing your motherboard from the antistatic bag. Unplug the power from your computer power supply and then touch a safely grounded object to release static charge (i.e. power supply case). For the safest conditions, MiTAC recommends wearing a static safety wrist strap.

(2) Hold the motherboard by its edges and do not touch the bottom of the board, or flex the board in any way.

(3) Avoid touching the motherboard components, IC chips, connectors, memory modules, and leads.

(4) Place the motherboard on a grounded antistatic surface or on the antistatic bag that the board was shipped in.

(5) Inspect the board for damage.

The following pages include details on how to install your motherboard into your chassis, as well as installing the processor, memory, disk drives and cables.

> **NOTE:** Do not apply power to the board if it has been damaged.

2.1 Board Image
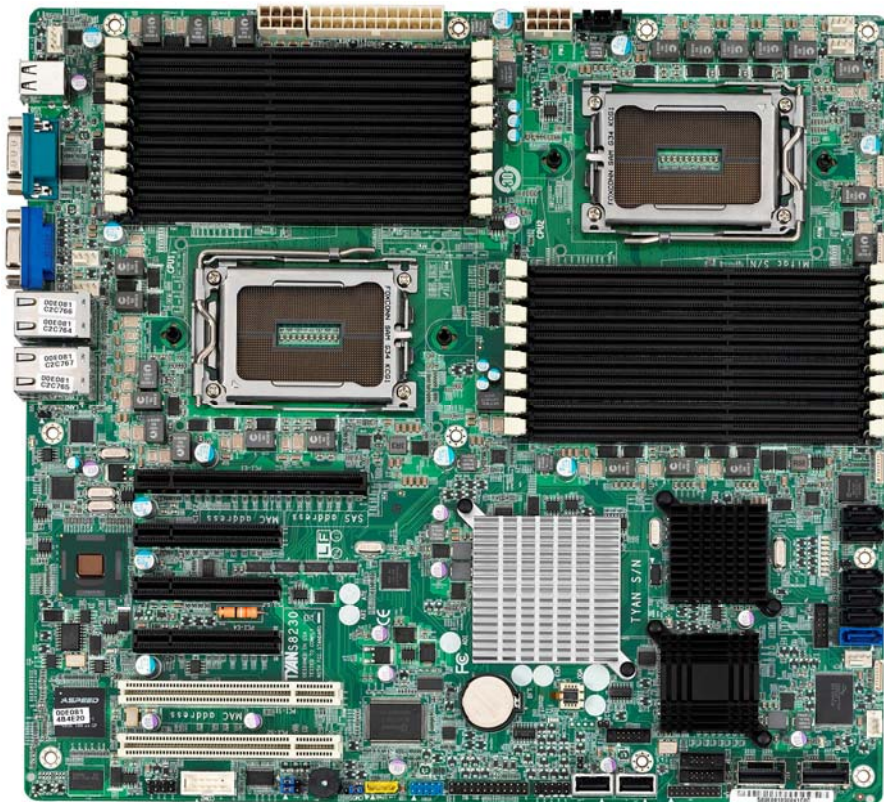
This picture is representative of the latest board revision available at the time of publishing. The board you receive may not look exactly like the above picture.

2.2 Block Diagram
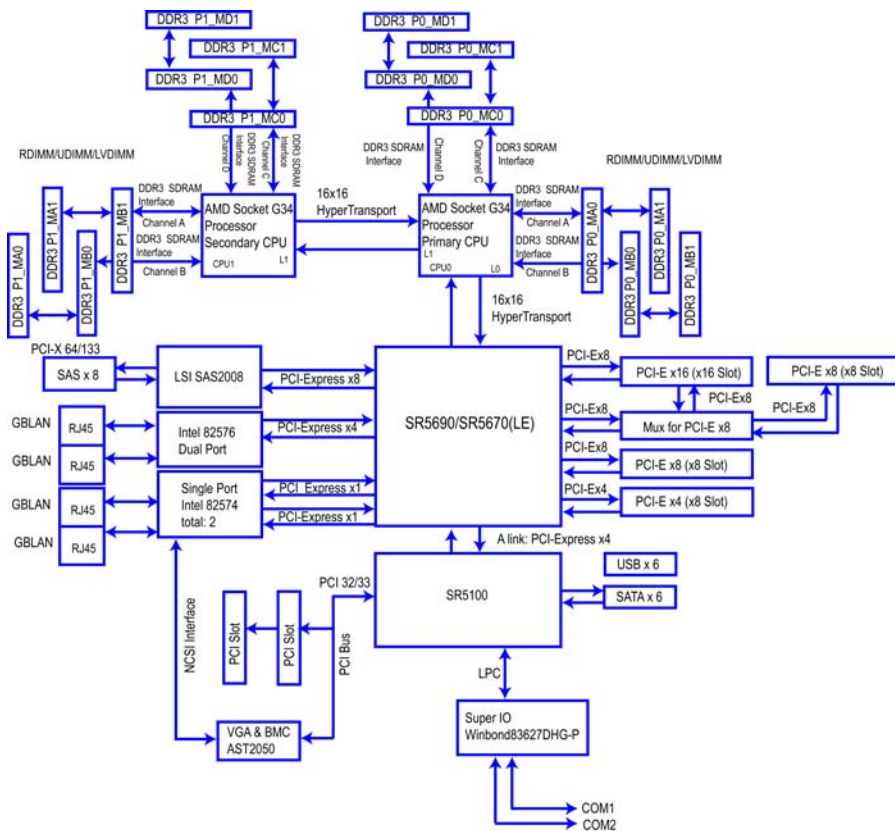
S8230 Block Diagram

2.3 Board Parts, Jumpers and Connectors
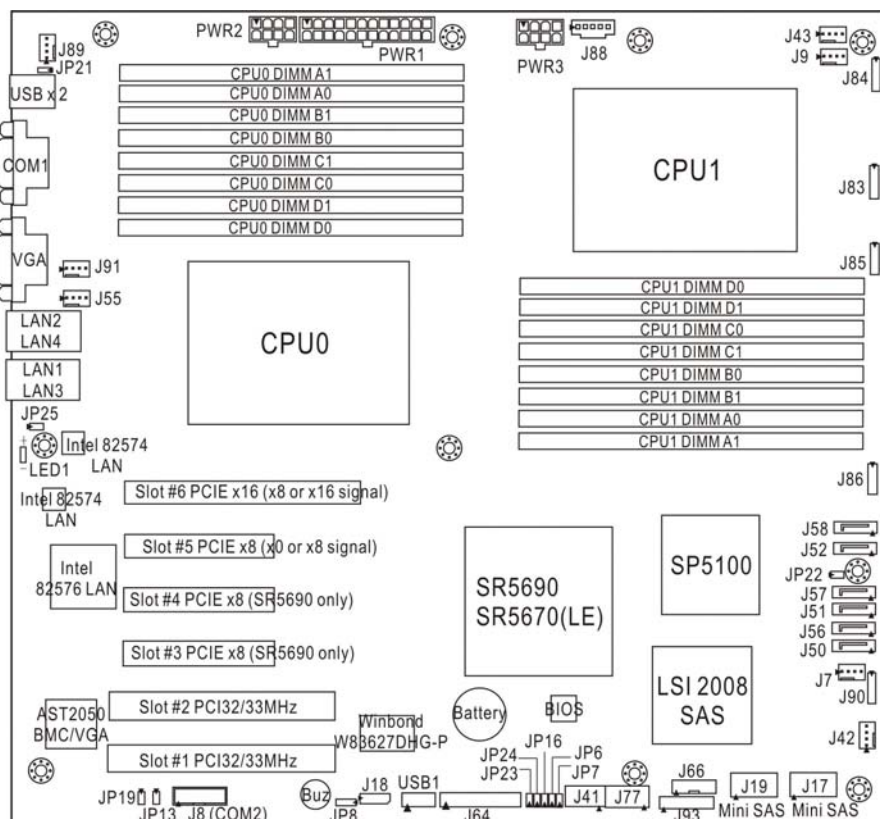
This diagram is representative of the latest board revision available at the time of publishing. The board you receive may not look exactly like the above diagram. But for the DIMM number please refer to the above placement for memory installation. For the latest board revision, please visit our web site at http://www.tyan.com.

Jumpers & Connectors

Jumper/Connector	Function
J7/J42/J43/J89/J91	4-pin Fan Connectors
J83/J84/J85/J86/J90	8-pin 4056 FAN Connector (Barebones use only)
J55/J9	4-pin CPU0/CPU1 Fan Header
J93	2x10 pin Fan Connector (Barebones use only)
J8 (COM2)	COM2 Header
J17/J19	Mini-SAS Connector
J18	IPMB Connector
J41/J77	Vertical [Type A] USB Connectors
J50/J56/J51/J57/J52/J58	SATA0/SATA1/SATA2/SATA3/SATA4/SATA5
J64	Front Panel Connector
J66	SAS Fault LED
J88	PSMI Connector
LED1	ID LED
USB1	USB Front Panel Header
JP6	SAS Enable/Disable Jumper
JP7	PCI-E Width Switch for Slot5 and Slot 6
JP8	Clear CMOS Jumper
JP16	Chassis Intrusion Header
JP19	BMC VGA Enable/Disable Jumper
JP21	CPU0 Memory Voltage Select Jumper
JP22	CPU1 Memory Voltage Select Jumper
JP23	LAN4 Active LED
JP24	LAN2 Active LED
JP25	ID LED Header

Jumper Legend

▪ ▪	**OPEN - Jumper OFF**	Without jumper cover
▪ ▪	**CLOSED - Jumper ON**	With jumper cover

J7/J42/J43/J89/J91: 4-Pin FAN Connectors

Pin	1	2	3	4
Signal	GND	+12V	Tachometer	PWM Control
Use this header to connect the cooling fan to your motherboard to keep the system stable and reliable.				

J55/J9: 4-pin CPU0/CPU1 Fan Connectors

Pin	1	2	3	4
Signal	GND	+12V	Tachometer	Fan PWM (Speed) Control

J83/J84/J85/J86/J90: 8-pin 4056 Fan Header (Barebones use only)

Signal	Pin	Pin	Signal
PWM1	**1**	**2**	+12V
TACH1	**3**	**4**	GND
GND	**5**	**6**	TACH2
+12V	**7**	**8**	PWM2
NOTE: Do not mix 8-pin Fan headers with 4-pin Fan headers. Mixing these fan headers will cause problems to the system.			

J93: 2x10-Pin FAN connector for TYAN (Barebones use only)

Signal	Pin	Pin	Signal
FANIN1	**1**	**2**	FANIN6
FANIN2	**3**	**4**	FANIN7
FANIN3	**5**	**6**	FANIN8
FANIN4	**7**	**8**	FANIN9
FANIN5	**9**	**10**	FANIN10
GND	**11**	**12**	KEY
FANCTL5	**13**	**14**	FANCTL4
FANIN11	**15**	**16**	N/C
FANIN12	**17**	**18**	N/C
N/C	**19**	**20**	FANCTL7

J18: IPMB Connector

Signal	Pin	Pin	Signal
IPMB_DATA	**1**	**2**	GND
IPMB_CLK	**3**	**4**	N/C
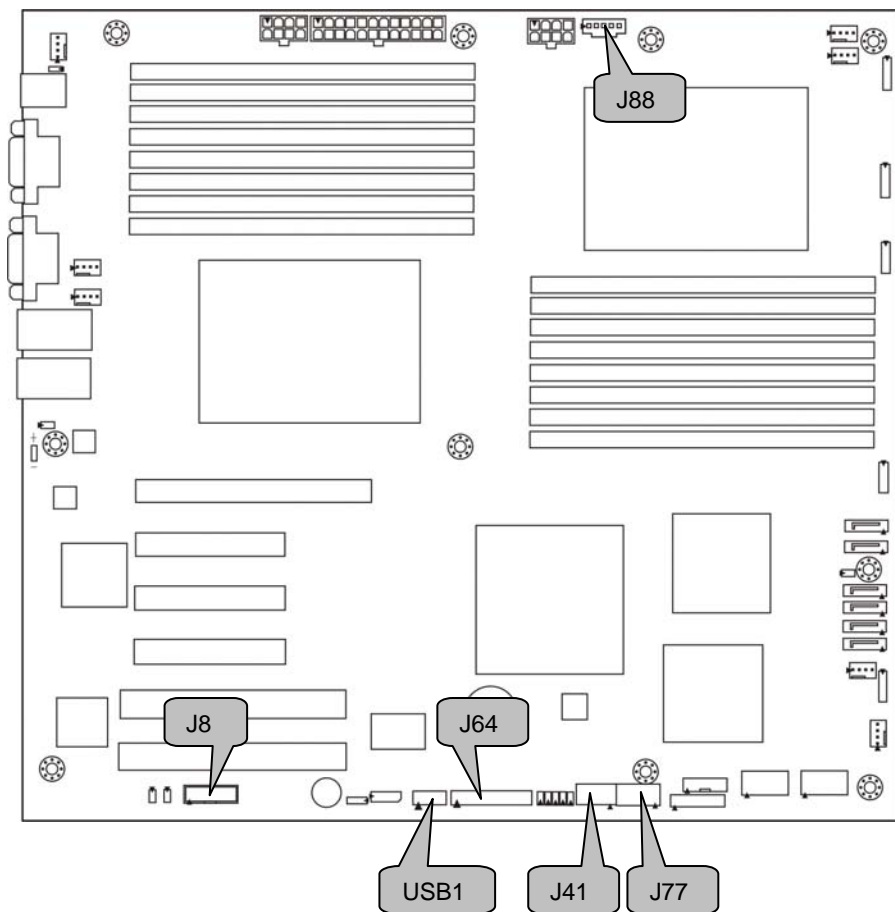
USB1: USB Front Panel Connector

	Signal	Pin	Pin	Signal
	PWR_5V	1	2	PWR-5V
	USB_N1	3	4	USB_N2
	USB_P1	5	6	USB_P2
	GND	7	8	GND
	KEY	9	10	N/C

J41/J77: Vertical (Type A) USB Connectors

	Pin	1	2	3	4
	Signal	+5V	USB D-	USB D+	GND

J88: PSMI Connector

	Pin	1	2	3	4	5
	Signal	SMB_CLK	SMB_DAT	SMBALERT	GND	V3P3

J64: TYFP1 Connector
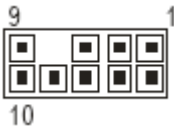
	Signal	Pin	Pin	Signal
	Power LED+	1	2	PWR
	KEY	3	4	System ID LED+
	Power LED -	5	6	System ID LED-
	HD LED+	7	8	Fault LED
	HD LED -	9	10	PSU Fault LED
	Power SW	11	12	LAN1 LED +
	GND	13	14	LAN1 LED -
	Reset SW	15	16	SMB Host Data
	GND	17	18	SMB Host CLK
	ID SW	19	20	INTRU#
	TEMP Sensor	21	22	LAN3 LED +
	NMI	23	24	LAN3 LED -

J8: COM2 Connector

	Signal	Pin	Pin	Signal
	DCD	1	2	DSR
	RXD	3	4	RTS
	TXD	5	6	CTS
	DTR	7	8	RI
	GND	9	10	KEY
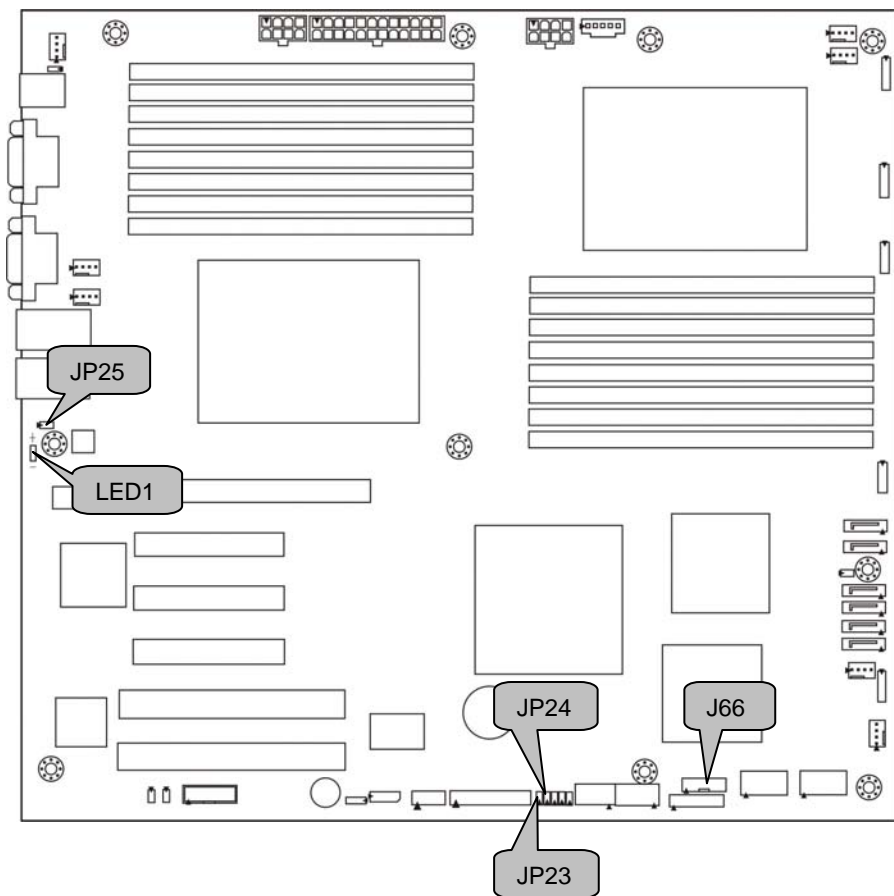
J66: SAS Fault LED

	Use this header to connect to the CPLD firmware update tool			
	Signal	Pin	Pin	Signal
	SAS Fault LED 0	1	2	SAS Fault LED 1
	SAS Fault LED 2	3	4	SAS Fault LED 3
	SAS Fault LED 4	5	6	SAS Fault LED 5
	KEY	7	8	SAS Fault LED 7
	SAS Fault LED 6	9	10	Ground

JP23: LAN4 LED Header

	Pin	Signal
	1	LAN4 LED+
	2	LAN4 LED-

JP24: LAN2 LED Header

	Pin	Signal
	1	LAN2 LED+
	2	LAN2 LED-

JP25: ID LED Header
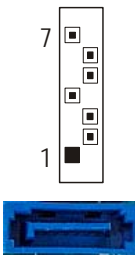
	Pin	Signal
	1	ID LED+
	2	ID LED-

LED1: ID LED

	Pin	Signal	
	+	P3V3_AUX	
	-	ID_SW_L	
	State	Color	Description
	On	Blue	System identified
	Off	Off	System not identified
	NOTE: IPMI can activate ID LED from remote site. Please visit the TYAN Web Site at **http://www.tyan.com** to download the latest AST2050 Software Configuration Guide for IPMI settings.		
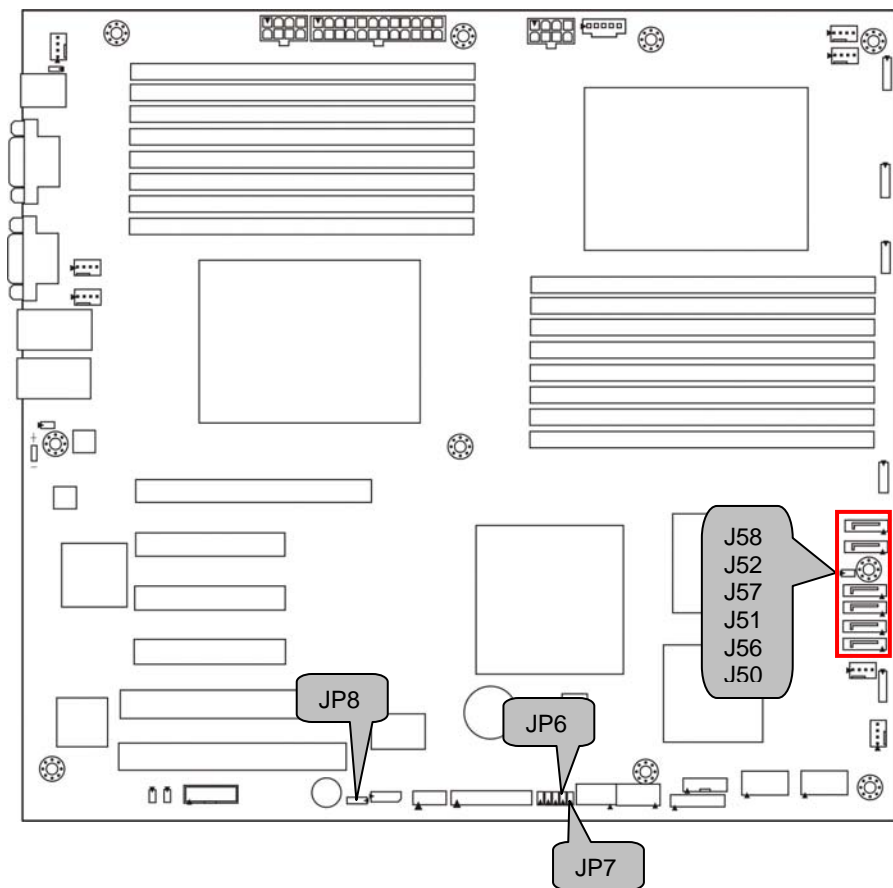
J50/J56/J51/J57/J52/J58: SATA Connector

Pin	Signal	
7	GND	Connects to the Serial ATA ready drives via the Serial ATA cable.
6	RXP	
5	RXN	
4	GND	
3	TXN	
2	TXP	
1	GND	

SATA0: J50	SATA1: J56
SATA2: J51	SATA3: J57
SATA4: J52	SATA5: J58

JP6: SAS Enable/Disable Jumper

■■	Open: Normal (**Default**)
■■	Closed: Disable on-board SAS function

JP7: PCIE Switch for Slot #6 (PCI-E1) and Slot #5 (PCI-E2)

■■	Open: Normal(**Default**) **NOTE:** If there is no device in PCI-E2, then PCI-E1 can support up to a x16 PCI-E signal. If there is a device in PCI-E2 then PCIe1 can only support up to x8 PCI-E signal
■■	Closed: Force PCI-E1 to max x8 PCI-E signal

JP8: Clear CMOS Jumper

■ ■ ■ 1 Normal (**Default**)	You can reset CMOS by using this jumper if you have forgotten your system/setup password or need to clear BIOS setting. 1. Power off system and disconnect both power connectors from the motherboard. 2. Put jumper cap back to Pin_1 and Pin_2 (default setting). 3. Use jumper cap to close Pin_2 and Pin_3 for seconds to Clear CMOS. 4. Reconnect power & power on system.
■ ■ ■ 1 Clear CMOS	

JP21

JP22

JP19
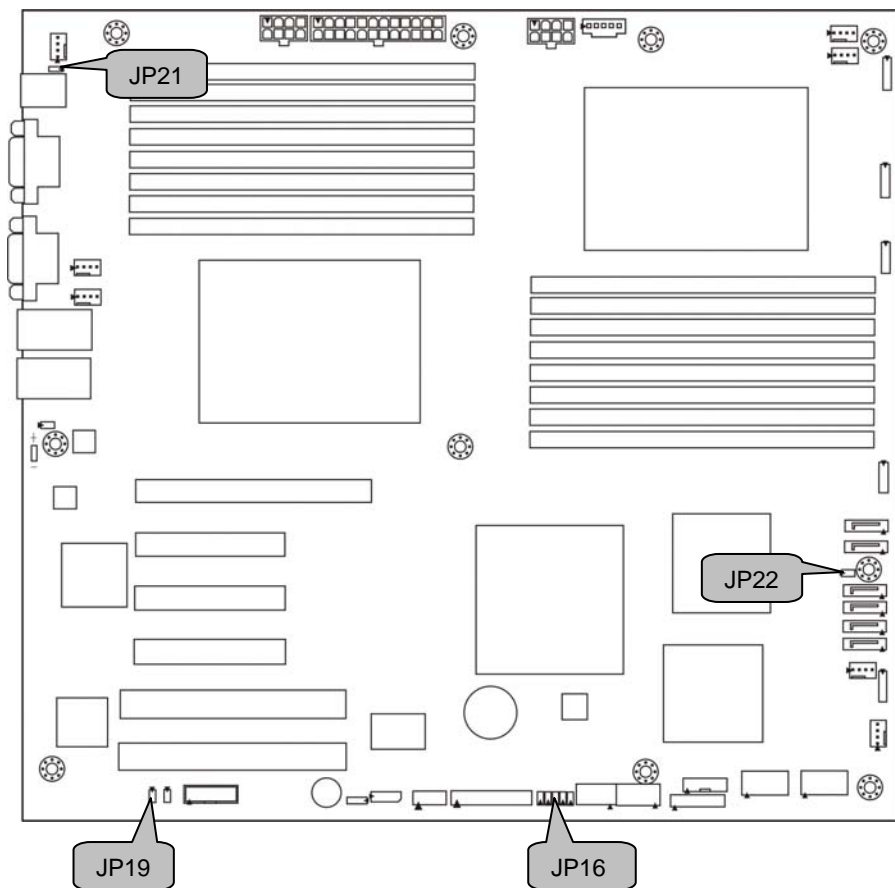
JP16

JP16: Chassis Intrusion Header

		Pin	Signal
1 ▣▣	Open: Use this jumper to **disable** the system chassis intrusion alarm.	**1**	INTRUDER#
▣▣	Closed: Use this jumper to **trigger** the system chassis intrusion alarm. (**Default**)	**2**	GND

JP19: BMC VGA Enable/Disable Jumper

▣▣	Open: Normal (**Default**)
▣▣	Closed: Disable onboard VGA function.

JP21: Low Voltage (1.35V) DDR3 Enable/Disable for CPU0 Jumper

▣▣	Open: Support regular 1.5V DDR3 memory (**Default**)
▣▣	Closed: Support for Low Voltage 1.35V DDR3 memory

JP22: Low Voltage (1.35V) DDR3 Enable/Disable for CPU1 Jumper

▣▣	Open: Support regular 1.5V DDR3 memory (**Default**)
▣▣	Closed: Support for Low Voltage 1.35V DDR3 memory

2.4 Installing the Processor and Heat sink

The S8230 supported AMD$^®$ processors are listed in section **1.2   Hardware Specifications** on page 4. Check our website at **http://www.tyan.com** for latest processor support.

> **NOTE:** MiTAC is not liable for damage as a result of operating an unsupported configuration.

Processor Installation (G34 1944-pin Socket for AMD CPU)

Follow the steps below to install the processors and heat sinks.

1.   Locate the CPU socket.

2.   Pull the CPU lever slightly away from the socket and then push it to a fully open position.
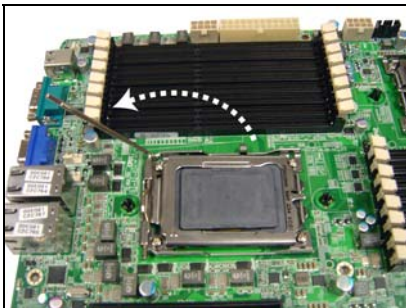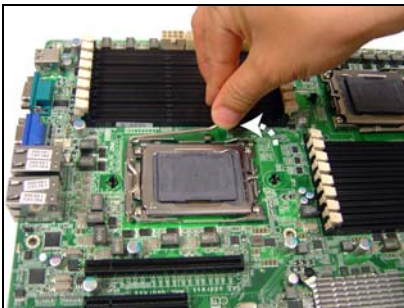
3. Lift the socket cover to a fully open position.
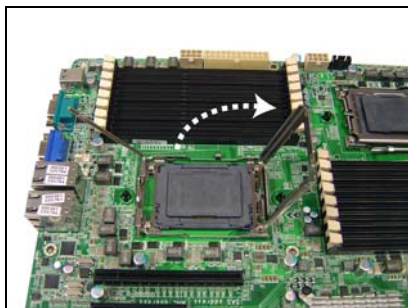
4. Take off the CPU protection cap.
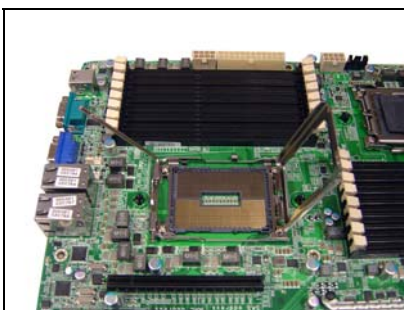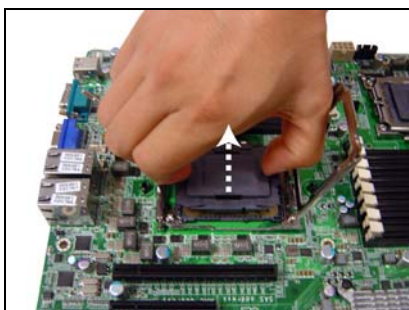
5. Place the CPU in the CPU socket.

6.   Close the socket cover and press the CPU socket lever down to lock the CPU in place.
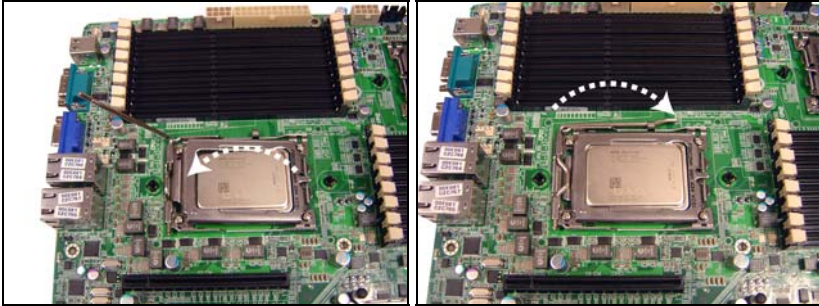
7.   Repeat the same procedures to install the second CPU.

Heat sink Installation

After installing the processor, you should proceed to install the heat sink. The CPU heat sink will ensure that the processor do not overheat and continue to operate at maximum performance for as long as you own them. The overheated processor is dangerous to the motherboard.

For the safest method of installation and information on choosing the appropriate heat sink, using heat sinks validated by AMD®. Please refer to the AMD® website: **http://www.amd.com**

The following diagram illustrates how to install heat sink onto the CPU of S8230.
8.   Place the heat sink on top of the CPU and secure it to the motherboard with 2 screws.

9.   Connect the heat sink Fan cable to the CPU0 FAN connector J55.
10. Repeat the same procedures to install the second heat sink (CPU1 FAN Connector J9).

2.5 Thermal Interface Material
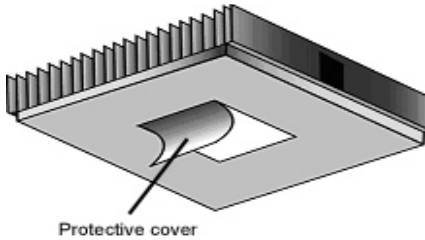
There are two types of thermal interface materials designed for use with the processors.

Protective cover

The most common material comes as a small pad attached to the heat sink at the time of purchase. There should be a protective cover over the material. Take care not to touch this material. Simply remove the protective cover and place the heat sink on the processor.

Thermal Compound

Processor Lid
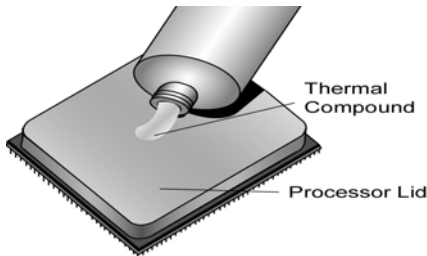
The second type of interface material is usually packaged separately. It is commonly referred to as 'thermal compound'. Simply apply a thin layer on to the CPU lid (applying too much will actually reduce the cooling).

NOTE: Always check with the manufacturer of the heat sink & processor to ensure that the thermal interface material is compatible with the processor and meets the manufacturer's warranty requirements.

2.6 Tips on Installing Motherboard in Chassis
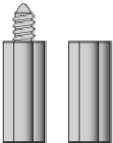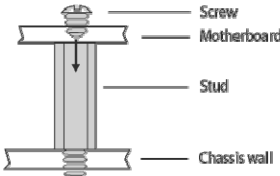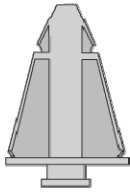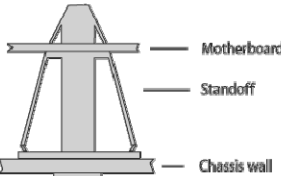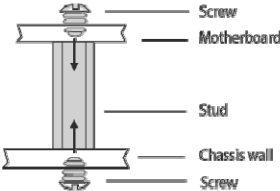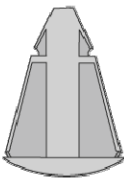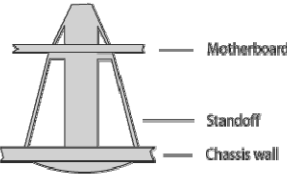
Before installing your motherboard, make sure your chassis has the necessary motherboard support studs installed. These studs are usually metal and are gold in color. Usually, the chassis manufacturer will pre-install the support studs. If you are unsure of stud placement, simply lay the motherboard inside the chassis and align the screw holes of the motherboard to the studs inside the case. If there are any studs missing, you will know right away since the motherboard will not be able to be securely installed.
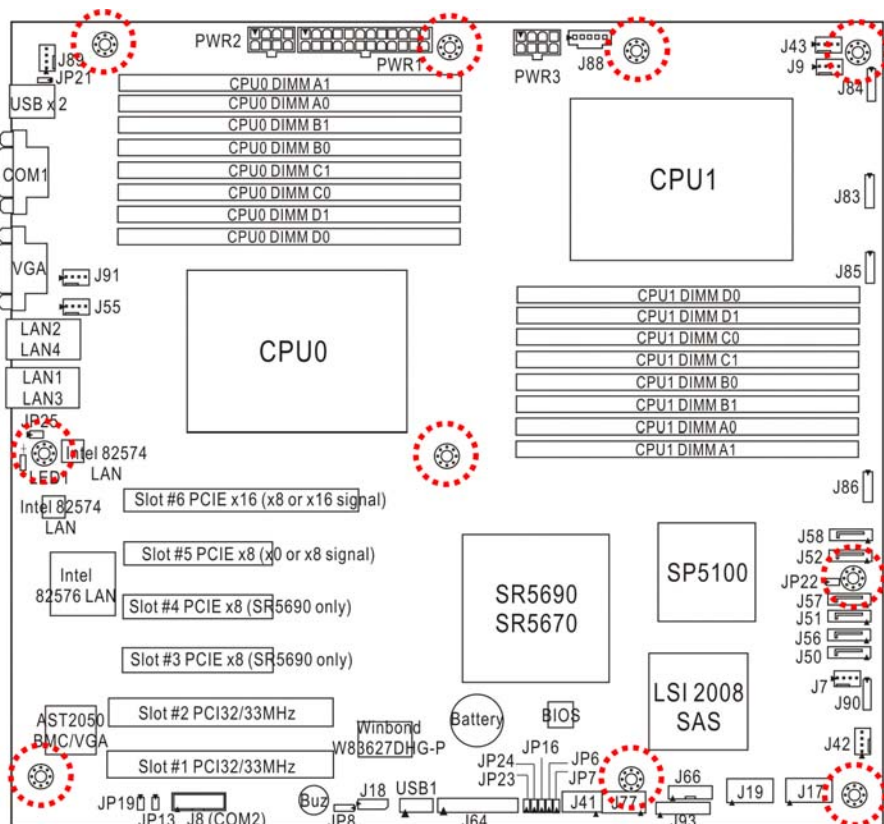
Some chassis include plastic studs instead of metal. Although the plastic studs are usable, MiTAC recommends using metal studs with screws that will fasten the motherboard more securely in place.

Below is a chart detailing what the most common motherboard studs look like and how they should be installed.

Mounting the Motherboard

Type	Solutions for installing	
	Screw Motherboard Stud Chassis wall	Screw Motherboard Stud Chassis wall
	Motherboard Standoff Chassis wall	Screw Motherboard Stud Chassis wall Screw
	Motherboard Standoff Chassis wall	

2.7   Installing the Memory

Before installing memory, ensure that the memory you have is compatible with the motherboard and processor. Check the TYAN Web site at: **www.tyan.com** for details of the type of memory recommended for your motherboard.

The following diagram shows common types of DDR3 memory modules.
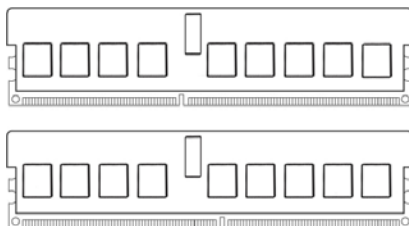
- Supports up to 256GB total of U/RDDR3 and LV RDDR3 at 800,1066 or 1333MHz speeds
- All installed memory will automatically be detected and no jumpers or settings need changing
- All memory must be of the **same type and density**
- Always populate the memory starting from DIMM A1 first

<u>**Recommended Memory Population Table**</u>

Memory Configuration Chart																
	CPU0								CPU1							
# of DIMM'S	Channel 1		Channel 2		Channel 3		Channel 4		Channel 1		Channel 2		Channel 3		Channel 4	
	A1	A0	B1	B0	C1	C0	D1	D0	A1	A0	B1	B0	C1	C0	D1	D0
1 DIMM	X								X							
2 DIMM	X		X						X		X					
4 DIMM	X		X		X		X		X		X		X		X	
8 DIMM	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

U-DIMM Module Support

DDR3 Speed/Voltage		DDR3 Rank Configuration	
1.35v	1.5v	DIMM0 (A0, B0, C0, D0)	DIMM1 (A1, B1, C1, D1)
800MHz	800MHz		SR and DR
800MHz	800MHz	SR and DR	SR and DR
1066MHz	1066MHz		SR and DR
1066MHz	1066MHz	SR and DR	SR and DR
n/a	1333MHz		SR and DR
n/a	1333MHz	SR and DR	SR and DR

Notes:

- UDIMM can support up to 4GB sized DIMM's
- Maximum of 8GB per channel
- SR and DR UDDR3 module support **only**
- SR and DR 1.35v Memory MAX speed of 1066MHz in a dual channel configuration
- SR and DR 1.5v Memory MAX speed of 1333MHz in a dual channel configuration

R-DIMM Module Support

DDR3 Speed/Voltage		DDR3 Rank Configuration	
1.35v	1.5v	DIMM0 (A0, B0, C0, D0)	DIMM1 (A1, B1, C1, D1)
800MHz	800MHz	n/a	SR and DR
800MHz	800MHz	n/a	QR
800MHz	800MHz	SR, DR and QR	SR, DR and QR
1066MHz	1066MHz	n/a	SR and DR
1066MHz	1066MHz	n/a	QR
1066MHz	1066MHz	SR and DR	SR and DR
n/a	1066MHz	QR	SR, DR and QR
n/a	1066MHz	SR, DR and QR	QR
n/a	1333MHz	n/a	SR and DR
n/a	1333MHz	n/a	QR
n/a	1333MHz	SR and DR	SR and DR

Notes:

- RDIMM can support up to 16GB sized DIMM's
- SR and DR Memory has a MAX amount of 16GB per channel
- SR and DR 1.35v Memory MAX speed of 1066MHz in a dual channel configuration
- SR and DR 1.5v Memory MAX speed of 1333MHz in a dual channel configuration
- QR Memory has a MAX amount of 32GB per channel
- QR 1.35v Memory MAX speed of 800MHz in a dual channel configuration
- QR 1.5v Memory MAX speed of 1066MHz in a dual channel configuration
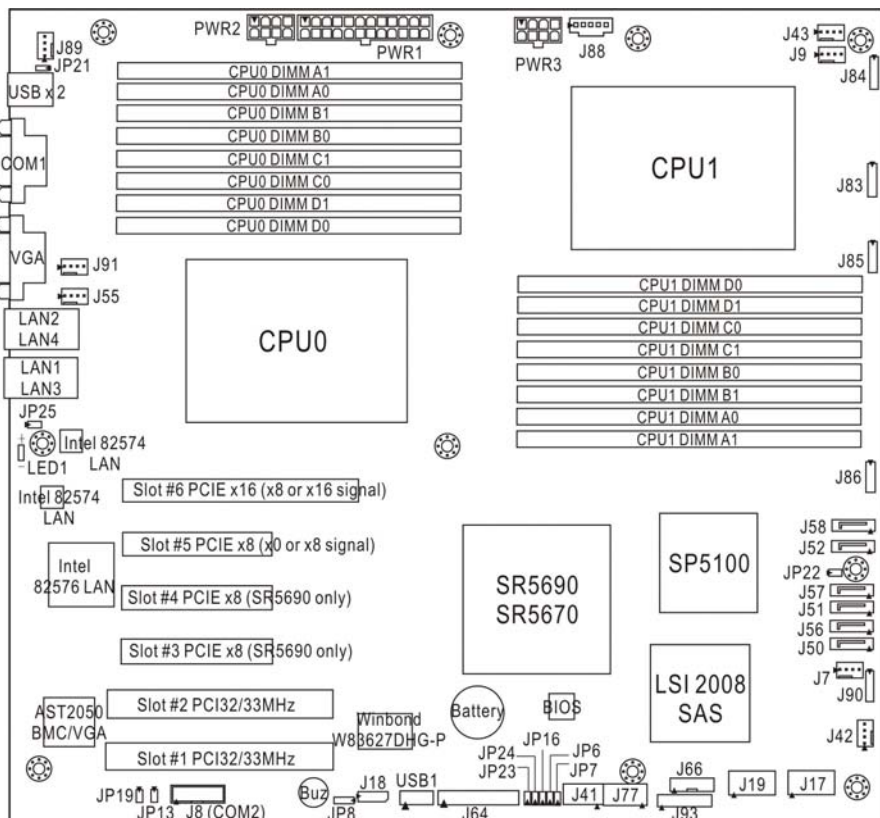
Memory Installation Procedure

Follow these instructions to install memory modules into the S8230.

1.   Press the locking levers in the direction shown in the following illustration.
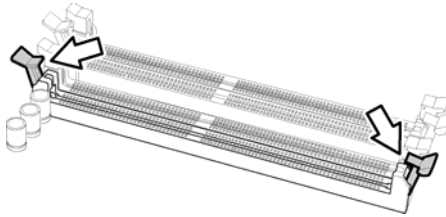
2.   Align the memory module with the socket. The memory module is keyed to fit only one way in the socket.

KEY SLOT
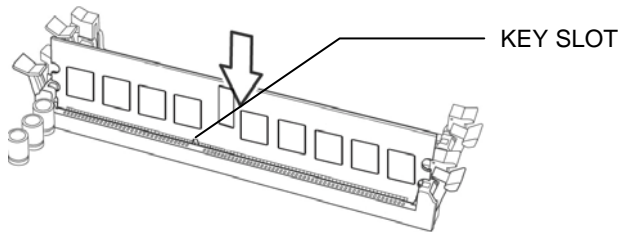
3.   Seat the module firmly into the socket by gently pressing down until it sits flush with the socket. The locking levers pop up into place.
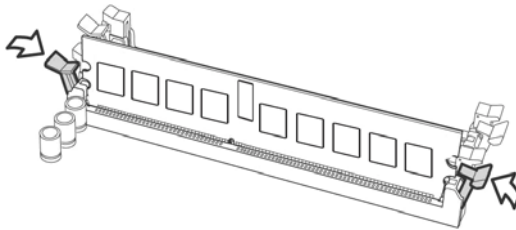
2.8 Attaching Drive Cables

Attaching Serial ATA Cables

S8230 is equipped with 6 Serial ATA (SATA) channels. Connections for the drives are very simple.
There is no need to set Master/Slave jumpers on SATA drives.
If you are in need of SATA/SAS cables or power adapters please contact your place of purchase.

The following pictures illustrate how to connect an SATA drive.

1. SATA drive cable connection

2. SATA drive power connection

3. SATA cable motherboard connector

4. SATA drive power adapter
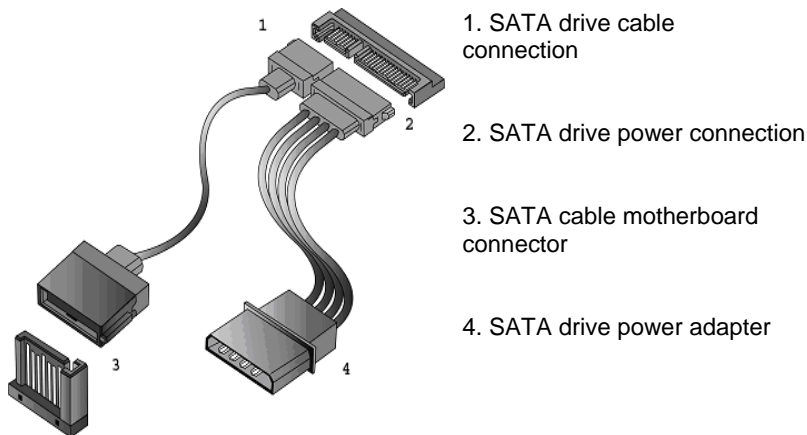
2.9 Installing Add-In Cards

Before installing add-in cards, it's helpful to know if they are fully compatible with your motherboard. For this reason, we've provided the diagrams below, showing the slots that may appear on your motherboard.

PCI-E Gen. 2 x 16 slot (x16 signal)

PCI-E x8 slot (x8 signal)

PCI 32/33MHz slot
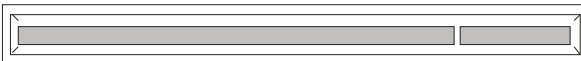
Simply find the appropriate slot for your add-in card and insert the card firmly. Do not force any add-in cards into any slots if they do not seat in place. It is better to try another slot or return the faulty card rather than damaging both the motherboard and the add-in card.

TIP: It's a good practice to install add-in cards in a staggered manner rather than making them directly adjacent to each other. Doing so allows air to circulate within the chassis more easily, thus improving cooling for all installed devices.

NOTE: You must always unplug the power connector to the motherboard before performing system hardware changes to avoid damaging the board or expansion device.

2.10   Connecting External Devices

Connecting external devices to the motherboard is an easy task. The motherboard supports a number of different interfaces through connecting peripherals. See the following diagrams for the details.

Connect to 82576 & LAN LED2   Connect to 82574 & LAN LED3

2 X USB ports   COM Port   VGA Port

Connect to 82574 & LAN LED4   Connect to 82576 & LAN LED1
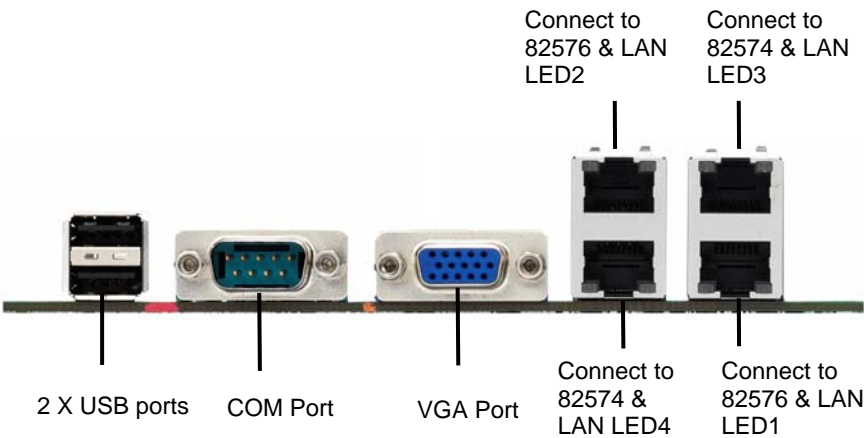
> **NOTE:** Peripheral devices can be plugged straight into any of these ports but software may be required to complete the installation.

Onboard LAN LED Color Definition

The two onboard Ethernet ports have green and yellow LEDs to indicate LAN status. The chart below illustrates the different LED states.

10/100/1000 Mbps LAN Link/Activity LED Scheme		Left LED	Right LED
10 Mbps	**Link**	Green	Off
	Active	Blinking Green	Off
100 Mbps	**Link**	Green	Green
	Active	Blinking Green	Green
1000 Mbps	**Link**	Green	Yellow
	Active	Blinking Green	Yellow
No Link		Off	Off

2.11 Installing the Power Supply

There are three power connectors on your S8230. It is required that you have an EPS12V power supply which has one 24-pin and two 8-pin connectors.
● 24-pin (PW1)

	Signal	Pin	Pin	Signal
	+3.3V	1	13	+3.3V
	+3.3V	2	14	-12V
	GND	3	15	GND
	+5V	4	16	PS_ON
	GND	5	17	GND
	+5V	6	18	GND
	GND	7	19	GND
	PS_GD	8	20	N/C
	5VSB	9	21	+5V
	+12V	10	22	+5V
	+12V	11	23	+5V
	+3.3V	12	24	GND

● 8-pin (PW2, PW3)

	Signal	Pin	Pin	Signal
	GND	1	5	+12V
	GND	2	6	+12V
	GND	3	7	+12V
	GND	4	8	+12V

> **NOTE:** Please be aware that ATX 2.x, ATX12V and ATXGES power supplies may **not** be compatible with the board and can damage the motherboard and/or CPU(s).

Applying power to the board:
● Connect the EPS12V 8-pin power connectors. Both PW2 and PW3 are for CPU loading. With light load processors, such as HE model, one 8-pin connector is OK. With SE model processors, both 8-pin power connectors are required.
● Connect the EPS/12V 24-pin power connector.
● Connect power cable to power supply and power outlet.

> **NOTE:** You must unplug the power supply before plugging the power cables to motherboard connectors.

2.12 Finishing Up

Congratulations on making it this far! You have finished setting up the hardware aspect of your computer. Before closing up your chassis, make sure that all cables and wires are connected properly, especially IDE cables and most importantly, jumpers. You may have difficulty powering on your system if the motherboard jumpers are not set correctly.

In the rare circumstance that you have experienced difficulty, you can find help by asking your vendor for assistance. If they are not available for assistance, please find setup information and documentation online at our website or by calling your vendor's support line.

NOTE

Chapter 3: BIOS Setup

3.1   About the BIOS

The BIOS is the basic input/output system, the firmware on the motherboard that enables your hardware to interface with your software. The BIOS determines what a computer can do without accessing programs from a disk. The BIOS contains all the code required to control the keyboard, display screen, disk drives, serial communications, and a number of miscellaneous functions. This chapter describes the various BIOS settings that can be used to configure your system.

The BIOS section of this manual is subject to change without notice and is provided for reference purposes only. The settings and configurations of the BIOS are current at the time of print and are subject to change, and therefore may not match exactly what is displayed on screen.

This section describes the BIOS setup program. The setup program lets you modify basic configuration settings. The settings are then stored in a dedicated, battery-backed memory (called NVRAM) that retains the information even when the power is turned off.

To start the BIOS setup utility:
1.   Turn on or reboot your system.
2.   Press <Del> during POST (F4 on remote console) to start the BIOS setup utility.

3.1.1   Setup Basics

The table below shows how to navigate in the setup program using the keyboard.

Key	Function
Tab	Moves from one selection to the next
Left/Right Arrow Keys	Changes from one menu to the next
Up/Down Arrow Keys	Moves between selections
Enter	Opens highlighted section
PgUp/PgDn Keys	Changes settings.

3.1.2 Getting Help

Pressing [**F1**] will display a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window, press [**ESC**] or the [**F1**] key again.

3.1.3 In Case of Problems

If you have trouble booting your computer after making and saving the changes with the BIOS setup program, you can restart the computer by holding the power button down until the computer shuts off (usually within 4 seconds); resetting by pressing CTRL-ALT-DEL; or clearing the CMOS.
The best advice is to only alter settings that you thoroughly understand. In particular, do not change settings in the Chipset section unless you are absolutely sure of what you are doing. The Chipset defaults have been carefully chosen either by MiTAC or your system manufacturer for best performance and reliability. Even a seemingly small change to the Chipset setup options may cause the system to become unstable or unusable.

3.1.4 Setup Variations

Not all systems have the same BIOS setup layout or options. While the basic look and function of the BIOS setup remains more or less the same for most systems, the appearance of your Setup screen may differ from the charts shown in this section. Each system design and chipset combination requires a custom configuration. In addition, the final appearance of the Setup program depends on the system designer. Your system designer may decide that certain items should not be available for user configuration, and remove them from the BIOS setup program.

> **NOTE**: The following pages provide the details of BIOS menu. Please be noticed that the BIOS menu are continually changing due to the BIOS updating. The BIOS menu provided are the most updated ones when this manual is written. Please visit TYAN's website at http://www.tyan.com for the information of BIOS updating.

3.2 Main Menu

In this section, you can alter general features such as the date and time.
Note that the options listed below are for options that can directly be changed within
the Main Setup screen.

```
                         BIOS SETUP UTILITY
 Main     Advanced    PCIPnP    Boot    Security    Chipset    Exit

 System Overview                                  Use [ENTER], [TAB]
                                                  or [SHIFT-TAB] to
 AMIBIOS                                          select a field.
 Core      :08.00.16
 Build Date:03/18/10                              Use [+] or [-] to
 Version   :V0.13a                                configure system Time.

 Processor
 AMD Opteron(tm) Processor 6174
 Speed     :2200MHz
 Count     :24

 System Memory                                 ←    Select Screen
 Size      :16384MB                            ↑↓   Select Item
                                               +-   Change Field
 System Time              [10:45:28]           Tab  Select Field
 System Date              [Fri 03/19/2010]     F1   General Help
                                               F10  Save and Exit
                                               ESC  Exit

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```

AMIBIOS
It displays the core number, date of BIOS build and the version of BIOS.

Processor
This displays the CPU information.

System Memory
This displays the amount of system memory present on the system.

System Time / Date setup
System Time: Adjusts the system clock.
HH (24 hours format): MM (Minutes): SS (Seconds)
System Date: Adjusts the system date.
MM (Months): DD (Days): YYYY (Years)

3.3 Advanced Menu

This section facilitates configuring advanced BIOS options for your system.

```
                    BIOS SETUP UTILITY
  Main   Advanced   PCIPnP   Boot   Security   Chipset   Exit

  Advanced Settings                             Configure CPU.

  WARNING: Setting wrong values in below sections
           may cause system to malfunction.

  ▶ CPU Configuration
  ▶ IDE Configuration
  ▶ SuperIO Configuration
  ▶ ACPI Configuration
  ▶ Hardware Health Configuration
  ▶ IPMI 2.0 Configuration
  ▶ MPS Configuration
  ▶ PCI Express Configuration         ←    Select Screen
  ▶ Remote Access Configuration       ↑↓   Select Item
  ▶ USB Configuration                 Enter Go to Sub Screen
                                      F1   General Help
                                      F10  Save and Exit
                                      ESC  Exit


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```

CPU Configuration
Configure CPU.

IDE Configuration
Configure the IDE devices.

Super IO Configuration
Configure the Super IO.

ACPI Configuration
Selection for Advanced ACPI Configuration.

Hardware Health Configuration
Configure / monitor the Hardware Health.

IPMI 2.0 Configuration
IPMI configuration including server monitoring and event log.
MPS Configuration

Configure the Multi-Processor Table.

PCI Express Configuration
Configure PCI Express Support.

Remote Access Configuration
Configure Remote Access.

USB Configuration
Configure the USB support.

3.3.1 Advanced CPU Configuration

This section allows you to fine-tune the processor options.

```
                      BIOS SETUP UTILITY
      Advanced
 ┌──────────────────────────────────────────┬─────────────────────────┐
 │ CPU Configuration                      ▲  │ Select which physical   │
 │ Module Version: 5.1100.1                  │ CPU's information to     │
 │ Physical Count: 4                         │ display. Note: Zero      │
 │ Logical Count : 24                        │ is always the "Boot      │
 │                                           │ Strap Processor" or      │
 │                                           │ main CPU. All others     │
 │ CPU Information          [Processor 0]    │ are "Application         │
 │ AMD Opteron(tm) Processor 6174            │ Processors."             │
 │ Revision: D1                              │                         │
 │ Cache L1: 128KB                           │                         │
 │ Cache L2: 512KB                           │                         │
 │ Cache L3: 12MB                            │                         │
 │ Speed   : 2200MHz,   NB Clk: 1800MHz      │                         │
 │ Able to Change Freq.  : Yes               │  ←    Select Screen     │
 │ uCode Patch Level     : 0x10000B5         │  ↑↓   Select Item       │
 │ GART Error Reporting       [Disabled]     │  +-   Change Option     │
 │ Microcode Update           [Enabled]      │  F1   General Help      │
 │ Secure Virtual Machine Mode [Enabled]     │  F10  Save and Exit     │
 │ PowerNow                   [Enabled]      │  ESC  Exit              │
 │ PowerCap                   [P-state 0]    │                         │
 │ ACPI SRAT Table            [Enabled]   ▼  │                         │
 └──────────────────────────────────────────┴─────────────────────────┘
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```

GART Error Reporting
This option should remain disabled for normal operation. The driver developer may
enable it for the purpose of testing.
> **Disabled** / Enable**d**

Microcode Update
> Disabled / **Enabled**

Secure Virtual Machine Mode
> Disabled / **Enabled**

PowerNow
Enable/disable the generation of ACPI_PPC, _PSS, and _PCT objects.
> Disabled / **Enabled**

PowerCap
The option can decide the highest performance P-state in OS.
> **P-state 0** / P-state 1 / P-state 2 / P-state 3 / P-state 4

ACPI SRAT Table
Enable or disable the building of ACPI SRAT Table.
　　　　Disabled / **Enabled**

CPU Prefetching
Enable or disable CPU prefetching.
　　　　Disabled / **Enabled**

IO Prefetching
Enable or disable IO prefetching.
　　　　Disabled / **Enabled**

Probe Filter
Initialization mode for Probe Filter.
　　　　Auto / Disable / MP Mode

3.3.2 Advanced IDE Configuration

```
                        BIOS SETUP UTILITY
  Advanced

  IDE Configuration                          DISABLED: disables the
                                             integrated IDE
  OnBoard PCI IDE Controller    [Both]       Controller.
                                             PRIMARY: enables only
  ▶ Primary IDE Master        : [Not Detected] the Primary IDE
  ▶ Primary IDE Slave         : [Not Detected] Controller.
  ▶ Secondary IDE Master      : [Not Detected] SECONDARY: enables
  ▶ Secondary IDE Slave       : [Not Detected] only the Secondary IDE
  ▶ Third IDE Master          : [Not Detected] Controller.
  ▶ Third IDE Slave           : [Not Detected] BOTH: enables both IDE
  ▶ Fourth IDE Master         : [Not Detected] Controllers.
  ▶ Fourth IDE Slave          : [Not Detected]
                                             ←    Select Screen
  Hard Disk Write Protect       [Disabled]   ↑↓   Select Item
  IDE Detect Time Out (Sec)     [35]         +-   Change Option
  ATA(PI) 80Pin Cable Detection [Host & Device] F1   General Help
                                             F10  Save and Exit
                                             ESC  Exit


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```

Onboard PCI IDE Controller
Disabled: disables the integrated IDE Controller
Primary: enables only the Primary IDE Controller
Secondary: enables only the Secondary IDE Controller
Both: enables both IDE Controller
      Disabled **/** Primary / Secondary **/ Both**

Primary/Secondary/Third/Fourth IDE Master
While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of auto detection of IDE devices.

Hard Disk Write Protect
Disable/Enable device write protection. This will be effective only if device is accessed through BIOS.
      Disabled / Enabled

IDE Detect Time Out (Sec)
Select the time out value for detecting ATA/ATAPI device(s).
      0~35 (at 5 interval)

ATA(PI) 80Pin Detection

Select the mechanism for detecting 80Pin ATA(PI) Cable.
Host & Device / Host / Device

3.3.3 Super I/O Configuration

```
                         BIOS SETUP UTILITY
    Advanced

 Configure Win627DHG Super IO Chipset         Allows BIOS to Select
                                              Serial Port1 Base
 Serial Port1 Address          [3F8/IRQ4]     Addresses.
 Serial Port2 Address          [2F8/IRQ3]
   Serial Port2 Mode           [Normal]
 Parallel Port Address         [378]
   Parallel Port Mode          [Normal]
   Parallel Port IRQ           [IRQ7]




                                              ←    Select Screen
                                              ↑↓   Select Item
                                              +-   Change Option
                                              F1   General Help
                                              F10  Save and Exit
                                              ESC  Exit



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```

Serial Port1 Address
Allows BIOS to configure Serial Port1 Base Address.
        Disabled / **3F8/IRQ4** / 2E8/IRQ3

Serial Port2 Address
Allows BIOS to configure Serial Port2 Base Address.
        Disabled / 2F8/IRQ3 / 2E8/IRQ3

Serial Port2 Mode
Allows BIOS to select mode for Serial Port2.
        Normal / IrDA / Ask IR

Parallel Port Address
Allows BIOS to select Parallel Port Base Address.
        Disabled / 378 / 278 / 3BC

Parallel Port IRQ
Allows BIOS to select Parallel Port IRQ
        IRQ7 / IRQ5

3.3.4 ACPI Configuration

```
                          BIOS SETUP UTILITY
   Advanced

   ACPI Settings                                   Advanced ACPI
                                                   Configuration settings
 ▶ Advanced ACPI Configuration
                                                   Use this section to
                                                   configure additional
                                                   ACPI options.




                                                   ←    Select Screen
                                                   ↑↓    Select Item
                                                   Enter Go to Sub Screen
                                                   F1    General Help
                                                   F10   Save and Exit
                                                   ESC   Exit
```

3.3.4.1 Advanced ACPI Configuration

```
                        BIOS SETUP UTILITY
   Advanced

   Advanced ACPI Configuration                    Enable RSDP pointers
                                                  to 64-bit Fixed System
   ACPI Version Features         [ACPI v3.0]      Description Tables. Di
   ACPI APIC support             [Enabled]        ACPI version has some
   AMI OEMB table                [Enabled]
   Headless mode                 [Disabled]

   C1E Support                   [Enable]



                                                  ←    Select Screen
                                                  ↑↓   Select Item
                                                  +-   Change Option
                                                  F1   General Help
                                                  F10  Save and Exit
                                                  ESC  Exit


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```

ACPI Version Features
Set this value to allow or prevent the system to be complaint with the ACPI 2.0
specification.
      ACPI 3.0 / ACPI 2.0 / ACPI 1.0

ACPI APIC Support
This option allows you to define whether or not to enable APIC features.
      Enabled / Disabled

AMI OEMB Table
Set this value to allow the ACPI BIOS to add a pointer to an OEMB table in the Root
System Description Table (RSDT) table.
      Enabled / Disabled

> **NOTE:** OEMB table is used to pass POST data to the AMI code
> during ACPI O/S operations.

Headless Mode
Enable or disable Headless operation mode through ACPI.
      Disabled / Enabled

C1E Support
Enhanced C1 state support.
          Disabled **/ Enabled**

3.3.5 Hardware Health Configuration

```
                          BIOS SETUP UTILITY
     Advanced

   W83795 Hardware Health Configuration             Sensor Monitoring for
                                                     BMC
   Smart FAN configuration          [Disabled]
   ▶ Sensor Data Register Monitoring




                                                     ←    Select Screen
                                                     ↑↓   Select Item
                                                     Enter Go to Sub Screen
                                                     F1   General Help
                                                     F10  Save and Exit
                                                     ESC  Exit


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```
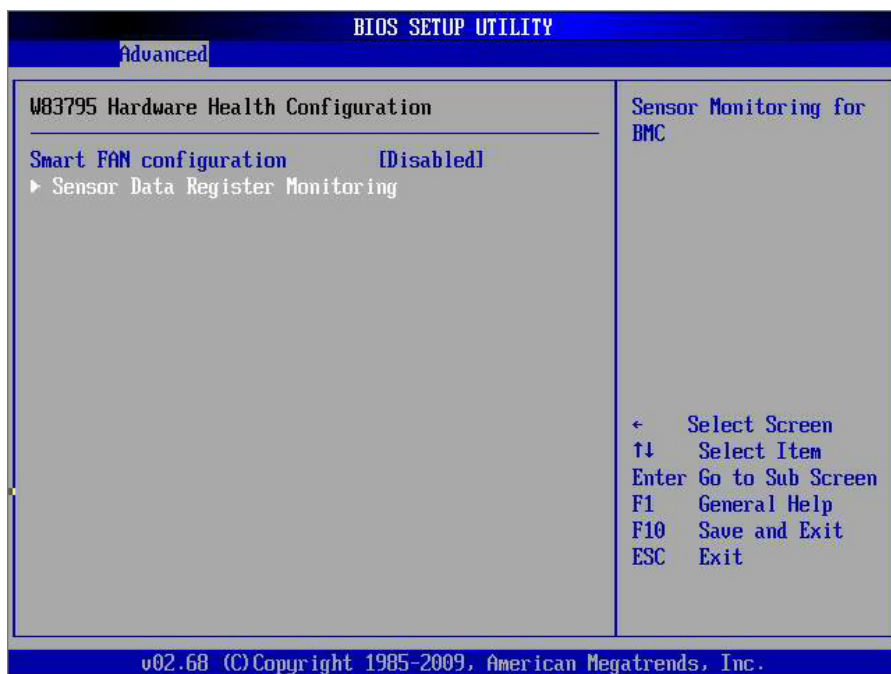
Smart FAN Configuration
Select Smart FAN mode:
- Disable:
- Smart Fan: fan speed up as temperature goes up
    Smart Fan **/ Disabled**

Sensor Data Register Monitoring
Sensor Monitoring for BMC

3.3.5.1 Sensor Data Register Monitoring

```
        Advanced

  ID# NAME                    READING        STATUS        Press Enter key to
  ─────────────────────────────────────────────────        display remain sensor
  10  12V1                  :12.040 V       OK
  11  12V                   :11.954 V       OK           ESC key to return this
  12  SIO_AVCC              :3.312 V        OK            page.
  13  VCC3.3               :3.328 V        OK
  16  12V                  :11.868 V        OK
  1E  3.3V DUAL            :3.280 V         OK
  1F  VBAT                 :3.248 V         OK
  30  P0_VDD               :1.096 V         OK
  31  P0_VDDNB             :1.080 V         OK
  32  P1_VDD               :1.096 V         OK
  33  P1_VDDNB             :1.072 V         OK        ←     Select Screen
  34  P0_VTT               :0.736 V         OK        ↑↓    Select Item
  35  P1_VTT               :0.744 V         OK        Enter Go to Sub Screen
  36  CPU0_VLDT            :1.192 V         OK        F1    General Help
  37  CPU1_VLDT            :1.184 V         OK        F10   Save and Exit
  38  VDDPCIE_RD890        :1.112 V         OK        ESC   Exit
  39  VDDC_RD890           :1.128 V         OK
  ▶ SDR Monitoring Next Page

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```

Read only. It can not be modified in user mode.

3.3.6 IPMI 2.0 Configuration

```
                          BIOS SETUP UTILITY
     Advanced

 IPMI 2.0 Configuration                          View all events in the
                                                 BMC Event Log.
 Status Of BMC                  Working          It will take a max. of
 ▶ View BMC System Event Log                     15 seconds to read all
 Clear BMC System Event Log                      BMC SEL records.
 ▶ Set LAN Configuration
 ▶ Set PEF Configuration
 BMC Watch Dog Timer Action    [Disabled]
 BMC Alert LED and Beep        [OFF]

 FW Key :                      [0000000]

                                                 ←    Select Screen
                                                 ↑↓   Select Item
                                                 Enter Go to Sub Screen
                                                 F1   General Help
                                                 F10  Save and Exit
                                                 ESC  Exit

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```

View BMC System Event Log
View all events in the BMC Event Log. It will take a max. of 15 seconds to read all
BMC SEL records.

Clear BMC System Event Log
Clear all events in BMC System Event Log.

Set LAN Configuration
Set LAN Configuration Parameters Command.

Set PEF Configuration
Set PEF Configuration Parameters Command.

BMC Watch Dog Timer Action
Allows the BMC to reset or power down the system if the operating system crashes
or hangs.
     Disabled / Enabled

BMC Alert LED and Beep
BMC Alert LED and Beep.
     OFF / ON

FW Key
Enter IPMI FW Key upgrade to IPMI or iKVM function.
[0000000]

3.2.6.1 View BMC System Event Log

```
                        BIOS SETUP UTILITY
        Advanced

 Total Number Of Entries:        295                 Use +/- to traverse
                                                     the event log.
 SEL Entry Number:               [  1]
 SEL Record ID:                  0001
 SEL Record Type:                02 (System Event)
 Event Timestamp:                Mar 5, 2010 10:48:13
 Generator ID:                   0001
 Event Message Format Ver:       04 (IPMI ver 2.0)
 Event Sensor Type:              0F (POST Error)
 Event Sensor Number:            00
 Event Dir Type:                 00
 Event Data:                     00 07 00
                                                     ←     Select Screen
                                                     ↑↓    Select Item
                                                     +-    Change Option
                                                     F1    General Help
                                                     F10   Save and Exit
                                                     ESC   Exit


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```

Read only. It can not be modified in user mode.

3.2.6.2 LAN Configuration

```
                        BIOS SETUP UTILITY
     Advanced

 LAN Configuration Status.                    This gorup provide
                                              setup function for
 Current IP source in BMC:        [DHCP]
 Current IP address in BMC:       192.168.000.058   1. IP Address Source
 Current Subnet Mask in BMC:      255.255.255.000   2. IP Address
 Current Gateway address in BMC: 192.168.000.001    3. Subnet Mask
 Current MAC address in BMC:      00.E0.81.F0.25.FA 4. Gateway Address

 ▶ Setup LAN Configuration

                                              ←     Select Screen
                                              ↑↓    Select Item
                                              Enter Go to Sub Screen
                                              F1    General Help
                                              F10   Save and Exit
                                              ESC   Exit

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```

Read only. It can not be modified in user mode.

3.2.6.2.1 Setup LAN Configuration

```
                          BIOS SETUP UTILITY
    Advanced

  Setup LAN Configuration.                          IPMI IP Address Source
  ─────────────────────────────────────            STATIC / DHCP
  IP Address Source         [STATIC]
  IP Address                [192.168.000.022]       After setup LAN
  Subnet Mask               [255.255.255.000]       Configure need select
                                                    Save LAN Configuration
  Save LAN Configuration                            and choice [Ok] to
                                                    enabled changes.



                                                    ←    Select Screen
                                                    ↑↓   Select Item
                                                    +-   Change Option
                                                    F1   General Help
                                                    F10  Save and Exit
                                                    ESC  Exit


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```

IP Address Source
Select IPMI IP Address Source.
> **STATIC /** DHCP

> **NOTE:**
> **IP Address** and **Subnet Mask** appear when **IP Address Source** is
> set to [STATIC].

IP Address / Subnet Mask
> Read only. It can not be modified in user mode.

Save LAN Configuration
After setup LAN Configuration, select Save LAN Configuration and click [OK] to
enable changes.

3.2.6.3 Set PEF Configuration

```
                          BIOS SETUP UTILITY
     Advanced

 Set PEF Configuration Parameters Command.              Enable or Disable PEF
                                                        Support.
 PEF SUPPORT                      [Enabled]
 PEF Action Global Control        [Alert]
 Alert Startup Delay              [Disabled]
 Startup Delay                    [Disabled]
 Event Message For PEF Action     [Disabled]



                                                    ←    Select Screen
                                                    ↑↓   Select Item
                                                    +-   Change Option
                                                    F1   General Help
                                                    F10  Save and Exit
                                                    ESC  Exit


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```

PEF Support
Enable or disable PEF support.
> **Enabled /** Disabled

PEF Action Global Control
Select action for PEF Action Global Control.
> **Alert /** Power Down / Reset System / Power Cycle / OEM Action /
> Diagnostic. Int.

Alert Startup Delay
Enable/disable Alert Startup Delay.
> **Disabled /** Enabled

Startup Delay
Enable/disable Startup Delay.
> **Disabled /** Enabled

Event Message For PEF Action
Enable/disable Event Message for PEF Action.
> **Disabled /** Enabled

3.3.7 MPS Configuration

```
                          BIOS SETUP UTILITY
   Advanced

  MPS Configuration                                    Select MPS
  ─────────────────────────────────────               Revision.
  MPS Revision                    [1.4]











                                                 ←     Select Screen
                                                 ↑↓    Select Item
                                                 +-    Change Option
                                                 F1    General Help
                                                 F10   Save and Exit
                                                 ESC   Exit


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```
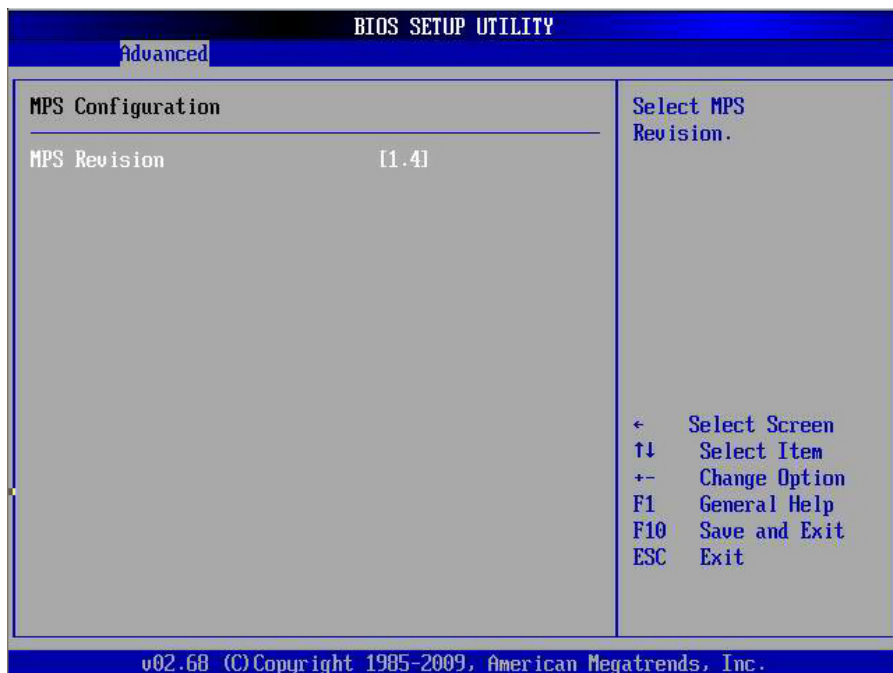
MPS Revision
Select MPS Revision.
         1.4 / 1.1

3.3.8 PCI-Express Configuration

```
                         BIOS SETUP UTILITY
     Advanced

  PCI Express Configuration                         Enables/Disables
                                                    Pci Express Device
  Relaxed Ordering                [Auto]            Relaxed Ordering.
  Maximum Payload Size            [Auto]
  Extended Tag Field              [Auto]
  No Snoop                        [Auto]
  Maximum Read Request Size       [Auto]
  Active State Power Management   [Disabled]
  Extended Synch                  [Auto]


                                                ←    Select Screen
                                                ↑↓   Select Item
                                                +-   Change Option
                                                F1   General Help
                                                F10  Save and Exit
                                                ESC  Exit



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```

Relax Ordering
Enables / Disables PCI Express Device Relaxed Ordering.
      Auto / Disabled / Enabled

Maximum Payload Size
Set Maximum Payload of PCI Express Device or allow System BIOS select the value.
      Auto / Disabled

Extended Tag Field
If Enabled, allows Device to use 8-bit Tag field as a requester.
      Auto / Disabled

No Snoop
Enables/Disables PCI Express Device No Snoop option.
      Auto / Disabled

Maximum Read Request Size
Set Maximum Read Request Size of PCI Express Device or allow System BIOS select the value.
      Auto / Disabled

Active State Power Management
Enable/disable PCI Express L0s AND L1 link power states.
Disabled / Enabled

Extended Synch
If enabled, allows generation of Extended Synchronization patterns.
Auto / Disabled

3.3.9 Remote Access Configuration

```
                        BIOS SETUP UTILITY
     Advanced

  Configure Remote Access type and parameters        Select Remote Access
                                                      type.
  Remote Access              [Disabled]




                                                      ←    Select Screen
                                                      ↑↓   Select Item
                                                      +-   Change Option
                                                      F1   General Help
                                                      F10  Save and Exit
                                                      ESC  Exit


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```
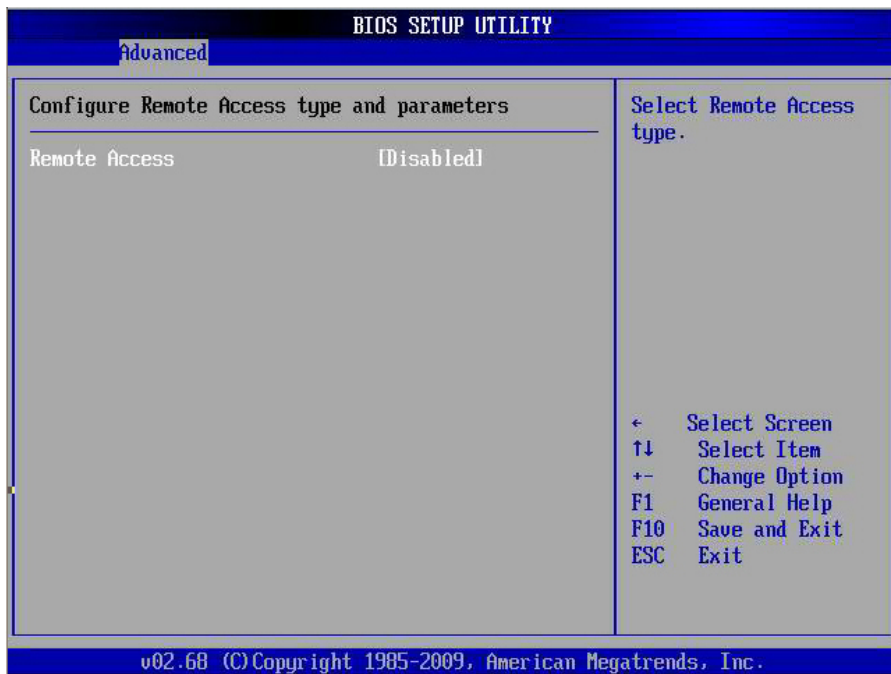
Remote Access
Enables remote access to system through serial port.
> **Disabled** / Enabled

NOTE:
The following BIOS items are available only when **Remove Access** is set
to [Enabled].

Serial Port Number
Select Serial Port for cosole redirection. Make sure the selected port is enabled.
> **COM1 /** COM2 / COM3 (virtual for BMC)

Serial Port Mode
Select Serial Port settings.

Flow Control
Select Flow Control for console redirection.
> **None /** Hardware / Software

Redirection After BIOS POST
Disabled: Turns off the redirection after POST Boot Loader.
Boot Loader: Redirection is active during POST and during Boot Loader.
Always: Redirection is always active. (Some Oss may not work if set to Always)
Always / Disabled / Boot Loader

Terminal Type
Select the target terminal type.
ANSI / VT100 / VT-UTF8

VT-UTF8 Combo Key Support
Enable VT-UFT8 Combination Key Support for ANSI/VT100 terminals.
Enabled / Disabled

Sredir Memory Display Delay
Gives the delay in seconds to display memory information.
No Delay / Delay 1 Sec / Delay 2 Sec / Delay 4 Sec

3.3.10   USB Configuration

```
                          BIOS SETUP UTILITY
     Advanced

 USB Configuration                              Enables support for
                                                legacy USB. AUTO
 Module Version - 2.24.5-13.4                    option disables
                                                legacy support if
 USB Devices Enabled :                          no USB devices are
   2 Keyboards, 2 Mice, 1 Hub                    connected.

 Legacy USB Support            [Enabled]
 USB 2.0 Controller Mode       [HiSpeed]
 BIOS EHCI Hand-Off            [Enabled]
 Legacy USB1.1 HC Support      [Enabled]

                                                ←    Select Screen
                                                ↑↓   Select Item
                                                +-   Change Option
                                                F1   General Help
                                                F10  Save and Exit
                                                ESC  Exit


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```

Legacy USB Support
Enables support for legacy USB. AUTO option disables legacy support if no USB
devices are connected.
> **Enabled** / Disabled / Auto

USB 2.0 Controller Mode
Configure the USB 2.0 controller in Hi Speed (480 Mbps) or Full Speed (12Mbps).
> **Hi Speed** / Full Speed

BIOS EHCI Hand-OFF
This is a work around for OSes without EHCI hand-off support. The EHCI
ownership change should claim by EHCI driver.
> **Enabled** / Disabled

Legacy USB1.1 HC Support
Enables support for legacy USB. Auto option disables legacy support if no USB
devices are connected.
> **Enabled** / Disabled

3.4 PCI/PnP Menu

```
                          BIOS SETUP UTILITY
  Main    Advanced    PCIPnP    Boot    Security    Chipset    Exit

  Advanced PCI/PnP Settings                        Clear NVRAM during
                                                   System Boot.
  WARNING: Setting wrong values in below sections
           may cause system to malfunction.

  Clear NVRAM                    [No]
  Plug & Play O/S                [No]
  PCI Latency Timer              [64]
  Allocate IRQ to PCI VGA        [Yes]
  Palette Snooping               [Disabled]
  PCI IDE BusMaster              [Enabled]
  OffBoard PCI/ISA IDE Card      [Auto]
                                                 ←    Select Screen
                                                 ↑↓   Select Item
                                                 +-   Change Option
                                                 F1   General Help
                                                 F10  Save and Exit
                                                 ESC  Exit


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```

Clear NVRAM
Clear NVRAM during system Boot.
> **No** / Yes

Plug & Play O/S
No: lets the BIOS configure all the devices in the system.
Yes: lets the operating system configure Plug and Play (PnP) devices not required
for boot if your system has a Plug and Play operating system.
> **No** / Yes

PCI Latency Timer
This setting controls how many PCI clocks each PCI device can hold the bus before
another PCI device takes over. When set to higher values, every PCI device can
conduct transactions for a longer time and thus improve the effective PCI bandwidth.
Values in units of PCI clocks for PCI device latency timer register
> **64** / 32 / 96 / 128 / 160 / 192 / 224 / 248

Allocate IRQ to PCI VGA
Yes: assigns IRQ to PCI VGA card if card requests IRQ.
> **Yes** / No

Palette Snooping
This is the default setting and should not be changed unless the VGA card manufacturer requires Palette Snooping to be Enabled.
Enabled: informs the PCI devices that an ISA graphics device is installed in the system so the card will function correctly.
Disabled / Enabled

PCI IDE Bus Master
Enabled: BIOS uses PCI bus mastering for reading / writing to IDE drives.
Enabled / Disabled

Offboard PCI/ISA IDE Card
Some PCI IDE cards may require this to be set to the PCI slot number that is holding the card.
Auto: Works for most PCI IDE cards.
Auto / PCI Slot 1 / PCI Slot 2 / PCI Slot 3 / PCI Slot 4/ PCI Slot 5 / PCI Slot 6

3.5 Boot Menu

```
                    BIOS SETUP UTILITY
                         Boot

 Boot Settings Configuration                    Allows BIOS to skip
 ─────────────────────────────────────────────  certain tests while
 Quick Boot                  [Enabled]           booting. This will
 Quiet Boot                  [Disabled]          decrease the time
 AddOn ROM Display Mode       [Force BIOS]        needed to boot the
 Bootup Num-Lock              [ON]               system.
 PS/2 Mouse Support           [Auto]
 Wait For 'F1' If Error       [Enabled]
 Hit 'DEL' Message Display    [Enabled]
 Interrupt 19 Capture         [Disabled]

                                                 ←    Select Screen
                                                 ↑↓   Select Item
                                                 +-   Change Option
                                                 F1   General Help
                                                 F10  Save and Exit
                                                 ESC  Exit


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```

Quick Boot
This option allows user bypass BIOS self test during POST.
  Enabled / Disabled

Quiet Boot
Disabled: displays normal POST messages.
Enabled: displays OEM log instead of POST messages.
  Disabled / Enabled

Add On ROM Display Mode
Allows user to force BIOS/Option ROM of add-on cards to be displayed during quiet
boot.
  Force BIOS / Keep Current

Boot Up Num-Lock
Selects Power-on state for Numlock.
  On / Off

PS/2 Mouse Support
Select support for PS/2 Mouse.
Auto / Enabled / Disabled

Wait for 'F1' If Error
Waits for F1 key to be present if error occurs.
Enabled / Disabled

Hit 'DEL' Message Display
Displays "Press DEL to run Setup in POST".
Enabled / Disabled

Interrupt 19 Capture
Enabled: allows option ROMs to trap interrupt 19.
Enabled / Disabled

3.6 Security Menu

```
                        BIOS SETUP UTILITY
  Main    Advanced    PCIPnP    Boot   Security   Chipset    Exit

  Security Settings                                Install or Change the
  ───────────────────────                          password.
  Supervisor Password :Not Installed
  User Password       :Not Installed

  Change Supervisor Password
  Change User Password

  Boot Sector Virus Protection   [Disabled]
  ─────────────────────────────────────────
  ▶ Trusted Computing
                                                 ←    Select Screen
                                                 ↑↓   Select Item
                                                 Enter Change
                                                 F1   General Help
                                                 F10  Save and Exit
                                                 ESC  Exit


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```

Supervisor Password/User Password
Read only.

Change Supervisor Password
Install or change the password.

Change User Password
Install or change the password.

Boot Sector Virus Protection
When it is set to [Enabled], BIOS will issue a virus warning message and beep if a
write to the boot sector or the partition table of the HDD is attempted.
        Disabled / Enabled

3.7 Chipset Menu

```
                          BIOS SETUP UTILITY
  Main     Advanced    PCIPnP    Boot    Security    Chipset    Exit

  Advanced Chipset Settings                          Options for NB

  ▶ NorthBridge Configuration
  ▶ SouthBridge Configuration
  ▶ RD890 Configuration
  ▶ OnBoard Peripherals Configuration




                                                  ←    Select Screen
                                                  ↑↓   Select Item
                                                  Enter Go to Sub Screen
                                                  F1    General Help
                                                  F10   Save and Exit
                                                  ESC   Exit


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```

Allows you to change NorthBridge, SouthBridge, RD890 and Onboard Peripherals
Configuration.

3.7.1 North Bridge Configuration

```
                        BIOS SETUP UTILITY
                                          Chipset

  NorthBridge Chipset Configuration

  ▶ Memory Configuration
  ▶ ECC Configuration
  ▶ DRAM Timing Configuration

  Memory Timing Parameters        [CPU Node 0]

    Memory CLK           :667 MHz, 667 MHz
    CAS Latency(Tcl)     :9 CLK , 9 CLK
    RAS/CAS Delay(Trcd)  :9 CLK , 9 CLK
    Row Precharge Time(Trp):9 CLK , 9 CLK
    Min Active RAS(Tras) :24 CLK, 24 CLK        ←   Select Screen
    RAS/RAS Delay(Trrd)  :4 CLK, 4 CLK          ↑↓   Select Item
    Row Cycle (Trc)      :33 CLK, 33 CLK        Enter Go to Sub Screen
    Read to Precharge(Trtp):5 CLK, 5 CLK        F1    General Help
    Write Recover Time(Twr):10 CLK, 10 CLK      F10   Save and Exit
                                                ESC   Exit


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```

Memory Timing Parameters
To select which node's timing parameters to display.
> **CPU Node 0** / CPU Node 1

3.7.1.1 Memory Configuration

```
                          BIOS SETUP UTILITY
                                            Chipset

 Memory Configuration                          Enable Bank Memory
                                               Interleaving
 Bank Interleaving          [Auto]
 Node Interleaving          [Disabled]
 Channel Interleaving       [Auto]
 CS Sparing Enable          [Disabled]
 Bank Swizzle Mode          [Enabled]



                                               ←    Select Screen
                                               ↑↓   Select Item
                                               +-   Change Option
                                               F1   General Help
                                               F10  Save and Exit
                                               ESC  Exit


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```
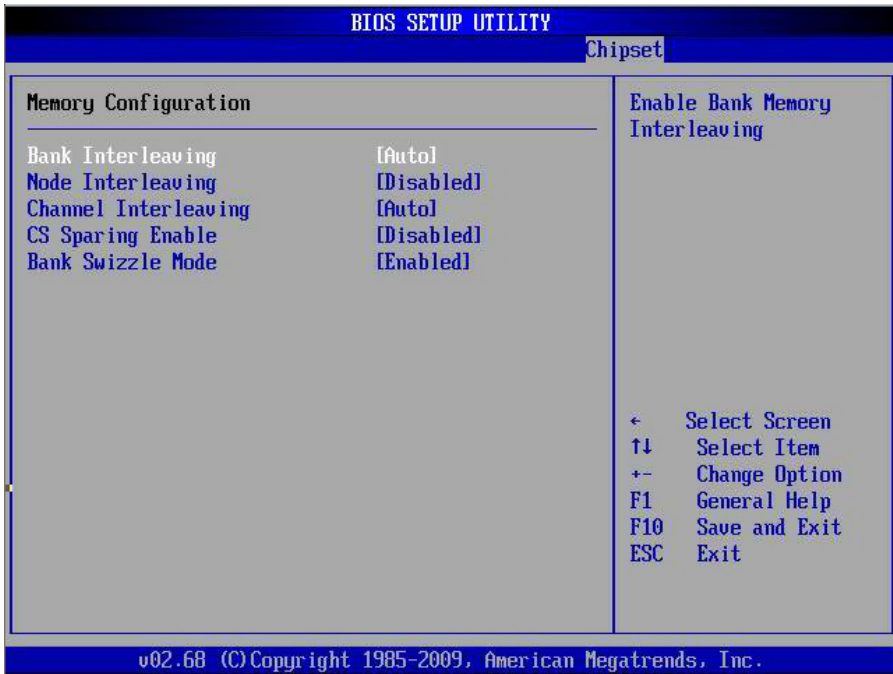
Bank Interleaving
Bank Interleave setting has to do with the actual RAM chip properties, most good quality RAM chips have "4-bank interleaving" and work best at this setting. Interleaving controls how actual hits to memory takes place.
Enable Bank Memory Interleaving.
     Auto / Disabled

Node Interleaving
Enable Node Memory Interleaving.
     Disabled / Enabled

Channel Interleaving
Enable Channel Memory Interleaving.
     Auto / Disabled

CS Sparing Enable
Reserve a spare memory rank in each node.
     Disabled / Enabled

Bank Swizzle Mode
Enable or disable bank swizzle mode.
     Enabled / Disabled

3.7.1.2 ECC Configuration

```
                         BIOS SETUP UTILITY
                                            Chipset

  ECC Configuration                                  Set the level of ECC
                                                     protection. Note: The
  ECC Mode                    [Basic ]               'Super' ECC mode
    DRAM ECC Enable           [Enabled]              dynamically sets the
                                                     DRAM scrub rate so
                                                     all of memory is
                                                     scrubbed in 8 hours.




                                                  ←    Select Screen
                                                  ↑↓   Select Item
                                                  +-   Change Option
                                                  F1   General Help
                                                  F10  Save and Exit
                                                  ESC  Exit


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```

ECC Mode
Select the level of ECC protection. Note: The "Super" ECC mode dynamically sets
the DRAM scrub rate so all of memory is scrubbed in 8 hours.
   Basic / Super / Disabled / Good / Max / User

DRAM ECC Enable
DRAM ECC allows hardware to report and correct memory errors automatically
maintaining system integrity.
   Enabled / Disabled

3.7.1.3 DRAM Timing Configuration

```
                        BIOS SETUP UTILITY
                                              Chipset

  DRAM Timing Configuration                           Options

  DRAM Timing Config        [Auto]             Auto
                                               Manual




                                               ←    Select Screen
                                               ↑↓   Select Item
                                               +-   Change Option
                                               F1   General Help
                                               F10  Save and Exit
                                               ESC  Exit



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```
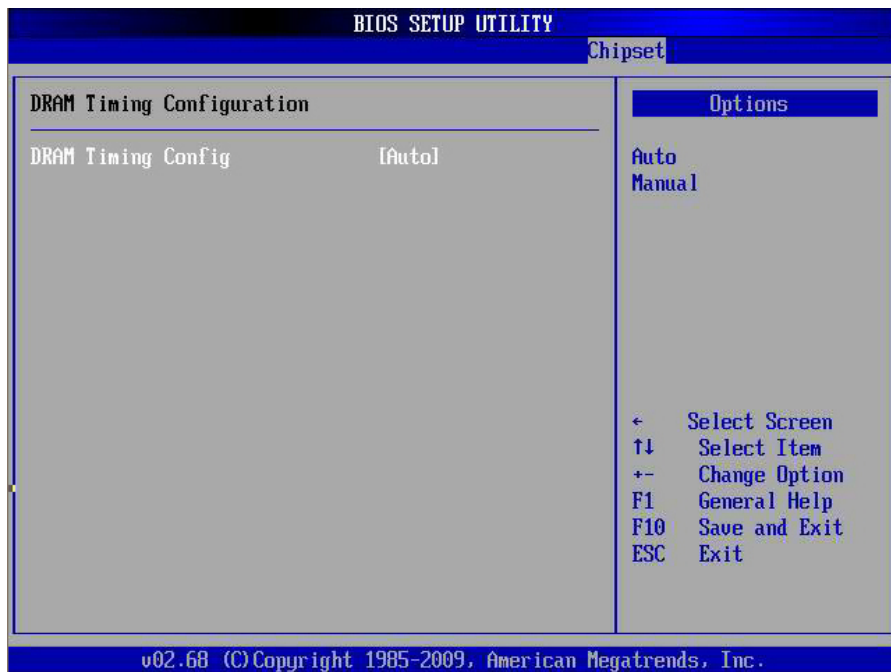
DRAM Timing Config
Select the DRAM Frequency programming method. If Auto, the DRAM speed will
be based on SPDs. If Limit, the DRAM speed will not exceed the specified value. If
Manual, the DRAM speed specified will be programmed by users.
     Auto / Manual / Limit

3.7.2 South Bridge Configuration

```
                        BIOS SETUP UTILITY
                                          Chipset

   SouthBridge Chipset Configuration                      Options

   SB700 CIMx Version : 5.4.0                          Disabled
                                                       Enabled
   OHCI HC(Bus 0 Dev 18 Fn 0)    [Enabled]
   OHCI HC(Bus0 Dev 18 Fn 1)     [Enabled]
   EHCI HC(Bus0 Dev 18 Fn 2)     [Enabled]
   OHCI HC(Bus0 Dev 19 Func 0)   [Enabled]
   OHCI HC(Bus 0 Dev 19 Func 1)  [Enabled]
   EHCI HC(Bus 0 Dev 19 Fn 2)    [Enabled]
   OHCI HC (Bus 0 Dev 20 Fn 5)   [Enabled]

   OnChip SATA Channel           [Enabled]       ←    Select Screen
   OnChip SATA Type              [Native IDE]    ↑↓   Select Item
   SATA IDE Combined Mode        [Enabled]       +-   Change Option
   PATA Channel Config           [SATA as primary]  F1   General Help
                                                 F10  Save and Exit
   Power Saving Features         [Disabled]      ESC  Exit


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```

OnChip SATA Channel
Enable or disable OnChip SATA channel.
Enabled / Disabled

OnChip SATA Type
Select OnChip SATA type.
Native IDE / RAID / AHCI

SATA IDE Combined Mode
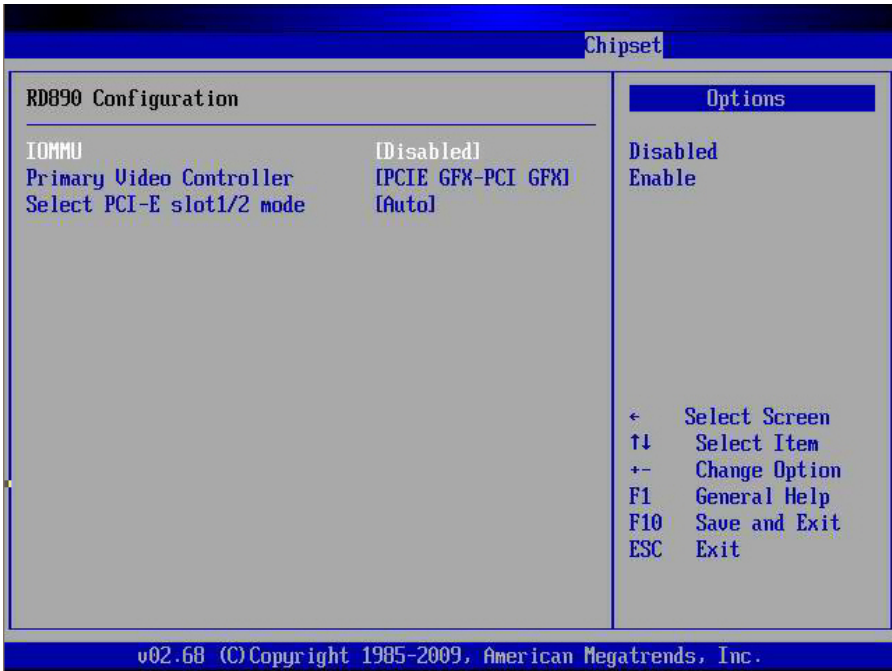Disabled / **Enabled**

PATA Channel Config
SATA as primary / SATA as seondary

Power Saving Features
Enable/Disable power saving features in SB. As general rule, this feature should be disabled for desktop and enabled for mobile. See AMD SB700 Power Saving document for more details.

Enabled / Disabled

3.7.3 RD890 Configuration

```
                                              Chipset

 RD890 Configuration                                          Options

 IOMMU                          [Disabled]         Disabled
 Primary Video Controller       [PCIE GFX-PCI GFX] Enable
 Select PCI-E slot1/2 mode      [Auto]



                                                   ←    Select Screen
                                                   ↑↓   Select Item
                                                   +-   Change Option
                                                   F1   General Help
                                                   F10  Save and Exit
                                                   ESC  Exit


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```

IOMMU
Disable or Enable IOMMU function.
> **Disabled** / Enabled

Primary Video Controller
PCIE GFX-PCI GFX: Video card scan from PCIE bus to PCI bus.
PCI GFX-PCIE GFX: Video card scan from PCI bus (onboard VGA) to PCIE bus.
> **PCIE GFX-PCI GFX** / PCI GFX-PCIE GFX

Select PCI-E slot1/2 mode
Auto: auto detect by BIOS
1x16: Slot1 – x16, Slot2 – not work
2x8: Slot1 – x8, Slot2 – x8
> **Auto** / 1x16 / 2x8

3.7.4 Onboard Peripherals Configuration

```
                                              Chipset

OnBoard LSI SAS2008          [Enable]                    Options
  SAS OPTROM                 [Enable]
OnBoard i82576 NIC           [Enable]           Enable
  i82576 PORT1 PXE           [Disabled]         Disabled
  i82576 PORT2 PXE           [Disabled]
OnBoard i82574 NIC #1        [Enable]
  i82574 #1 PXE              [Disabled]
OnBoard i82574 NIC #2        [Enable]
  i82574 #2 PXE              [Disabled]

Restore on AC Power Loss     [Power Off]
Chassis intrusion detection  [Disabled]
Watchdog Mode                [Disabled]
                                                ←     Select Screen
                                                ↑↓    Select Item
                                                +-    Change Option
                                                F1    General Help
                                                F10   Save and Exit
                                                ESC   Exit


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```

Restore On AC Power Loss
Configure how the system board responds to a power failure.
> **Power Off** / Power On / Last State

Chassis Intrusion Detection
Disabled: Disable Chassis Intrusion Detection.
Enabled: When a chassis open event is detected, the BIOS will record the event and issue a warning beep.
> **Disabled** / Enabled

Watchdog Mode
Disabled: Disable Watchdog
POST: BIOS POST Watchdog, timer counting starts at PowerOn, stops at OS boot
OS: Boot Watchdog, starts at OS boot
PowerOn: Start at PowerOn
> **Disabled** / PowerOn / POST / OS

3.8 Exit Menu

```
                        BIOS SETUP UTILITY
  Main    Advanced    PCIPnP    Boot    Security    Chipset    Exit

  Exit Options                                  Exit system setup
  _____               after saving the
                                                changes.
  Save Changes and Exit
  Discard Changes and Exit                      F10 key can be used
  Discard Changes                               for this operation.

  Load Optimal Defaults
  Load Failsafe Defaults




                                                ←    Select Screen
                                                ↑↓   Select Item
                                                Enter Go to Sub Screen
                                                F1   General Help
                                                F10  Save and Exit
                                                ESC  Exit


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```

Save Changes and Exit
Use this option to exit setup utility and re-boot.
All new selections you have made are stored into CMOS.
System will use the new settings to boot up.

Discard Changes and Exit
Use this option to exit setup utility and re-boot.
All new selections you have made are not stored into CMOS.
System will use the old settings to boot up.

Discard Changes
Use this option to restore all new setup values that you have made but not saved
into CMOS.

Load Optimal Defaults
Use this option to load default performance setup values.
Use this option when system CMOS values have been corrupted or modified
incorrectly.

Load Failsafe Defaults
Use this option to load all default failsafe setup values.
Use this option when troubleshooting.

Chapter 4: Diagnostics

NOTE: if you experience problems with setting up your system, always check the following things in the following order:

Memory, Video, CPU

By checking these items, you will most likely find out what the problem might have been when setting up your system. For more information on troubleshooting, check the TYAN website at http://www.tyan.com.

4.1 Beep Codes

Fatal errors, which halt the boot process, are communicated through two kinds of audible beeps.
● Eight short beeps: It indicates that a video error has occurred.
● A single long beep repeatedly: It indicates that a DRAM error has occurred. The most common type of error is a memory error.

Before contacting your vendor or TYAN Technical Support, be sure that you note as much as you can about the beep code length and order that you experience. Also, be ready with information regarding add-in cards, drives and O/S to speed the support process and come to a quicker solution.

4.2 Flash Utility

Every BIOS file is unique for the motherboard it was designed for. For Flash Utilities, BIOS downloads, and information on how to properly use the Flash Utility with your motherboard, please check the TYAN web site at http://www.tyan.com

> **NOTE:** Please be aware that by flashing your BIOS, you agree that in the event of a BIOS flash failure, you must contact your dealer for a replacement BIOS. There are no exceptions. TYAN does not have a policy for replacing BIOS chips directly with end users. In no event will TYAN be held responsible for damages done by the end user.

4.3 AMIBIOS Post Code

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer.Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
24	Uncompress and initialize any platform specific BIOS modules.
30	Initialize System Management Interrupt.
2A	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.

Checkpoint	Description
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information.
39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, … etc.) successfully installed in the system and update the BDA, EBDA…etc.
50	Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7A	Initializes remaining option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed / requested.
8C	Late POST initialization of chipset registers.
8E	Program the peripheral parameters. Enable/Disable NMI as selected
90	Late POST initialization of system management interrupt.
A0	Check boot password if installed.
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A8	Prepare CPU for OS boot including final MTRR values.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector. Deinitializes the ADM module.
AB	Prepare BBS for Int 19 boot.
AC	End of POST initialization of chipset registers.
B1	Save system context for ACPI.
00	Passes control to OS Loader (typically INT19h).

NOTE

Glossary

ACPI (Advanced Configuration and Power Interface): a power management specification that allows the operating system to control the amount of power distributed to the computer's devices. Devices not in use can be turned off, reducing unnecessary power expenditure.

AGP (Accelerated Graphics Port): a PCI-based interface which was designed specifically for demands of 3D graphics applications. The 32-bit AGP channel directly links the graphics controller to the main memory. While the channel runs only at 66 MHz, it supports data transmission during both the rising and falling ends of the clock cycle, yielding an effective speed of 133 MHz.

ATAPI (AT Attachment Packet Interface): also known as IDE or ATA; a drive implementation that includes the disk controller on the device itself. It allows CD-ROMs and tape drives to be configured as master or slave devices, just like HDDs.

ATX: the form factor designed to replace the AT form factor. It improves on the AT design by rotating the board 90 degrees, so that the IDE connectors are closer to the drive bays, and the CPU is closer to the power supply and cooling fan. The keyboard, mouse, USB, serial, and parallel ports are built-in.

Bandwidth: refers to carrying capacity. The greater the bandwidth, the more data the bus, phone line, or other electrical path can carry. Greater bandwidth results in greater speed.

BBS (BIOS Boot Specification): a feature within the BIOS that creates, prioritizes, and maintains a list of all Initial Program Load (IPL) devices, and then stores that list in NVRAM. IPL devices have the ability to load and execute an OS, as well as provide the ability to return to the BIOS if the OS load process fails. At that point, the next IPL device is called upon to attempt loading of the OS.

BIOS (Basic Input/Output System): the program that resides in the ROM chip, which provides the basic instructions for controlling your computer's hardware. Both the operating system and application software use BIOS routines to ensure compatibility.

Buffer: a portion of RAM which is used to temporarily store data; usually from an application though it is also used when printing and in most keyboard drivers. The CPU can manipulate data in a buffer before copying it to a disk drive. While this improves system performance (reading to or writing from a disk drive a single time is much faster than doing so repeatedly) there is the possibility of losing your data should the system crash. Information in a buffer is temporarily stored, not permanently saved.

Bus: a data pathway. The term is used especially to refer to the connection between the processor and system memory, and between the processor and PCI or ISA local buses.

Bus mastering: allows peripheral devices and IDEs to access the system memory without going through the CPU (similar to DMA channels).

Cache: a temporary storage area for data that will be needed often by an application. Using a cache lowers data access times since the information is stored in SRAM instead of slower DRAM. Note that the cache is also much smaller than your regular memory: a typical cache size is 512KB, while you may have as much as 4GB of regular memory.

Closed and open jumpers: jumpers and jumper pins are active when they are "on" or "closed", and inactive when they are "off" or "open".

CMOS (Complementary Metal-Oxide Semiconductors): chips that hold the basic startup information for the BIOS.

COM port: another name for the serial port, which is called as such because it transmits the eight bits of a byte of data along one wire, and receives data on another single wire (that is, the data is transmitted in serial form, one bit after another). Parallel ports transmit the bits of a byte on eight different wires at the same time (that is, in parallel form, eight bits at the same time).

DDR (Double Data Rate): a technology designed to double the clock speed of the memory. It activates output on both the rising and falling edge of the system clock rather than on just the rising edge, potentially doubling output.

DIMM (Dual In-line Memory Module): faster and more capacious form of RAM than SIMMs, and do not need to be installed in pairs.

DIMM bank: sometimes called DIMM socket because the physical slot and the logical unit are the same. That is, one DIMM module fits into one DIMM socket, which is capable of acting as a memory bank.

DMA (Direct Memory Access): channels that are similar to IRQs. DMA channels allow hardware devices (like soundcards or keyboards) to access the main memory without involving the CPU. This frees up CPU resources for other tasks. As with IRQs, it is vital that you do not double up devices on a single line. Plug-n-Play devices will take care of this for you.

DRAM (Dynamic RAM): widely available, very affordable form of RAM which looses data if it is not recharged regularly (every few milliseconds). This refresh requirement makes DRAM three to ten times slower than non-recharged RAM such as SRAM.

ECC (Error Correction Code or Error Checking and Correcting): allows data to be checked for errors during run-time. Errors can subsequently be corrected at the same time that they're found.

EEPROM (Electrically Erasable Programmable ROM): also called Flash BIOS, it is a ROM chip which can, unlike normal ROM, be updated. This allows you to keep up with changes in the BIOS programs without having to buy a new chip. TYAN®'s BIOS updates can be found at http://**www.tyan.com**

ESCD (Extended System Configuration Data): a format for storing information about Plug-n-Play devices in the system BIOS. This information helps properly configure the system each time it boots.

Firmware: low-level software that controls the system hardware.

Form factor: an industry term for the size, shape, power supply type, and external connector type of the Personal Computer Board (PCB) or motherboard. The standard form factors are the AT and ATX.

Global timer: onboard hardware timer, such as the Real-Time Clock (RTC).

HDD: stands for Hard Disk Drive, a type of fixed drive.

H-SYNC: controls the horizontal synchronization/properties of the monitor.

HyperTransport™: a high speed, low latency, scalable point-to-point link for interconnecting ICs on boards. It can be significantly faster than a PCI bus for an equivalent number of pins. It provides the bandwidth and flexibility critical for today's networking and computing platforms while retaining the fundamental programming model of PCI.

IC (Integrated Circuit): the formal name for the computer chip.

IDE (Integrated Device/Drive Electronics): a simple, self-contained HDD interface. It can handle drives up to 8.4 GB in size. Almost all IDEs sold now are in fact Enhanced IDEs (EIDEs), with maximum capacity determined by the hardware controller.

IDE INT (IDE Interrupt): Hardware interrupt signal that goes to the IDE.

I/O (Input/Output): the connection between your computer and another piece of hardware (mouse, keyboard, etc.)

IRQ (Interrupt Request): an electronic request that runs from a hardware device to the CPU. The interrupt controller assigns priorities to incoming requests and delivers them to the CPU. It is important that there is only one device hooked up to each IRQ line; doubling up devices on IRQ lines can lock up your system. Plug-n-Play operating systems can take care of these details for you.

Latency: the amount of time that one part of a system spends waiting for another part to catch up. This occurs most commonly when the system sends data out to a peripheral device and has to wait for the peripheral to spread (peripherals tend to be slower than onboard system components).

NVRAM: ROM and EEPROM are both examples of Non-Volatile RAM, memory that holds its data without power. DRAM, in contrast, is volatile.

Parallel port: transmits the bits of a byte on eight different wires at the same time.

PCI (Peripheral Component Interconnect): a 32 or 64-bit local bus (data pathway) which is faster than the ISA bus. Local buses are those which operate within a single system (as opposed to a network bus, which connects multiple systems).

PCI PIO (PCI Programmable Input/Output) modes: the data transfer modes used by IDE drives. These modes use the CPU for data transfer (in contrast, DMA channels do not). PCI refers to the type of bus used by these modes to communicate with the CPU.

PCI-to-PCI Bridge: allows you to connect multiple PCI devices onto one PCI slot.

Pipeline burst SRAM: a fast secondary cache. It is used as a secondary cache because SRAM is slower than SDRAM, but usually larger. Data is cached first to the faster primary cache, and then, when the primary cache is full, to the slower secondary cache.

PnP (Plug-n-Play): a design standard that has become ascendant in the industry. Plug-n-Play devices require little set-up to use. Devices and operating systems that are not Plug-n-Play require you to reconfigure your system each time you add or change any part of your hardware.

PXE (Preboot Execution Environment): one of four components that together make up the Wired for Management 2.0 baseline specification. PXE was designed to define a standard set of preboot protocol services within a client with the goal of allowing networked-based booting to boot using industry standard protocols.

RAID (Redundant Array of Independent Disks): a way for the same data to be stored in different places on many hard drives. By using this method, the data is stored redundantly and multiple hard drives will appear as a single drive to the operating system. RAID level 0 is known as striping, where data is striped (or overlapped) across multiple hard drives, but offers no fault-tolerance. RAID level 1 is known as mirroring, which stores the data within at least two hard drives, but does not stripe. RAID level 1 also allows for faster access time and fault-tolerance, since either hard drive can be read at the same time. RAID level 0+1 is striping and mirroring, providing fault-tolerance, striping, and faster access all at the same time.

RAIDIOS: RAID I/O Steering (Intel)

RAM (Random Access Memory): technically refers to a type of memory where any byte can be accessed without touching the adjacent data and is often referred to the system's main memory. This memory is available to any program running on the computer.

ROM (Read-Only Memory): a storage chip which contains the BIOS; the basic instructions required to boot the computer and start up the operating system.

SDRAM (Synchronous Dynamic RAM): called as such because it can keep two sets of memory addresses open simultaneously. By transferring data alternately from one set of addresses and then the other, SDRAM cuts down on the delays associated with non-synchronous RAM, which must close one address bank before opening the next.

Serial port: called as such because it transmits the eight bits of a byte of data along one wire, and receives data on another single wire (that is, the data is transmitted in serial form, one bit after another).

SCSI Interrupt Steering Logic (SISL): Architecture that allows a RAID controller, such as AcceleRAID 150, 200 or 250, to implement RAID on a system board-embedded SCSI bus or a set of SCSI busses. SISL: SCSI Interrupt Steering Logic (LSI) (only on LSI SCSI boards)

Sleep/Suspend mode: in this mode, all devices except the CPU shut down.

SDRAM (Static RAM): unlike DRAM, this type of RAM does not need to be refreshed in order to prevent data loss. Thus, it is faster and more expensive.

SLI (Scalable Link Interface): NVIDIA SLI technology links two graphics cards together to provide scalability and increased performance. NVIDIA SLI takes advantage of the increased bandwidth of the PCI Express bus architecture, and features hardware and software innovations within NVIDIA GPUs (graphics processing units) and NVIDIA MCPs (media and communications processors). Depending on the application, NVIDIA SLI can deliver as much as two times the performance of a single GPU configuration.

Standby mode: in this mode, the video and hard drives shut down; all other devices continue to operate normally.

UltraDMA-33/66/100: a fast version of the old DMA channel. UltraDMA is also called UltraATA. Without a proper UltraDMA controller, your system cannot take advantage of higher data transfer rates of the new UltraDMA/UltraATA hard drives.

USB (Universal Serial Bus): a versatile port. This one port type can function as a serial, parallel, mouse, keyboard or joystick port. It is fast enough to support video transfer, and is capable of supporting up to 127 daisy-chained peripheral devices.

VGA (Video Graphics Array): the PC video display standard

V-SYNC: controls the vertical scanning properties of the monitor.

ZCR (Zero Channel RAID): PCI card that allows a RAID card to use the onboard SCSI chip, thus lowering cost of RAID solution

ZIF Socket (Zero Insertion Force socket): these sockets make it possible to insert CPUs without damaging the sensitive CPU pins. The CPU is lightly placed in an open ZIF socket, and a lever is pulled down. This shifts the processor over and down, guiding it into the board and locking it into place.

Technical Support

If a problem arises with your system, you should first turn to your dealer for direct support. Your system has most likely been configured or designed by them and they should have the best idea of what hardware and software your system contains. Hence, they should be of the most assistance for you. Furthermore, if you purchased your system from a dealer near you, take the system to them directly to have it serviced instead of attempting to do so yourself (which can have expensive consequences).

If these options are not available for you then TYAN® Computer Corporation can help. Besides designing innovative and quality products for over a decade, TYAN has continuously offered customers service beyond their expectations. TYAN®'s website (**www.tyan.com**) provides easy-to-access FAQ searches and online Trouble Ticket creation as well as Instant Chat capabilities with our Support Agents. TYAN® also provides easy-to-access resources such as in-depth Linux Online Support sections with downloadable Linux drivers and comprehensive compatibility reports for chassis, memory and much more. With all these convenient resources just a few keystrokes away, users can easily find the latest software and operating system components to keep their systems running as powerful and productive as possible. TYAN® also ranks high for its commitment to fast and friendly customer support through email. By offering plenty of options for users, TYAN® serves multiple market segments with the industry's most competitive services to support them.

"TYAN's tech support is some of the most impressive we've seen, with great response time and exceptional organization in general" - Anandtech.com

Help Resources:

> 1. See the beep codes section of this manual.
> 2. See the TYAN® website for FAQ's, bulletins, driver updates, and other information: **http://www.tyan.com**
> 3. Contact your dealer for help BEFORE calling TYAN®.
> 4. Check the TYAN® user group:
> **alt.comp.periphs.mainboard.TYAN**

Returning Merchandise for Service

During the warranty period, contact your distributor or system vendor FIRST for any product problems. This warranty only covers normal customer use and does not cover damages incurred during shipping or failure due to the alteration, misuse, abuse, or improper maintenance of products.

> **NOTE:**
> A receipt or copy of your invoice marked with the date of purchase is required before any warranty service can be rendered. You may obtain service by calling the manufacturer for a Return Merchandise Authorization (RMA) number. The RMA number Should be prominently displayed on the outside of the shipping carton and the package should be mailed prepaid. TYAN® will pay to have the board shipped back to you.

Notice for the USA
Compliance Information Statement (Declaration of Conformity Procedure) DoC
FCC Part 15: This device complies with part 15 of the FCC Rules

Operation is subject to the following conditions:

This device may not cause harmful interference, and this device must accept any interference received including interference that may cause undesired operation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try one or more of the following measures:
Reorient or relocate the receiving antenna.
Increase the separation between the equipment and the receiver.
Plug the equipment into an outlet on a circuit different from that of the receiver.
Consult the dealer on an experienced radio/television technician for help.

Notice for Canada
This apparatus complies with the Class B limits for radio interference as specified in the Canadian Department of Communications Radio Interference Regulations. (Cet appareil est conforme aux norms de Classe B d'interference radio tel que specifie par le Ministere Canadien des Communications dans les reglements d'ineteference radio.)

CAUTION: Lithium battery included with this board. Do not puncture, mutilate, or dispose of battery in fire. There is danger of an explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by manufacturer. Dispose of used battery according to manufacturer instructions and in accordance with your local regulations.

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