AMD SR5690/5670/5650 Register Reference Guide

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Chapter 1
Introduction

1.1 About This Guide

This manual serves as a register reference guide for the AMD SR5690/5670/5650 ASIC. The differences between these variants are as follows: SR5690 has all the PCIe® ports described in this document; SR5670 does not have PCIE-GPP2 Port 1 and PCIE-GPP3b (therefore, all references to GPP2 Port 1 and GPP3b in this document do not apply to SR5670); SR5650 does not have PCIE-GPP2 and GPP3b (therefore, all references to GPP2 and GPP3b in this document do not apply to SR5650).

Note: Register access should not be attempted to indirect register spaces where that space is not supported for a particular variant, or when the associated component is powered down.

For more details on supported features in each variant, please refer to the SR5690, SR5670 and SR5650 Databooks.

- *Chapter 1* outlines the notations and conventions used throughout this manual.
- *Chapter 2* provides detailed descriptions of the registers.
- *Appendix A* provides two cross-referenced lists of the registers (one sorted by register name and the other by address).

1.2 Nomenclature and Conventions

1.2.1 Register Description Format

All registers in this document are described with the format of the sample table below. All offsets are in hexadecimal notation, while programmed bits are in either binary or hexadecimal notation.

NB_ADAPTER_ID - R - 32 bits - nbconfig:0x2C			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID *(mirror of NB_ADAPTER_ID_W:SUBSYSTEM_VENDOR_ID)*	15:0	0x0	Subsystem vendor ID
SUBSYSTEM_ID *(mirror of NB_ADAPTER_ID_W:SUBSYSTEM_ID)*	31:16	0x0	Subsystem ID
Subsystem Vendor ID and Subsystem ID register			

Register Information	Example
Register name	NB_ADAPTER_ID
Read / Write capability R = Readable W = Writable RW = Readable and Writable	R
Register size	32 bits
Register address(es)*	nbconfig:0x2C

Register Information	Example
Field name	SUBSYSTEM_VENDOR_ID
Field position/size	15:0
Field default value	0x0
Field description	Subsystem vendor ID
Field mirror information	*(mirror of NB_ADAPTER_ID_W:SUBSYSTEM_VENDOR_ID)*
Brief register description	Subsystem Vendor ID and Subsystem ID register
*** Note:** There maybe more than one address; the convention used is as follows: **[aperName:offset]** - single mapping, to one aperture/decode and one offset **[aperName1, aperName2, …, aperNameN:offset]** - multiple mappings to different apertures/decodes but same offset **[aperName:startOffset-endOffset]** - mapped to an offset range in the same aperture/decode	

Warning: Do not attempt to modify the values of registers or bit fields that are marked as "Reserved." Doing so may cause the system to behave in unexpected ways.

1.2.2 Numeric Representations

- Hexadecimal numbers are appended with “h” whenever there is a risk of ambiguity. Other numbers are assumed to be in decimal.

1.2.3 Changes Indication

Changes and additions from the previous release of this document are highlighted in red. Refer to *Appendix B: Revision History* at the end of this manual for a detailed revision history.

Chapter 2
Register Descriptions

2.1 Register Spaces and Device IDs

2.1.1 PCI Configuration Space

The SR5690/5670/5650 places all of its internal devices on the same bus number. By default, the bus number is assigned by the processor based on the first type 0 configuration cycle. The primary SR5690/5670/5650 which attaches to the southbridge must reside on logical PCI bus 0. Base access to PCI configuration space is done via normal HyperTransport™ type 0 configuration cycles. Access to registers in extended configuration space may be done via extended HyperTransport type 0 configuration cycles or via BAR3 memory-mapped cycles.

The following table lists the default assignment of device numbers within the SR5690/5670/5650 as well as any PCI capabilities located in their respective configuration space.

Device	Function	Description	Capabilities
0	0	Host-bridge	HyperTransport, HyperTransport 3, HT Error Retry, HT UnitID Clumping, MSI, MSI Mapping
0	1	Host-bridge + clock configuration controls	None
0	2	IOMMU device	IOMMU, MSI, MSI Mapping
2	0	PCI Express bridge for GPP1 port 0	PCI Express PM, PCI Express, MSI, SSID, MSI Mapping, Advance Error Reporting, Access Control Services
3	0	PCI Express bridge for GPP1 port 1	PCI Express PM, PCI Express, MSI, SSID, MSI Mapping, Advance Error Reporting, Access Control Services
4	0	PCI Express bridge for GPP3a port 0	PCI Express PM, PCI Express, MSI, SSID, MSI Mapping, Advance Error Reporting, Access Control Services
5	0	PCI Express bridge for GPP3a port 1	PCI Express PM, PCI Express, MSI, SSID, MSI Mapping, Advance Error Reporting, Access Control Services
6	0	PCI Express bridge for GPP3a port 2	PCI Express PM, PCI Express, MSI, SSID, MSI Mapping, Advance Error Reporting, Access Control Services
7	0	PCI Express bridge for GPP3a port 3	PCI Express PM, PCI Express, MSI, SSID, MSI Mapping, Advance Error Reporting, Access Control Services
8	0	Transparent bridge to SB – normally hidden	
9	0	PCI Express bridge for GPP3a port 4	PCI Express PM, PCI Express, MSI, SSID, MSI Mapping, Advance Error Reporting, Access Control Services
10	0	PCI Express bridge for GPP3a port 5	PCI Express PM, PCI Express, MSI, SSID, MSI Mapping, Advance Error Reporting, Access Control Services

11**	0	PCI Express bridge for GPP2 port 0	PCI Express PM, PCI Express, MSI, SSID, MSI Mapping, Advance Error Reporting, Access Control Services
12*	0	PCI Express bridge for GPP2 port 1	PCI Express PM, PCI Express, MSI, SSID, MSI Mapping, Advance Error Reporting, Access Control Services
13*	0	PCI Express bridge for GPP3b port 0	PCI Express PM, PCI Express, MSI, SSID, MSI Mapping, Advance Error Reporting, Access Control Services
* Not present in SR5670 and SR5650 ** Not present in SR5650			

2.1.2 Memory-Mapped Register Spaces

The SR5690/5670/5650 contains 2 memory-mapped register spaces.

Register Space	BAR Location	Description
iommummreg	Device 0 Function 2 Register 0x44 and 0x48	IOMMU memory-mapped registers
ioapicmmreg	ioapicind 0x1 and 0x2	IOAPIC memory-mapped registers

2.1.3 Indirect Register Spaces

The SR5690/5670/5650 contains several indirect register spaces accessed via index/data pairs in the PCI configuration space or in memory-mapped space.

Indirect Space	Index/Data Location	Description
Nbmiscind	Dev0, Fn0, Reg 0x60 / 0x64	Miscellaneous registers
Htiunbind	Dev0, Fn0, Reg 0x94 / 0x98	HyperTransport controls
ioapicind	Dev0, Fn0, Reg 0xF8 / 0xFC	IOAPIC controls
ioapicmmiscind	IOAPIC MM BAR + 0x00 / 0x10	IOAPIC redirection table
Pcieind	Dev0, Fn0, Reg 0xE0 / 0xE4	PCIE per-core controls for GPP1
Pcieind	Dev0, Fn0, Reg 0xE0 / 0xE4	PCIE per-core controls for GPP2
Pcieind	Dev0, Fn0, Reg 0xE0 / 0xE4	PCIE per-core controls for GPP3a
Pcieind *	Dev0, Fn0, Reg 0xE0 / 0xE4	PCIE per-core controls for GPP3b
Pcieind	Dev0, Fn0, Reg 0xE0 / 0xE4	PCIE per-core controls for SB
Pcieind_p	Dev2, Fn0, Reg 0xE0 / 0xE4	PCIE per-port controls for GPP1 port 0
Pcieind_p	Dev3, Fn0, Reg 0xE0 / 0xE4	PCIE per-port controls for GPP1 port 1
Pcieind_p	Dev11, Fn0, Reg 0xE0 / 0xE4	PCIE per-port controls for GPP2 port 0
Pcieind_p*	Dev12, Fn0, Reg 0xE0 / 0xE4	PCIE per-port controls for GPP2 port 1
Pcieind_p	Dev4, Fn0, Reg 0xE0 / 0xE4	PCIE per-port controls for GPP3a port 0
Pcieind_p	Dev5, Fn0, Reg 0xE0 / 0xE4	PCIE per-port controls for GPP3a port 1
Pcieind_p	Dev6, Fn0, Reg 0xE0 / 0xE4	PCIE per-port controls for GPP3a port 2
Pcieind_p	Dev7, Fn0, Reg 0xE0 / 0xE4	PCIE per-port controls for GPP3a port 3
Pcieind_p	Dev9, Fn0, Reg 0xE0 / 0xE4	PCIE per-port controls for GPP3a port 4
Pcieind_p	Dev10, Fn0, Reg 0xE0 / 0xE4	PCIE per-port controls for GPP3a port 5
Pcieind_p *	Dev13, Fn0, Reg 0xE0 / 0xE4	PCIE per-port controls for GPP3b port 0

Pcieind_p	Dev8, Fn0, Reg 0xE0 / 0xE4	PCIE per-port controls for SB
Iommul2ind	Dev0, Fn2, Reg 0xF0 / 0xF4	IOMMU L2 controls
Iommul1ind	Dev0, Fn2, Reg 0xF8 / 0xFC	IOMMU L1 controls for GPP1
Iommul1ind**	Dev0, Fn2, Reg 0xF8 / 0xFC	IOMMU L1 controls for GPP2
Iommul1ind	Dev0, Fn2, Reg 0xF8 / 0xFC	IOMMU L1 controls for GPP3a
Iommul1ind *	Dev0, Fn2, Reg 0xF8 / 0xFC	IOMMU L1 controls for GPP3b
Iommul1ind	Dev0, Fn2, Reg 0xF8 / 0xFC	IOMMU L1 controls for SB
Iommul1ind	Dev0, Fn2, Reg 0xF8 / 0xFC	IOMMU L1 controls for SBVC1
* Not present in SR5670 and SR5650 ** Not present in SR5650		

2.1.4 Vendor and Device IDs

The vendor ID is 0x1002. This is the former ATI vendor ID which is now owned by AMD. AMD officially has two vendor IDs.

Device	Default Location	Device ID
nbconfig host bridge	Device 0 function 0	0x5A10 – SR5690 0x5A12 – SR5670 0x5A13 – SR5650
clkconfig host bridge	Device 0 function 1	0x5A22
IOMMU	Device 0 function 2	0x5A23
PCI Express bridge for GPP1 port 0	Device 2 function 0	0x5A16
PCI Express bridge for GPP1 port 1	Device 3 function 0	0x5A17
PCI Express bridge for GPP3a port 0	Device 4 function 0	0x5A18
PCI Express bridge for GPP3a port 1	Device 5 function 0	0x5A19
PCI Express bridge for GPP3a port 2	Device 6 function 0	0x5A1A
PCI Express bridge for GPP3a port 3	Device 7 function 0	0x5A1B
Transparent bridge to SB – normally hidden	Device 8 function 0	0x5A21
PCI Express bridge for GPP3a port 4	Device 9 function 0	0x5A1C
PCI Express bridge for GPP3a port 5	Device 10 function 0	0x5A1D
PCI Express bridge for GPP2 port 0 **	Device 11 function 0	0x5A1F
PCI Express bridge for GPP2 port 1 *	Device 12 function 0	0x5A20
PCI Express bridge for GPP3b port 0 *	Device 13 function 0	0x5A1E
* Not present in SR5670 and SR5650 ** Not present in SR5650		

2.1.5 Subsystem Vendor and Subsystem IDs

Both the subsystem vendor ID and subsystem ID are writeable by system BIOS during POST based on the OEM's vendor and subsystem ID. Nbconfig, clkconfig, and all PCIe® bridges have their subsystem vendor ID and subsystem ID tied together (writeable via device 0 function 0 register 0x50). IOMMU has a separate register to control subsystem vendor ID and subsystem ID (writeable via device 0 function 2 register 0x68).

2.2 Configuration Space Registers

2.2.1 NBCONFIG Registers

NB_VENDOR_ID - R - 16 bits - nbconfig:0x0			
Field Name	**Bits**	**Default**	**Description**
VENDOR_ID	15:0	0x1002	Vendor Identifier This 16-bit field identifies the manufacturer of the device: Advanced Micro Devices, Inc.

NB_DEVICE_ID - R - 16 bits - nbconfig:0x2			
Field Name	**Bits**	**Default**	**Description**
DEVICE_ID	15:0	0x5A10 for SR5690 0x5A12 for SR5670 0x5A13 for SR5650	Device Identifier This 16-bit field is assigned by the device manufacturer and identifies the type of device.

NB_COMMAND - RW - 16 bits - nbconfig:0x4			
Field Name	**Bits**	**Default**	**Description**
IO_ACCESS_EN	0	0x0	I/O Access Enable This register controls no hardware. This function does not respond to I/O cycles.
MEM_ACCESS_EN	1	0x0	Memory Access Enable Controls access to memory-mapped I/O space via local BAR registers. 0=Disable 1=Enable
BUS_MASTER_EN	2	0x0	Bus Master Enable This register controls no hardware. This function does not generate its own DMA requests.
RESERVED_RO_3 (R)	3	0x0	This bit is always 0 for HyperTransport devices. 0=Disable 1=Enable
RESERVED_RO_4 (R)	4	0x0	This bit is always 0 for HyperTransport devices. 0=Disable 1=Enable
RESERVED_RO_5 (R)	5	0x0	This bit is always 0 for HyperTransport devices. 0=Disable 1=Enable
PARITY_ERROR_EN (R)	6	0x0	Parity Error Response This bit is always 0 because this function does not log errors in the master data error register.
Reserved0 (R)	7	0x0	This bit is always 0 for HyperTransport devices. 0=Disable 1=Enable
SERR_EN	8	0x0	System Error Enable Enables hardware to set SIGNALED_SYSTEM_ERROR and enables HyperTransport to initiate a sync flood. 0=Disable 1=Enable

RESERVED_RO_9 (R)	9	0x0	This bit is always 0 for HyperTransport devices. 0=Disable 1=Enable
INTERRUPT_DISABLE	10	0x0	Disables legacy interrupt generation for HyperTransport and internal parity errors. 0=Legacy interrupts enabled 1=Legacy interrupts disabled
Reserved (R)	15:11	0x0	

NB_STATUS - RW - 16 bits - nbconfig:0x6			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_STATUS (R)	3	0x0	Interrupt Status This bit indicates whether the function has an unserviced interrupt. This register indicates the interrupt status in both legacy and MSI modes
CAP_LIST (R)	4	0x1	Capabilities List This bit is set to indicate that this device's configuration space supports a capabilities list.
RESERVED_RO_5 (R)	5	0x0	This bit is always 0 for HyperTransport devices.
Reserved (R)	6	0x0	This bit is always 0 for HyperTransport devices.
RESERVED_RO_7 (R)	7	0x0	This bit is always 0 for HyperTransport devices.
MASTER_DATA_ERROR (R)	8	0x0	Master Data Error This function does not set the master data error status bit because it does not accept dma read responses.
RESERVED_RO_10_9 (R)	10:9	0x0	This field is always 0 for HyperTransport devices.
SIGNAL_TARGET_ABORT (R)	11	0x0	Signaled Target Abort This bit is always 0 because this device does not terminate transactions with target aborts.
RECEIVED_TARGET_ABORT	12	0x0	Received Target Abort This bit is set by whenever a host transaction to the southbridge port is terminated due to a target-abort. This bit is cleared by writing a 1. 0=Inactive 1=Active
RECEIVED_MASTER_ABORT	13	0x0	Received Master Abort This bit is set whenever a host transaction to the southbridge port is terminated due to a master-abort. This bit is cleared by writing a 1. 0=Inactive 1=Active
SIGNALED_SYSTEM_ERROR	14	0x0	Signaled System Error This bit is set whenever SERR_EN is set and the device generates a System Error. This bit is cleared by writing a 1. 0=No Error 1=SERR asserted
DATA_ERROR_DETECTED (R)	15	0x0	Data Error Detected This bit is always 0 because this function does not log the receipt of poisoned data targetting the function's BARs.
General NB status Flags			

NB_REVISION_ID - R - 8 bits - nbconfig:0x8			
Field Name	**Bits**	**Default**	**Description**
MINOR_REV_ID	3:0	0x0	Identifies the stepping number of the device
MAJOR_REV_ID	7:4	0x0	Identifies the revision number of the device
Revision Identification			

NB_REGPROG_INF - R - 8 bits - nbconfig:0x9			
Field Name	**Bits**	**Default**	**Description**
REG_LEVEL_PROG_INF	7:0	0x0	Indicates a Host bridge device.
Program Interface			

NB_SUB_CLASS - R - 8 bits - nbconfig:0xA			
Field Name	**Bits**	**Default**	**Description**
SUB_CLASS_INF	7	0x0	Indicates a Host bridge device.
Sub-Class Code			

NB_BASE_CODE - R - 8 bits - nbconfig:0xB			
Field Name	**Bits**	**Default**	**Description**
BASE_CLASS_CODE	7:0	0x6	Indicates a Bridge device
Class Code			

NB_CACHE_LINE - R - 8 bits - nbconfig:0xC			
Field Name	**Bits**	**Default**	**Description**
CACHE_LINE_SIZE	7:0	0x0	This field is always 0 for HyperTransport devices.
Cache Line Size			

NB_LATENCY - R - 8 bits - nbconfig:0xD			
Field Name	**Bits**	**Default**	**Description**
LATENCY_TIMER	7:0	0x0	This field is always 0 for HyperTransport devices.
Latency Timer			

NB_HEADER - R - 8 bits - nbconfig:0xE			
Field Name	**Bits**	**Default**	**Description**
HEADER_TYPE	6:0	0x0	Bits [6:5] are 0, indicating that Type 00 Configuration Space Header format is supported.
DEVICE_TYPE	7	0x1	Bit [7] is 1 to indicate a multi-function device. 0=Single-Function Device 1=Multi-Function Device
Header Type			

NB_BIST - R - 8 bits - nbconfig:0xF			
Field Name	**Bits**	**Default**	**Description**
BIST_COMP	3:0	0x0	This field is always 0 for HyperTransport devices.
BIST_STRT	6	0x0	This field is always 0 for HyperTransport devices.
BIST_CAP	7	0x0	This field is always 0 for HyperTransport devices.
Built-in-self-test			

NB_BAR1_RCRB - RW - 32 bits - nbconfig:0x14			
Field Name	**Bits**	**Default**	**Description**
MEM_IO (R)	0	0x0	Memory: This bit is hardwired to 0 to indicate that this base address register maps into memory space 0=Memory 1=I/O
TYPE (R)	2:1	0x0	Type: This bit field is hardwired to indicate that this base register is 32 bits wide and mapping can be performed anywhere in the 32-bit address space
PREFETCH_EN (R)	3	0x0	Unprefetchable: This bit is hardwired to 0 to indicate that this range is un-prefetchable
RCRB_BASE	31:12	0x0	Base Address High[31:12] This filed is used to define a 4K memory mapped root complex register block
Descriptor for memory mapped RCRB registers			

NB_BAR2_PM2 - RW - 32 bits - nbconfig:0x18			
Field Name	**Bits**	**Default**	**Description**
MEM_IO (R)	0	0x1	I/O Space: This bit is hardwired to 1 to indicate that this base address register maps into x86 I/O space. 0=Memory 1=I/O
RESERVED (R)	1	0x0	
PM2_BASE_LOW (R)	4:2	0x0	This field specifies that there are 8 DWORD registers allocated to this space.
PM2_BASE	31:5	0x0	PM2_BLK Base: This bit field forms the upper part of BAR2. This field is loaded by BIOS software and specifies the base of PM2_BLK.
Descriptor for Power management PM2 Control Block			

NB_BAR3_PCIEXP_MMCFG - RW - 32 bits - nbconfig:0x1C			
Field Name	**Bits**	**Default**	**Description**
MEM_IO (R)	0	0x0	Memory: This bit is hardwired to 0 to indicate that this base address register maps into memory space 0=Memory 1=I/O
TYPE (R)	2:1	0x2	Type: This bit field is hardwired to 2'b10 to indicate that this base register is 64 bits wide and mapping can be performed anywhere in the 64-bit address space
PREFETCH_EN (R)	3	0x0	Prefetchable: This bit is hardwired to 1 to indicate that this range is prefetchable
MEM_BASE_LOW (R)	20:4	0x0	Base Address Low This bit field is hardwired to return zeros to indicate that xx Kbytes are allocated to PCI Express Configuration Registers.
MEM_BASE_HIGH	31:21	0x0	Base Address High This bit field forms the upper part of BAR3. This field is loaded by BIOS software
Descriptor for memory mapped PCI Express Configuration registers			

NB_BAR3_UPPER_PCIEXP_MMCFG - RW - 32 bits - nbconfig:0x20			
Field Name	**Bits**	**Default**	**Description**
MEM_BASE_UPPER	31:0	0x0	Upper 32 bit of BAR3 base address
Descriptor for upper part of memory mapped PCI Express Configuration registers			

NB_ADAPTER_ID - R - 32 bits - nbconfig:0x2C			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID *(mirror of NB_ADAPTER_ID_W:SUBSYSTEM_VENDOR_ID)*	15:0	0x0	Subsystem vendor ID
SUBSYSTEM_ID *(mirror of NB_ADAPTER_ID_W:SUBSYSTEM_ID)*	31:16	0x0	Subsystem ID
Subsystem Vendor ID and Subsystem ID register			

NB_CAPABILITIES_PTR - R - 32 bits - nbconfig:0x34			
Field Name	**Bits**	**Default**	**Description**
CAP_PTR	7:0	0xf0	This field contains a byte offset into a device's configuration space containing the first item in the capabilities list.
Capabilities Pointer			

NB_INTERRUPT_LINE - RW - 8 bits - nbconfig:0x3C			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_LINE	7:0	0x0	This field is read-write for software purposes but controls no hardware.

NB_INTERRUPT_PIN - R - 8 bits - nbconfig:0x3D			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_PIN	7:0	0x0	This field indicates the INTx line used to generate legacy interrupts. 0=No legacy interrupt supported 1=INTA 2=INTB 3=INTC 4=INTD All other encodings are not supported.
Interrupt Pin			

NB_HT_ERROR_RETRY_CAPABILITY - R - 32 bits - nbconfig:0x40			
Field Name	**Bits**	**Default**	**Description**
CAPABILITY_ID	7:0	0x8	Indicates that this is a HyperTransport capability
CAPABILITY_POINTER	15:8	0x54	Pointer to the next configuration space capability
RESERVED	26:16	0x0	Reserved for future use. This register controls no hardware
CAPABILITY_TYPE	31:27	0x18	Indicates that this is the HyperTransport Error Retry capability

NB_HT_ERROR_RETRY_CONTROL_STATUS - RW - 32 bits - nbconfig:0x44			
Field Name	**Bits**	**Default**	**Description**
LINK_RETRY_EN_0	0	0x0	Enables Error Retry Mode. This register requires a warm-reset to take effect
FORCE_SINGLE_ERROR_0	1	0x0	Forces an upstream error on the HyperTransport link. This register is automatically cleared by hardware
ROLLOVER_NONF_EN_0 (R)	2	0x0	Triggers a non-fatal interrupt to be generated when the error retry counter overflows
FORCE_SINGLE_STOMP_0	3	0x0	Forces an upstream stomp packet on the HyperTransport link. This register is automatically cleared by hardware
RETRY_NONF_EN_0 (R)	4	0x0	Triggers a non-fatal interrupt to be generated when an error retry event occurs
RETRY_FATAL_EN_0 (R)	5	0x0	Triggers a fatal interrupt to be generated when an error retry event occurs
ALLOWED_ATTEMPTS_0	7:6	0x3	Indicates the number of short training attempts to make before attempting full training.
RETRY_SENT_0	8	0x0	Indicates the link sent a disconnect Nop to initiate a retry sequence. Write 1 to clear
COUNT_ROLLOVER_0	9	0x0	Indicates the retry counter has rolled over. Write 1 to clear
STOMP_RECEIVED_0	10	0x0	Indicates that a stomp packet has been received. Write 1 to clear
RESERVED_15_11 (R)	15:11	0x0	Reserved for future use. This register controls no hardware
reserved_23_16 (R)	23:16	0x0	Reserved for future use. This register controls no hardware
reserved_31_24 (R)	31:24	0x0	Reserved for future use. This register controls no hardware

NB_HT_ERROR_RETRY_COUNT - RW - 32 bits - nbconfig:0x48			
Field Name	**Bits**	**Default**	**Description**
RETRY_COUNT_0	15:0	0x0	Indicates the number of retry sequences the hardware has made
reserved_31_16 (R)	31:16	0x0	Reserved for future use. This register controls no hardware

NB_PCI_CTRL - RW - 32 bits - nbconfig:0x4C			
Field Name	**Bits**	**Default**	**Description**
FUNCTION_1_ENABLE	0	0x0	Enables access to Device 0 Function 1 0=Disable 1=Enable
APIC_ENABLE	1	0x1	Reserved for future use. This register controls no hardware 0=Disable 1=Enable
AlwaysUnLk	2	0x1	If set, always issues UnLk request for cpu lock transaction. If not set, only issues UnLk when RdLk is successful. This is a legacy register that should always be set to 0. This device does not issue locked transactions. 0=Disable 1=Enable
Cf8Dis	3	0x0	Disables I/O port 0xCF8 cycle decoding to configuration space. This is a legacy control register that should always be set to 0. This device does not expect to see I/O access to port 0xCF8. Instead it expects to see HyperTransport configuration cycles. 0=Enable 1=Disable
PMEDis	4	0x0	Disables PME message generation to the southbridge 0=Enable 1=Disable
SErrDis	5	0x0	Disables SERR in-band message generation to the southbridge 0=Enable 1=Disable
BMMsgEn	6	0x0	Enables BM_Set message generation to the southbridge 0=Disable 1=Enable
DisLockP2P	7	0x0	If set, p2p requests can be interleaved into MemRdLk sequences. If clear, p2p requests are blocked during cpu lock transactions. This is a legacy register that should always be set to 0. This device does not issue locked transactions. 0=Enable 1=Disable
PMArbDisSel	10:8	0x0	Setting bit [0] will disable BIF request when PMArbDis is set. Setting bit [1] will disable rx0(graphics PCIe®) DMA request when PMArbDis is set. Setting bit [2] will disable rx1(SB and general purpose PCIe) DMA request when PMArbDis is set
CsrStatus	11	0x0	1=CSR is detected. Write 1 to clear this bit. Writiong 0 has no effect 0=Inactive 1=Active
CfgRdTime	14:12	0x2	3-bit setting for RBBM read data bus data latch latency
P2PDynamicClkOff	15	0x0	If set to 1, the IOC dynamic clock must be running in order to support p2p traffic 0=Enable 1=Disable
WakeC2En	16	0x0	Enables Wake_from_C2 message to be issued to the southbridge whenever interrupts are received 0=Enable 1=Disable

BAR2_PM2Enable	17	0x0	Enables read/write access to NB_BAR2_PM2 register; Clearing this bit hides BAR2 0=Disable 1=Enable
P4IntEnable	18	0x0	Forces 0xFEEx_xxxx cycles to be forwarded upstream to system memory. This is a legacy register that should always be set to 0. 0=Disable 1=Enable
SLPEnable	20	0x0	This register controls no hardware 0=Enable 1=Disable
SLP_Pad_Enable	21	0x0	This register controls no hardware 0=Enable 1=Disable
BAR1_Enable	22	0x0	Enables read/write access to NB_BAR1_RCRB register; Clearing this bit hides BAR1 0=Enable 1=Disable
MMIOEnable	23	0x0	Enables MMIO decoding. The MMIOBase and MMIOLimit registers will be used to mark off a memory-mapped I/O range and prevent requests in this range from being decoded as system memory addresses 0=Enable 1=Disable
IsocArbMode	24	0x0	This register controls no hardware 0=Enable 1=Disable
IsocHiPr	25	0x0	This register controls no hardware 0=Enable 1=Disable
HPDis	26	0x0	Disables HotPlug message generation to the southbridge 0=Enable 1=Disable
PCI Control Register			

NB_ADAPTER_ID_W - RW - 32 bits - nbconfig:0x50			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID	15:0	0x1002	Values written into this register are reflected in the subsystem vendor ID
SUBSYSTEM_ID	31:16	0x5a10	Values written into this register are reflected in the subsystem ID
Subsystem Vendor ID and Subsystem ID write register			

NB_UNITID_CLUMPING_CAPABILITY - R - 32 bits - nbconfig:0x54			
Field Name	**Bits**	**Default**	**Description**
CAPABILITY_ID	7:0	0x8	Indicates that this is a HyperTransport capability
CAPABILITY_POINTER	15:8	0x9c	Pointer to the next configuration space capability
RESERVED	26:16	0x0	Reserved for future use. This register controls no hardware
CAPABILITY_TYPE	31:27	0x12	Indicates this is the UnitID Clumping capability

NB_UNITID_CLUMPING_SUPPORT - R - 32 bits - nbconfig:0x58			
Field Name	**Bits**	**Default**	**Description**
RESERVED_0	0	0x0	Reserved for future use. This register controls no hardware
SUPPORT	31:1	0x0	Indicates which on-board UnitIDs support the HyperTransport clumping capability

NB_UNITID_CLUMPING_ENABLE - RW - 32 bits - nbconfig:0x5C			
Field Name	**Bits**	**Default**	**Description**
RESERVED_0 (R)	0	0x0	Reserved for future use. This register controls no hardware
ENABLE	31:1	0x0	Enables clumping for selected UnitIDs. See the *AMD* SR5690/5670/5650 *Register Programming Requirements* document on how to enable this feature

NB_MISC_INDEX - RW - 32 bits - nbconfig:0x60			
Field Name	**Bits**	**Default**	**Description**
NB_MISC_IND_ADDR	6:0	0x0	Sets the register address used to access the NBMISCIND indirect register space
NB_MISC_IND_WR_EN	7	0x0	Northbridge Misc. index register write enable 0=Disable writes to NB_MISC_DATA 1=Enable writing to NB_MISC_DATA

Northbridge Misc. index register address and write enable

NB_MISC_DATA - RW - 32 bits - nbconfig:0x64			
Field Name	**Bits**	**Default**	**Description**
NBMISCDATA	31:0	0x0	Read/Write register data for the NBMISCIND register indicated by NB_MISC_INDEX:NB_MISC_IND_ADDR

HT_PARITY_ERR_CONTROL_STATUS - RW - 32 bits - nbconfig:0x68			
Field Name	**Bits**	**Default**	**Description**
NON_FATAL_HT_ERR (R)	0	0x0	Asserted to indicate the detection of a non-fatal HT error. This register merges multiple HT error status bits that are mapped onto the non-fatal error interrupt condition.
FATAL_HT_ERR (R)	1	0x0	Asserted to indicate the detection of a fatal HT error. This register merges multiple HT error status bits that are mapped onto the fatal error interrupt condition.
NON_FATAL_HT_ERR_MSI_MSG_NUMBER	3:2	0x0	Indicates to software which MSI interrupt vector is used for non-fatal HyperTransport error interrupts. Hardware assigns this register depending on the value of the multiple message enable field in the MSI capability header.
FATAL_HT_ERR_MSI_MSG_NUMBER	5:4	0x0	Indicates to software which MSI interrupt vector is used for fatal HyperTransport error interrupts. Hardware assigns this register depending on the value of the multiple message enable field in the MSI capability header.

CORR_PARITY_ERR (R)	8	0x0	Indicates the detection of a correctable parity error. This is the OR of the individual memory macro parity error detection bits in htiunbind space that are mapped onto the correctable error condition.
NON_FATAL_PARITY_ERR (R)	9	0x0	Indicates the detection of a non-fatal parity error. This is the OR of the individual memory macro parity error detection bits in htiunbind space that are mapped onto the non-fatal error condition.
FATAL_PARITY_ERR (R)	10	0x0	Indicates the detection of a fatal parity error. This is the OR of the individual memory macro parity error detection bits in htiunbind space that are mapped onto the fatal error condition.
HT_PARITY_INTX_MSG	14:12	0x0	This register changes the value in the INTERRUPT_PIN register and determines which INTx message HT and parity errors use. 0=No legacy interrupts supported 1=INTA 2=INTB 3=INTC 4=INTD
HT_MSI_REMAP	15	0x0	
CORR_PARITY_ERR_REP_EN	16	0x0	Enables interrupt generation when CORR_PARITY_ERR is set
NON_FATAL_PARITY_ERR_REP_EN	17	0x0	Enables interrupt generation when NON_FATAL_PARITY_ERR is set
FATAL_PARITY_ERR_REP_EN	18	0x0	Enables interrupt generation when FATAL_PARITY_ERR is set
SERR_ON_CORR_PARITY_ERR	19	0x0	When set, SERR# is signalled through the signalled system error status bit upon the detection of a correctable parity error
SERR_ON_NON_FATAL_PARITY_ERR	20	0x0	When set, SERR# is signalled through the signalled system error status bit upon the detection of a non-fatal parity error
SERR_ON_FATAL_PARITY_ERR	21	0x0	When set, SERR# is signalled through the signalled system error status bit upon the detection of a fatal parity error
CORR_PARITY_ERR_MSI_MSG_NUMBER	23:22	0x0	Indicates to software which MSI interrupt vector is used for correctable parity error interrupts. Hardware assigns this register depending on the value of the multiple message enable field in the MSI capability header.
NON_FATAL_PARITY_ERR_MSI_MSG_NUMBER	25:24	0x0	Indicates to software which MSI interrupt vector is used for non-fatal parity error interrupts. Hardware assigns this register depending on the value of the multiple message enable field in the MSI capability header.
FATAL_PARITY_ERR_MSI_MSG_NUMBER	27:26	0x0	Indicates to software which MSI interrupt vector is used for fatal parity error interrupts. Hardware assigns this register depending on the value of the multiple message enable field in the MSI capability header.
IOMMU_CACHE_PARITY_ERR_MAP	29:28	0x0	Determines how IOMMU cache parity errors are mapped onto parity error status registers 00=Correctable 01=Non-fatal 10=Fatal 11=Reserved
PARITY_ERR_MAP	31:30	0x1	Determines how non-IOMMU-cache internal parity errors are mapped onto parity error status registers 00=Reserved 01=Non-fatal 10=Fatal 11=Reserved
HyperTransport and Parity Error Control			

MSI_CAPABILITY_POINTER_0 - RW - 32 bits - nbconfig:0x70			
Field Name	**Bits**	**Default**	**Description**
CAPABILITY_ID (R)	7:0	0x5	Indicates that this is the MSI capability
NEXT_POINTER (R)	15:8	0x0	Pointer to the next configuration space capability
MSI_ENABLE	16	0x0	Enables MSI for this function and causes legacy interrupts to be disabled
MULTIPLE_MESSAGE_CAPABLE (R)	19:17	0x2	Indicates the number of MSI messages requested by this function
MULTIPLE_MESSAGE_ENABLE	22:20	0x0	Sets the number of MSI messages assigned to this function
CAP_64b (R)	23	0x0	Clear to indicate that only a 32-bit MSI address is supported
Reserved (R)	31:24	0x0	
MSI Control Register			

MSI_CAPABILITY_POINTER_1 - RW - 32 bits - nbconfig:0x74			
Field Name	**Bits**	**Default**	**Description**
Reserved (R)	1:0	0x0	
MSG_ADDRESS	31:2	0x0	Determines the address used to issue MSI messages.

MSI_CAPABILITY_POINTER_2 - RW - 32 bits - nbconfig:0x78			
Field Name	**Bits**	**Default**	**Description**
MSG_DATA	15:0	0x0	Determines the data value used with MSI messages. The lower bits may be overriden by hardware if multiple messages are enabled.

NB_IOC_CFG_CNTL - RW - 32 bits - nbconfig:0x7C			
Field Name	**Bits**	**Default**	**Description**
FORCE_INTGFX_DISABLE	0	0x0	Reserved for future use. This register controls no hardware. 0=Normal 1=DISABLE
CFG_Q_F1000_800	1	0x0	Reserved for future use. This register controls no hardware. 0=Disable 1=Enable
F1000_800_en	2	0x0	Reserved for future use. This register controls no hardware. 0=Disable 1=Enable
spare_29_0	29:3	0x0	Reserved for future use. This register controls no hardware.
NB_BAR3_PCIEXP_REG_WREN	30	0x0	Enables writes to the BAR3 register 0=Disable 1=Enable
IOC CFG control register			

SCRATCH_NBCFG - RW - 32 bits - nbconfig:0x80			
Field Name	**Bits**	**Default**	**Description**
SCRATCH	31:0	0x0	This register may be used by system software for scratch purposes. It does not control any hardware.
This register is used for scratch reading and writing			

NB_PCI_ARB - RW - 32 bits - nbconfig:0x84			
Field Name	**Bits**	**Default**	**Description**
RCRB_ENABLE	0	0x0	Enables RCRB memory mapped cfg access through BAR1. This is a legacy register that should always be set to 0 0=Disable 1=Enable
PM2_SB_ENABLE	2	0x0	Enables PM2_CNTL(BAR2) IO mapped cfg write access to be broadcast to both the northbridge and the southbridge. 0=Disable 1=Enable
EV6MODE	4	0x0	EV6 Mode: Creates a hole in memory between 640K and 1M for memory-mapped I/O. This affects DMA requests attempting to access system memory 0=Enable 1=Disable
_14M_HOLE	5	0x0	14M Memory Hole: Creates a hole in memory from 14 Mb to 15 Mb. This affects DMA requests attempting to access system memory 0=Disable 1=Enable
_15M_HOLE	6	0x0	15M Memory Hole: Creates a hole in memory from 15 Mb to 16 Mb. This affects DMA requests attempting to access system memory 0=Disable 1=Enable
PM_REG_ENABLE	7	0x0	Power Management Register Enable: Enables BAR2 IO access decoding. 0=Disable 1=Enable
PMEMode	8	0x0	PME message mode: 0=PME_Turn_Off is triggered by receipt of a PME_Turn_Off message from the southbridge. 1=PME_Turn_Off is triggered by writing 1 to PMETurnOff. 0=Disable 1=Enable
PMETurnOff	9	0x0	PME_Turn_Off message trigger: In case PMEMode is set, writing 1 to this bit will trigger a PME_Turn_Off messages to all connected downstream PCI Express ports. This bit is reset only when the system powered is off. 0=Disable 1=Enable
PMETOAckStatus (R)	10	0x0	Set when all connected downstream PCI Express ports return PMETOAck after PME_Turn_Off is sent
READ_DATA_ERROR_DISABLE	12	0x0	Reserved for future use. This register controls no hardware.

MDA_DEBUG	15	0x0	MDA Debug: Allows monochrome display adapters (MDA) to be used simultaneously with PCI Express cards for the debug of display drivers. The behavior depends on the value of the VGA Enable in any of the PCI Express bridges MDA Address Ranges: Memory: 0B0000h-0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh VGA=0, MDA=0: All MDA and VGA references go to the southbridge VGA=0, MDA=1: Operation undefined VGA=1, MDA=0: All VGA references go to PCI Express, MDA only (I/O 3BFh) goes to the southbridge VGA=1, MDA=1: All VGA references go to PCI Express, All MDA (including memory) goes to the southbridge 0=Disable 1=Enable
BAR3BusRange	18:16	0x0	0 - BAR3[27:20] are all used for bus number decoding so BAR3 memory map range is decoded down to bit 28. 1 - BAR3[20] is used for bus number decoding so memory map range is down to bit 21. 2 - BAR3[21:20] are used for bus number decoding so memory map range is down to bit 22. 3 - BAR3[22:20] are used for bus number decoding so memory map range is down to bit 23. ... 7 - BAR3[26:20] are used for bus number decoding so memory map range is down to bit 27.
AGP_VGA_BIOS	31:24	0x3	AGP VGA BIOS: Indicate that the corresponding (16K) segment should be mapped to PCI Express bridge 2. Bit [24] corresponds to the addresses 0xC0000-0xC3FFF and bit [31] maps addresses 0xDC000-0xDFFFF to bridge 2's PCI Express® interface. This register controls a legacy address decoder and generally does not need to be programmed
This register provides general PCI arbiter mode control			

NB_CFG_STAT - RW - 32 bits - nbconfig:0x88			
Field Name	**Bits**	**Default**	**Description**
CPU_DIVIDER (R)	3:0	0x0	Reserved for future use. This register controls no hardware.
OUT_CLK_DELAY (R)	4	0x0	Reserved for future use. This register controls no hardware.
IN_CLK_DELAY (R)	5	0x0	Reserved for future use. This register controls no hardware.
Reserved0 (R)	7	0x0	Reserved for future use. This register controls no hardware.
FAMILY_ID	15:8	0x0	Family ID
Reserved1 (R)	17:16	0x0	Reserved for future use. This register controls no hardware.
SYS_CLK_MUX (R)	28:26	0x0	Reserved for future use. This register controls no hardware.

NB_TOP_OF_DRAM_SLOT1 - RW - 32 bits - nbconfig:0x90			
Field Name	**Bits**	**Default**	**Description**
TOP_OF_DRAM	31:23	0x0	This register is used to define the top of system memory below 4G. The address is exclusive and must be set just above the top of physical memory below 4G. DMA requests that are not peer-to-peer that miss system memory may be aborted depending on the DMA routing mode.

Top of system memory below 4G.

HTIU_NB_INDEX - RW - 32 bits - nbconfig:0x94			
Field Name	**Bits**	**Default**	**Description**
HTIU_NB_IND_ADDR	7:0	0x0	Sets the register address used to access the HTIUNBIND indirect register space
HTIU_NB_IND_WR_EN	8	0x0	0=Disable writes to HTIU_NB_DATA 1=Enable writing to HTIU_NB_DATA

HTIU_NB_DATA - RW - 32 bits - nbconfig:0x98			
Field Name	**Bits**	**Default**	**Description**
HTIU_NB_DATA	31:0	0x0	Read/Write register data for the HTIUNBIND register indicated by HTIU_NB_INDEX:HTIU_NB_IND_ADDR

NB_HT3_CAPABILITY - RW - 32 bits - nbconfig:0x9C			
Field Name	**Bits**	**Default**	**Description**
CAPABILITY_ID (R)	7:0	0x8	Indicates that this is a HyperTransport capability
CAPABILITY_POINTER (R)	15:8	0x70	Pointer to the next configuration space capability
REG_IND	17:16	0x0	Index 00=HyperTransport 3 Configuration Registers 01=Receiver BIST Registers 10=Transmitter BIST Registers
UCC (R)	18	0x1	Indicates support for unthrottled commands
BIST_CAP (R)	19	0x1	Indicates support for the BIST feature
CPIC (R)	20	0x1	Indicates support for the command packet insertion feature
LS3C (R)	21	0x1	Indicates support for the LS3 low-power link state
RESERVED (R)	23:22	0x0	Reserved for future use
CAPABILITY_TYPE (R)	31:24	0xd0	Indicates that this is the HyperTransport 3 capability

NB_HT3_GLOBAL_LINK_TRAIN - RW - 32 bits - nbconfig:0xA0			
Field Name	**Bits**	**Default**	**Description**
T0_TIME	5:0	0x3a	Defines the amount of time spent in the Training 0 state after recovering from LDTSTOP. See the HyperTransport 3 specification for the encoding

InLnLSSt	7:6	0x0	Inactive Lane State 00=CAD/CTL driven to logic 0. CLK running 01=Same as PHY OFF 10=Same as operational. CAD/CTL driving undefined scrambled data 11=Same as Disconnected - set as per the LSSel register
CONNDLY	8	0x0	Connect Delay. Delays the effects of TXOFF until LDTSTOP or Warm Reset
RXCALEE	9	0x0	This register controls no hardware
RETRYFORCE	11:10	0x0	Retry Force 00=No forced retries 01=Force retry every 250us 10=Force retry every 500us 11=Force retry every 1ms
reserved_12 (R)	12	0x0	Reserved for future use. This register controls no hardware
RSV_31_13	31:13	0x0	Reserved for future use. This register controls no hardware

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b00, the register name is NB_HT3_GLOBAL_LINK_TRAIN and the fields are as defined in the above table.

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b01, the register name and fields are defined as follows:

NB_HT3_Receiver_Pattern_control:

FieldName	Bits	Default
Order	2:0	0x0
PatCnt	9:3	0X0
ModSel	12:10	0X0
ModCnt	19:13	0X0
ConstSel	20	0X0
ConstCnt	25:21	0X0
Reserved (Access R)	31:26	0X0

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b10, the register name and fields are defined as follows:

NB_HT3_Transmitter_Pattern_control:

FieldName	Bits	Default
Order	2:0	0x0
PatCnt	9:3	0x0
ModSel	12:10	0x0
ModCnt	19:13	0x0
ConstSel	20	0x0
ConstCnt	25:21	0x0
Reserved (Access R)	31:26	0x0

NB_HT3_LINK_TRANSMITTER_CONF_0 - RW - 32 bits - nbconfig:0xA4			
Field Name	**Bits**	**Default**	**Description**
DP1	4:0	0x0	Reserved for future use. This register controls no hardware
reserved_12_5	12:5	0x0	Reserved for future use. This register controls no hardware
COMPLIANCE	15:13	0x0	DC Compliace Test 000=Normal Operation 001=Send TxHiZ 010=Send TxL0 Logic 0 011=Send TxL1 Logic 1 100=Reserved 101=Send TxIdle 110=Reserved 111=Reserved
MARGIN_LEVEL	18:16	0x0	Sets the transmitter attenuation level 0=No attenuation
rsv_20_19 (R)	20:19	0x0	Reserved for future use. This register controls no hardware
RSV_23_21	23:21	0x0	Reserved for future use. This register controls no hardware
DL1	27:24	0x5	Sets the transmitter deemphasis level
rsv_28_27 (R)	28	0x0	Reserved for future use. This register controls no hardware
RSV_29 (R)	29	0x0	Reserved for future use. This register controls no hardware
PREEN	30	0x0	Reserved for future use. This register controls no hardware
DEEMPEN	31	0x0	Enables transmitter post-cursor deemphasis

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b00, the register name is NB_HT3_LINK_TRANSMITTER_CONF_0 and the fields are as defined in the above table.

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b01, the register name and fields are defined as follows:

NB_HT3_Receiver_Pattern_Buffer_1:

FieldName	Bits	Default
Pattern_1	23:0	0x0
Reserved (Access R)	31:24	0x0

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b10, the register name and fields are defined as follows:

NB_HT3_Transmitter_Pattern_Buffer_1:

FieldName	Bits	Default
Pattern_1	23:0	0x0
Reserved (Access R)	31:24	0x0

NB_HT3_LINK_RECEIVER_CONF_0 - RW - 32 bits - nbconfig:0xA8			
Field Name	**Bits**	**Default**	**Description**
COMPLIANCE	1:0	0x0	Receiver Compliace 00=Normal Operation 01=Reserved 10=RxOff 11=Reserved
RESERVED_7_2 (R)	7:2	0x0	Reserved for future use. This register controls no hardware
EQLvL (R)	9:8	0x0	Reserved for future use. This register controls no hardware
RESERVED_14_10	14:10	0x0	Reserved for future use. This register controls no hardware
EQEn (R)	15	0x0	Reserved for future use. This register controls no hardware
MGNINDX	19:16	0x0	Sets the time-margining level
rsv_22_20 (R)	22:20	0x0	Reserved for future use. This register controls no hardware
RESERVED_29_23 (R)	29:23	0x0	Reserved for future use. This register controls no hardware
MGNDIR	30	0x0	This register controls no hardware. Margining is applied equally to both sides of the data eye
MGNEN	31	0x0	Enables time-margining

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b00, the register name is NB_HT3_LINK_RECEIVER_CONF_0 and the fields are as defined in the above table.

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b01, the register name and fields are defined as follows:

NB_HT3_Receiver_Mask:

FieldName	Bits	Default
CTL_CAD	17:0	0x3FFFF
Reserved (Access R)	31:18	0x0

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b10, the register name and fields are defined as follows:

NB_HT3_Transmitter_Mask:

FieldName	Bits	Default
CTL_CAD	17:0	0x3FFFF
Reserved (Access R)	31:18	0x0

NB_HT3_LINK_TRAINING_0 - RW - 32 bits - nbconfig:0xAC			
Field Name	**Bits**	**Default**	**Description**
GANGED (R)	0	0x1	This device only supports ganged operation
AC (R)	1	0x0	This device does not support AC-coupled mode
EIGHT_TO_TEN_BIT_EN (R)	2	0x0	This device does not support 8b/10b coding
SCREN	3	0x0	Scrambler Enable
TOTALATTEMPT	6:4	0x7	Total Attempts - Defines the number of long retry attempts made during failed training sequences
LSSel	8:7	0x0	LS Select 00=LS1 - CLK running. CAD/CTL sending TxIdle 01=Reserved 10=LS2 - CLK/CAD/CTL sending TxIdle 11=LS3 - CLK/CAD/CTL sending either HiZ or TxGndTrm
HotPlugEn (R)	9	0x0	Read-only 0. This device does not support hot-plugging
BISTEn	10	0x0	Built-in Self-Test Enable
ILMEn	11	0x0	Internal Loopback Mode Enable
LaneSel	13:12	0x0	Lane Select - Refer to the HyperTransport 3 specification for details regarding this register
DISCMDTHRT	14	0x0	Disables Command Throttling
RESERVED_15 (R)	15	0x0	Reserved for future use. This register controls no hardware
SerLane	19:16	0x0	Serial Lane Select. Refer to the HyperTransport 3 specification for details regarding this register
CPIEn	20	0x0	Reserved for future use. This register controls no hardware
reserved_31_21	31:21	0x0	Reserved for future use. This register controls no hardware

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b00, the register name is NB_HT3_LINK_TRAINING_0 and the fields are as defined in the above table.

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b01, the register name and fields are defined as follows:

NB_HT3_Receiver_Inversion:

FieldName	Bits	Default
Inversion	17:0	0x0
Reserved (Access R)	31:18	0x0

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b10, the register name and fields are defined as follows:

NB_HT3_Transmitter_Inversion:

FieldName	Bits	Default
Inversion	17:0	0x0
Reserved (Access R)	31:18	0x0

NB_HT3_LINK_FREQUENCY_EXTENSION - RW - 32 bits - nbconfig:0xB0			
Field Name	**Bits**	**Default**	**Description**
FreqExt0	0	0x0	Controls the upper bit of the extended HyperTransport frequency code
FreqCapExt0 (R)	15:1	0x7	Indicates that extended HyperTransport frequency is supported Bit 1 - 2.8Ghz Mode Bit 2 - 3.0Ghz Mode Bit 3 - 3.2Ghz Mode Bits 4->15 Reserved
FreqExt1 (R)	16	0x0	This field is reserved because the device only contains a single HyperTransport link
FreqCapExt1 (R)	31:17	0x0	This field is reserved because the device only contains a single HyperTransport link

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b00, the register name is NB_HT3_LINK_FREQUENCY_EXTENSION and the fields are as indicated in the above table.

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b01, the register name and fields are defined as follows:

NB_HT3_Receiver_Pattern_Buffer_2:

FieldName	Bits	Default
Pattern_2	23:0	0x0
Reserved (Access R)	31:24	0x0

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b10, the register name and fields are defined as follows:

NB_HT3_Transmitter_Pattern_Buffer_2:

FieldName	Bits	Default
Pattern_2	23:0	0x0
Reserved (Access R)	31:24	0x0

NB_HT3_LINK_TRANSMITTER_CONF_1 - RW - 32 bits - nbconfig:0xB4			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	Reserved when REG_IND = 00. This register controls no hardware. This device only contains a single HyperTransport link.

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b00, the register name is NB_HT3_LINK_TRANSMITTER_CONF_1 and the fields are as defined in the above table.

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b01, the register name and fields are defined as follows:

NB_HT3_Receiver_Pattern_Buffer_2_Select:

FieldName	Bits	Default
Pattern_Buffer_2_Enable	17:0	0x0

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b10, the register name and fields are defined as follows:

NB_HT3_Transmitter_Pattern_Buffer_2_Select:

FieldName	Bits	Default
Pattern_Buffer_2_Enable	17:0	0x0

NB_HT3_LINK_RECEIVER_CONF_1 - RW - 32 bits - nbconfig:0xB8			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	Reserved when REG_IND = 00. This register controls no hardware. This device only contains a single HyperTransport link.

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b00, the register name is NB_HT3_LINK_RECEIVER_CONF_1 and the fields are as defined in the above table.

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b01, the register name and fields are defined as follows:

NB_HT3_Receiver_Pattern_Buffer_Extension:

FieldName	Bits	Default
Pattern_Buffer_1	15:0	0x0
Pattern_Buffer_2	31:16	0x0

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b10, the register name and fields are defined as follows:

NB_HT3_Transmitter_Pattern_Buffer_Extension:

FieldName	Bits	Default
Pattern_Buffer_1	15:0	0x0
Pattern_Buffer_2	31:16	0x0

NB_HT3_LINK_TRAINING_1 - RW - 32 bits - nbconfig:0xBC			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	Reserved when REG_IND = 00. This register controls no hardware. This device only contains a single HyperTransport link.

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b00, the register name is NB_HT3_LINK_TRAINING_1 and the fields are as defined in the above table.

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b01, the register name and fields are defined as follows:

NB_HT3_Receiver_Scramble:

FieldName	Bits	Default
Scramble	17:0	0x0
Reserved (Access R)	31:18	0x0

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b10, the register name and fields are defined as follows:

NB_HT3_Transmitter_Scramble:

FieldName	Bits	Default
Scramble	17:0	0x0
Reserved (Access R)	31:18	0x0

NB_HT3_BIST_CONTROL - RW - 32 bits - nbconfig:0xC0			
Field Name	**Bits**	**Default**	**Description**
RSV_0 (R)	0	0x0	Reserved for future use. This register controls no hardware
RxDis	1	0x0	Receiver Disable. The transmitter will advance using the minimal number of training sequences. Receiver BIST checking is disabled.
RESERVED_4_2 (R)	4:2	0x0	Reserved for future use. This register controls no hardware
INVROTEN	5	0x0	Inversion Rotate Enable
ERRSTAT	7:6	0x0	Error Status. 00=No Error 01=Training Error 10=Pattern Miscompare 11=Reserved
ERRLNNUM	12:8	0x0	Error Lane Number. Indicates the lane number where the first error was detectetd
RESERVED_15_13 (R)	15:13	0x0	Reserved for future use. This register controls no hardware
ERRCNT	26:16	0x0	Error Count - Indicates the number of errors detected during BIST operation
RESERVED_30_27 (R)	30:27	0x0	Reserved for future use. This register controls no hardware
width (R)	31	0x0	Read-only 1. This indicates the on-board BIST engine is 16-bits wide

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b00, the register name is NB_HT3_BIST_CONTROL and the fields are as defined in the above table.

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b01, the register name and fields are defined as follows:

NB_HT3_Receiver_Error:

FieldName	Bits	Default
Receiver_error	17:0	0x0
Reserved (Access R)	31:18	0x0

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b10, the register name and fields are defined as follows:

NB_HT3_Reserved:

FieldName	Bits	Default
Reserved (Access R)	31:0	0x0

NB_HT_LINK_COMMAND - RW - 32 bits - nbconfig:0xC4			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	7:0	0x8	Indicates that this is a HyperTransport capability
NEXT_PTR (R)	15:8	0x40	Read only register pointing to the next item in the capability list
BASE_UNIT_ID	20:16	0x0	Specifies the HyperTransport base Unit ID for this device. Relocating the base unit id is not supported
UNIT_ID_COUNT (R)	25:21	0x14	Specifies the number of Unit IDs used by the chip
MASTER_HOST (R)	26	0x0	Set to 0 to indicate the host is accessed through HyperTransport link 0
DEFAULT_DIRECTION (R)	27	0x0	Set to 0 to indicate that requests are sent to the host bridge via link 0
DROP_ON_UNINIT_LINK	28	0x0	This register controls no hardware. This device stalls requests targetted to the HyperTransport interface when the interface is not initialized

SLAVE_PRIMARY_TYPE (R)	31:29	0x0	Indicates that this is a primary HyperTransport interface capability

NB_HT_LINK_CONF_CNTL - RW - 32 bits - nbconfig:0xC8			
Field Name	**Bits**	**Default**	**Description**
RESERVED_0 (R)	0	0x0	Reserved for future use. This register controls no hardware
CRC_FLOOD_ENABLE	1	0x0	CRC flood enable: 0 - Periodic CRC errors do not result in a sync flood 1 - Periodic CRC errors result in a sync flood
RESERVED_2 (R)	2	0x0	Reserved for future use. This register controls no hardware
CRC_ERROR_COMMAND	3	0x0	CRC error command: 0 - transmitter CRC values match the values calculated per the link specification 1 - the link tranmission logic generates erroneous CRC values
LINK_FAILURE	4	0x0	This bit is set by hardware when an error results in a HyperTransport syncflood. The contents of this register are preserved across a warm reset and are cleared by a cold reset.
INIT_COMPLETE	5	0x0	This bit is set when low level link initialization has successfully complete. If device on the other side is unable to properly perform link initilization, then the bit is not set
END_OF_CHAIN (R)	6	0x0	Read-only 0 to indicate that this interface is not the end of the HyperTransport chain
TRANSMITTER_OFF	7	0x0	Transmitter Off: 0 - Normal operation 1 - Transmitter is disabled. Outputs are tristate
CRC_ERROR_DETECTED	9:8	0x0	This register is set by hardware. Each bit may be cleared by writing 1. The contents of this register are preserved across a warm reset and are cleared by a cold reset. Bit 9 indicates a periodic CRC error on the upper byte of the HyperTransport link in HyperTransport 1 mode. This register is not used in HyperTransport 3 mode. Bit 8 indicates a periodic CRC error on the lower byte of the HyperTransport link in HyperTransport 1 mode. In HyperTransport 3 mode, this register is set when an unrecoverable HyperTransport error occurs leading to a syncflood
RESERVED_11_10 (R)	11:10	0x0	Reserved for future use. This register controls no hardware
IsocEn	12	0x0	Enable Isochronous flow-control mode. This register requires a warm-reset to take effect. Please see the appropriate processor BKDG on additional settings required to enable IFCM
LDT3S_ENABLE	13	0x0	HyperTransport link tristate enable. The contents of this register are preserved across a warm reset and are cleared by a cold reset. 0 - during disconnect state, the HyperTransport link transmitter is driven but in an underfined state 1 - during disconnect state, the HyperTransport link transmitter is placed into the high impedance state.
EXTENDED_CNTL_TIME	14	0x0	Specifies the time in which the control is held during HyperTransport 1 initialization. The contents of this register are preserved across a warm reset and are cleared by a cold reset. 0 - at least 16 bit time 1 - about 50 microseconds.

HT_64bEn	15	0x0	HyperTransport 64-bit address extension enable: 1 - HT 64-bit address extension is enabled. The device supports 52-bit phyiscal addressing 0 - HT 64-bit address extension is not enabled. The device supports 40-bit physical addressing
MAX_LINK_WIDTH_IN (R)	18:16	0x1	Specifies the maximum incomming link width of the HyperTransport interface to be 16 bits
RESERVED_19 (R)	19	0x0	Reserved for future use. This register controls no hardware
MAX_LINK_WIDTH_OUT (R)	22:20	0x1	Specifies the maximum outgoing link width of the HyperTransport interface to be 16 bits
RESERVED_23 (R)	23	0x0	Reserved for future use. This register controls no hardware
LINK_WIDTH_IN	26:24	0x0	Specified the operating of the input width 000 - 8 bits 001 - 16 bits 100 - 2 bits - not supported 101 - 4 bits - not supported 111 - not connect. The contents of this register are preserved across a warm reset and are cleared by a cold reset.
RESERVED_27 (R)	27	0x0	Reserved for future use. This register controls no hardware
LINK_WIDTH_OUT	30:28	0x0	Specified the operating of the output width: 000 - 8 bits 001 - 16 bits 100 - 2 bits - not supported 101 - 4 bits - not supported 111 - not connect. The contents of this register are preserved across a warm reset and are cleared by a cold reset.
RESERVED_31 (R)	31	0x0	Reserved for future use. This register controls no hardware

NB_HT_LINK_END - R - 32 bits - nbconfig:0xCC			
Field Name	**Bits**	**Default**	**Description**
Reserved_3_0	3:0	0x0	Reserved for future use. This register controls no hardware
LINK_FAILURE	4	0x1	Hardwired to 1 because there is no secondary HyperTransport link on this device
Reserved_5	5	0x0	Reserved for future use. This register controls no hardware
END_OF_CHAIN	6	0x1	Hardwired to 1 because there is no secondary HyperTransport link on this device
TRANSMITTER_OFF	7	0x1	Hardwired to 1 because there is no secondary HyperTransport link on this device
Reserved_8_31	31:8	0x0	Reserved for future use. This register controls no hardware
HT Link end			

NB_HT_LINK_FREQ_CAP_A - RW - 32 bits - nbconfig:0xD0			
Field Name	**Bits**	**Default**	**Description**
MINOR_REVISION (R)	4:0	0x0	Indicates the minor revision of the HyperTransport specification this device supports
MAJOR_REVISION (R)	7:5	0x3	Indicates the major revision of the HyperTransport specification this device supports

LINK_FREQUENCY_A	11:8	0x0	Specifies the HyperTransport link frequency: 0h=200Mhz 1h=Reserved 2h=400Mhz 3h=Reserved 4h=600Mhz 5h=800Mhz 6h=1000MHz 7h=1200MHz 8h=1400MHz 9h=1600MHz ah=1800MHz bh=2000MHz ch=2200MHz dh=2400MHz eh=2600MHz fh=Reserved. The contents of this register are preserved across a warm reset and are cleared by a cold reset.
Protocol_Error	12	0x0	Set by hardware to indicate the detection of a protocol error. Write 1 to clear. The contents of this register are preserved across a warm reset and are cleared by a cold reset.
Overflow_Error	13	0x0	Set by hardware to indicate the detection of a flow-control buffer overflow condition in the receiver. Write 1 to clear. The contents of this register are preserved across a warm reset and are cleared by a cold reset.
LINK_FREQ_CAP_A (R)	31:16	0x7ff5	This register indicates which HyperTransport frequencies are supported by the part. Each bit indicates that the corresponding encoded HyperTransport frequency is supported (e.g. bit 14 indicates 2600 MHz support).
HT link frequency channel A			

NB_HT_LINK_FREQ_CAP_B - R - 32 bits - nbconfig:0xD4			
Field Name	**Bits**	**Default**	**Description**
LINK_DEVICE_FEATURE_CAP	7:0	0x13	Indicates which optional HyperTransport features are supported by the device. Bit 0 indicates support for isochronous flow-control mode Bit 1 indicates support for LDTSTOP# Bit 4 indicates support for 64-bit addressing
RESERVED	31:8		Reserved for future use. This register controls no hardware.
HT link frequency channel B			

NB_HT_ENUMERATION_SCRATCHPAD - RW - 32 bits - nbconfig:0xD8			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_PAD	15:0	0x0	This register may be used as temporary storage by the system BIOS software. It controls no hardware
Protocol_Error_Flood_Enable	16	0x0	Causes a sync flood to be generated when the HyperTransport protocol error status bit is set.
Overflow_Error_Flood_Enable	17	0x0	Causes a sync flood to be generated when the HyperTransport overflow error status bit is set.
Protocol_Error_Fatal_Enable	18	0x0	Causes a fatal interrupt to be generated when the HyperTransport protocol error status bit is set.
Overflow_Error_Fatal_Enable	19	0x0	Causes a fatal interrupt to be generated when the HyperTransport overflow error status bit is set.
Response_Error_Fatal_Enable	21	0x0	Causes a fatal interrupt to be generated when the HyperTransport response error status bit is set.
CRC_Error_Fatal_Enable	22	0x0	Causes a fatal interrupt to be generated when any of the HyperTransport crc error status bits are set.
RESERVED_24_23 (R)	24:23	0x0	Reserved for future use. This register controls no hardware
Response_Error	25	0x0	Hardware sets this bit to indicate that a HyperTransport response error was detected. Write 1 to clear. The contents of this register are preserved across a warm reset and are cleared by a cold reset.
Protocol_Error_Nonfatal_Enable	26	0x0	Causes a non-fatal interrupt to be generated when the HyperTransport protocol error status bit is set.
Overflow_Error_Nonfatal_Enable	27	0x0	Causes a non-fatal interrupt to be generated when the HyperTransport overflow error status bit is set.
Response_Error_Nonfatal_Enable	29	0x0	Causes a non-fatal interrupt to be generated when the HyperTransport response error status bit is set.
CRC_Error_Nonfatal_Enable	30	0x0	Causes a non-fatal interrupt to be generated when any of the HyperTransport crc error status bits are set.
RESERVED_31 (R)	31	0x0	Reserved for future use. This register controls no hardware
HT scratch pad			

NB_HT_MEMORY_BASE_UPPER - RW - 32 bits - nbconfig:0xDC			
Field Name	**Bits**	**Default**	**Description**
MEMORY_BASE_UPPER_8BIT	7:0	0x0	Extends the nonprefetchable memory base register defined for bridges to 40 bits
MEMORY_LIMIT_UPPER_8BIT	15:8	0x0	Extends the nonprefetchable memory limit register defined for bridges to 40 bits
BUS_NUMBER (R)	23:16	0x0	Contains the values of the bus number captured from the first type 0 configuration cycle received by this device

HT memory upper base

NB_PCIE_INDX_ADDR - RW - 32 bits - nbconfig:0xE0			
Field Name	**Bits**	**Default**	**Description**
NB_PCIE_INDX_ADDR	7:0	0x0	Sets the register address used to access the PCIEIND indirect register space

PCIE_CORE_SEL	18:16	0x0	0=GPP1 and GPP2 (reads target GPP1) 1=GPP3a, GPP3b, SB (reads target SB) Note: for SR5670 GPP3b does not apply 2=All PCIe® cores (reads target SB) 3=GPP3b (not applicable to SR5670) 4=GPP1 5=SB 6=GPP2 7=GPP3a

NB_PCIE_INDX_DATA - RW - 32 bits - nbconfig:0xE4			
Field Name	**Bits**	**Default**	**Description**
NB_PCIE_INDX_DATA	31:0	0x0	Read/Write register data for the PCIEIND register indicated by NB_PCIE_INDX_ADDR:NB_PCIE_INDX_ADDR and NB_PCIE_INDX_ADDR:NB_PCIE_CORE_SEL

MSI_MAPPING_CAPABILITY - RW - 32 bits - nbconfig:0xF0			
Field Name	**Bits**	**Default**	**Description**
CAPABILITY_ID (R)	7:0	0x8	Indicates a Hypertransport™ capability list item
CAPABILITY_POINTER (R)	15:8	0xc4	Points to the next capability list item
EN (R)	16	0x1	Always set to 1 to indicate that the MSI Mapping Capability is always enabled
FIXD (R)	17	0x1	Always set to 1 to indicate that this device only maps MSI interrupts with address 0x0000_0000_FEEx_xxxx onto HyperTransport interrupts and that the mapping range is not programmable.
RSV	26:18	0x0	Reserved for future use. This register controls no hardware
CAPABILITY_TYPE (R)	31:27	0x15	Indicates the MSI Mapping Capability
MSI to HyperTransport interrupt mapping capability			

IOAPIC_INDEX - RW - 32 bits - nbconfig:0xF8			
Field Name	**Bits**	**Default**	**Description**
INDEX	7:0	0x0	Sets the register address used to access the IOAPICMISCIND indirect register space.

IOAPIC_DATA - RW - 32 bits - nbconfig:0xFC			
Field Name	**Bits**	**Default**	**Description**
DATA	31:0	0x0	Read/Write register data for the IOAPICMISCIND register indicated by IOAPIC_INDEX:INDEX

2.2.2 NBCONFIGFUNC2 Registers

IOMMU_VENDOR_ID - R - 16 bits - nbconfigfunc2:0x0			
Field Name	**Bits**	**Default**	**Description**
VENDOR_ID	15:0	0x1002	Vendor Identifier. This 16-bit field identifies the manufacturer of the device: Advanced Micro Devices Inc.

IOMMU_DEVICE_ID - R - 16 bits - nbconfigfunc2:0x2			
Field Name	**Bits**	**Default**	**Description**
DEVICE_ID	15:0	0x5A23	Device Identifier. This 16-bit field is assigned by the device manufacturer and identifies the type of device.

IOMMU_COMMAND - RW - 16 bits - nbconfigfunc2:0x4			
Field Name	**Bits**	**Default**	**Description**
IO_ACCESS_EN (R)	0	0x0	I/O Access Enable This register controls no hardware. This function does not declare any standard I/O BARs. 0=Disable 1=Enable
MEM_ACCESS_EN (R)	1	0x0	Memory Access Enable This register controls no hardware. This function does not declare any standard memory BARs. 0=Disable 1=Enable
BUS_MASTER_EN	2	0x0	Bus Master Enable 1=This function is allowed to generate DMA requests 0=This function is not allowed to generate DMA requests 0=Disable 1=Enable
Reserved1 (R)	5:3	0x0	Reserved for future use. This register controls no hardware 0=Disable 1=Enable
PARITY_ERROR_EN	6	0x0	Parity Error Enable 1=This function is allowed to set the PARITY_ERROR_DETECTED status bit 0=This function is not allowed to set the PARITY_ERROR_DETECTED status bit 0=Disable 1=Enable
Reserved0 (R)	7	0x0	Reserved for future use. This register controls no hardware 0=Disable 1=Enable
SERR_EN (R)	8	0x0	System Error Enable This function does not set the signaled system error status bit 0=Disable 1=Enable
Reserved2 (R)	9	0x0	Reserved for future use. This register controls no hardware 0=Disable 1=Enable

INTERRUPT_DIS	10	0x0	Interrupt Disable 1=This function is not allowed to generate legacy INTx interrupts 0=This function is allowed to generate legacy INTx interrupts 0=Disable 1=Enable
Reserved (R)	15:11	0x0	Reserved for future use. This register controls no hardware

IOMMU_STATUS - RW - 16 bits - nbconfigfunc2:0x6			
Field Name	**Bits**	**Default**	**Description**
Reserved (R)	2:0	0x0	Reserved for future use. This register controls no hardware
INT_Status (R)	3	0x0	Interrupt Status 1=This function has an outstanding interrupt 0=This function does not have any outstanding interrupts 0=Disable 1=Enable
CAP_LIST (R)	4	0x1	Capabilities List This bit is set to indicate that this function`s configuration space supports a capabilities list. 0=Disable 1=Enable
Reserved1 (R)	7:5	0x0	Reserved for future use. This register controls no hardware
MASTER_DATA_ERROR	8	0x0	Master Data Error RW1C. This bit is set by hardware whenever PARITY_ERROR_EN is set and this function receives a read response with the data error attribute set 0=Disable 1=Enable
Reserved2 (R)	10:9	0x0	Reserved for future use. This register controls no hardware
SIGNAL_TARGET_ABORT (R)	11	0x0	Signal Target Abort This bit is always set to 0 because this function does not terminate host requests with target abort 0=No Abort 1=Target Abort asserted
RECEIVED_TARGET_ABORT	12	0x0	Received Target Abort RW1C. This bit is set by hardware whenever this function receives a read response with the target abort status 0=Inactive 1=Active
RECEIVED_MASTER_ABORT	13	0x0	Received Target Abort RW1C. This bit is set by hardware whenever this function receives a read response with the master abort status 0=Inactive 1=Active
SIGNALED_SYSTEM_ERROR (R)	14	0x0	Signaled System Error This bit is always set to 0 because this function does not generate signaled system error status
PARITY_ERROR_DETECTED	15	0x0	Parity Error Detected RW1C. This bit is set by hardware whenever this function receives a read response with the data error attribute set

IOMMU_REVISION_ID - R - 8 bits - nbconfigfunc2:0x8			
Field Name	**Bits**	**Default**	**Description**
MINOR_REV_ID	3:0	0x0	Identifies the stepping number of the function
MAJOR_REV_ID	7:4	0x0	Identifies the revision number of the function

IOMMU_REGPROG_INF - R - 8 bits - nbconfigfunc2:0x9			
Field Name	**Bits**	**Default**	**Description**
REG_LEVEL_PROG_INF	7:0	0x0	Register Programming Interface IOMMU

IOMMU_SUB_CLASS - R - 8 bits - nbconfigfunc2:0xA			
Field Name	**Bits**	**Default**	**Description**
SUB_CLASS_INF	7:0	0x6	Sub-Class Code IOMMU

IOMMU_BASE_CODE - R - 8 bits - nbconfigfunc2:0xB			
Field Name	**Bits**	**Default**	**Description**
BASE_CLASS_CODE	7:0	0x8	Sub-Class Code System Base Peripheral

IOMMU_CACHE_LINE - R - 8 bits - nbconfigfunc2:0xC			
Field Name	**Bits**	**Default**	**Description**
CACHE_LINE_SIZE	7:0	0x0	Reserved for future use. This register controls no hardware

IOMMU_LATENCY - R - 8 bits - nbconfigfunc2:0xD			
Field Name	**Bits**	**Default**	**Description**
LATENCY	7:0	0x0	Reserved for future use. This register controls no hardware

IOMMU_HEADER - R - 8 bits - nbconfigfunc2:0xE			
Field Name	**Bits**	**Default**	**Description**
HEADER_TYPE	7:0	0x80	Header Type Indicates a multi-function device with a type 0 configuration space header

IOMMU_BIST - R - 8 bits - nbconfigfunc2:0xF			
Field Name	**Bits**	**Default**	**Description**
BIST_COMP	3:0	0x0	Reserved for future use. This register controls no hardware
BIST_STRT	6	0x0	Reserved for future use. This register controls no hardware
BIST_CAP	7	0x0	Reserved for future use. This register controls no hardware

IOMMU_ADAPTER_ID - RW - 32 bits - nbconfigfunc2:0x2C			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID (R)	15:0	0x0	Subsystem vendor ID
SUBSYSTEM_ID (R)	31:16	0x0	Subsystem ID

IOMMU_CAPABILITIES_PTR - RW - 32 bits - nbconfigfunc2:0x34			
Field Name	**Bits**	**Default**	**Description**
CAP_PTR (R)	7:0	0x40	Capabilities Pointer Points to the start of the capabilities list

IOMMU_INTERRUPT_LINE - RW - 8 bits - nbconfigfunc2:0x3C			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_LINE	7:0	0x0	This register is read/write for software compatibility. It controls no hardware

IOMMU_INTERRUPT_PIN - RW - 8 bits - nbconfigfunc2:0x3D			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_PIN (R)	7:0	0x0	This field indicates the INTx line used to generate legacy interrupts. 0=Legacy interrupts disabled 1=INTA 2=INTB 3=INTC 4=INTD All other encodings are not supported.

IOMMU_CAP_HEADER - RW - 32 bits - nbconfigfunc2:0x40			
Field Name	**Bits**	**Default**	**Description**
IOMMU_CAP_ID (R)	7:0	0xf	Indicates a Secure Device capability block.
IOMMU_CAP_PTR (R)	15:8	0x54	Indicates the location of the next capability block if one is present.
IOMMU_CAP_TYPE (R)	18:16	0x3	Specifies the layout of the Capability Block as an IOMMU capability block.
IOMMU_CAP_REV (R)	23:19	0x1	Specifies the IOMMU specification revision.
IOMMU_IO_TLBSUP (R)	24	0x0	Indicates support for remote IOTLBs.

IOMMU_HT_TUNNEL_SUP (R)	25	0x0	HyperTransport tunnel translation support. This register is always set to 0 to indicate that the device does not contain a HyperTransport tunnel supporting address translation.
IOMMU_NP_CACHE (R)	26	0x0	1=Indicates that the IOMMU caches page table entries that are marked as not present. When this bit is set, software must issue an invalidate after any change to a PDE or PTE. 0=Indicates that the IOMMU caches only page table entries that are marked as present. When NpCache is clear, software must issue an invalidate after any change to a PDE or PTE marked present before the change. Note: For hardware implementations of the IOMMU, this bit must be 0b.
Reserved (R)	31:27	0x0	Reserved for future use. This register controls no hardware

IOMMU_CAP_BASE_LO - RW - 32 bits - nbconfigfunc2:0x44			
Field Name	**Bits**	**Default**	**Description**
IOMMU_ENABLE	0	0x0	1=IOMMU accepts memory accesses to the address specified in the Base Address Register. When Enable is written with a 1, all IOMMU RW capability registers in PCI configuration space are locked until the next system reset.
Reserved (R)	13:1	0x0	Reserved for future use. This register controls no hardware
IOMMU_BASE_ADDR_LO	31:14	0x0	Specifies address bits [31:14] of the 16K-byte-aligned base address of the IOMMU memory-mapped control registers.

IOMMU_CAP_BASE_HI - RW - 32 bits - nbconfigfunc2:0x48			
Field Name	**Bits**	**Default**	**Description**
IOMMU_BASE_ADDR_HI	31:0	0x0	Specifies address bits [63:32] of the 16K-byte-aligned base address of the IOMMU memory-mapped control registers.

IOMMU_CAP_RANGE - RW - 32 bits - nbconfigfunc2:0x4C			
Field Name	**Bits**	**Default**	**Description**
Reserved (R)	31:0	0x0	Reserved for future use. This register controls no hardware

IOMMU_CAP_MISC - RW - 32 bits - nbconfigfunc2:0x50			
Field Name	**Bits**	**Default**	**Description**
IOMMU_MSI_NUM (R)	4:0	0x0	Indicates the MSI vector used for interrupt messages generated by the IOMMU
Reserved (R)	7:5	0x0	Reserved for future use. This register controls no hardware
IOMMU_PA_SIZE (R)	14:8	0x30	This field must indicate the size of the maximum physical address generated by the IOMMU. The value is the (unsigned) binary log of the maximum address size. Allowed values are 40, 48 and 52; all other values are reserved. 010_1000b=40 bits 011_0000b=48 bits 011_0100b=52 bits

IOMMU_VA_SIZE (R)	21:15	0x40	This field must indicate the size of the maximum virtual address processed by the IOMMU. The value is the (unsigned) binary log of the maximum address size. Allowed values are 32, 40, 48, and 64; all other values are reserved. 010_0000b=32 bits 010_1000b=40 bits 011_0000b=48 bits 100_0000b=64 bits (default)
IOMMU_HT_ATS_RESV	22	0x0	1=The HyperTransport? Address Translation address range for ATS responses is reserved and cannot be translated by the IOMMU. 0=The Address Translation address range can be translated by the IOMMU.

IOMMU_MSI_CAP - RW - 32 bits - nbconfigfunc2:0x54			
Field Name	**Bits**	**Default**	**Description**
MSI_CAP_ID (R)	7:0	0x5	Indicates that this is the MSI capability
MSI_CAP_PTR (R)	15:8	0x64	Pointer to the next configuration space capability
MSI_EN	16	0x0	Enables MSI for this function and causes legacy interrupts to be disabled
MSI_MULT_MESS_CAP (R)	19:17	0x0	Indicates the number of MSI messages requested by this function
MSI_MULT_MESS_EN (R)	22:20	0x0	Sets the number of MSI messages assigned to this function
MSI_64_EN (R)	23	0x1	Indicates that a 64-bit MSI address is supported
Reserved (R)	31:24	0x0	Reserved for future use. This register controls no hardware

IOMMU_MSI_ADDR_LO - RW - 32 bits - nbconfigfunc2:0x58			
Field Name	**Bits**	**Default**	**Description**
Reserved (R)	1:0	0x0	Reserved for future use. This register controls no hardware
MSI_ADDR_LO	31:2	0x0	This register sets address bits [31:2] used to issue MSI messages.

IOMMU_MSI_ADDR_HI - RW - 32 bits - nbconfigfunc2:0x5C			
Field Name	**Bits**	**Default**	**Description**
MSI_ADDR_HI	31:0	0x0	This register sets address bits [63:32] used to issue MSI messages.

IOMMU_MSI_DATA - RW - 32 bits - nbconfigfunc2:0x60			
Field Name	**Bits**	**Default**	**Description**
MSI_DATA	15:0	0x0	This register sets the data issued with MSI messages.
Reserved (R)	31:16	0x0	Reserved for future use. This register controls no hardware

IOMMU_MSI_MAPPING_CAP - RW - 32 bits - nbconfigfunc2:0x64			
Field Name	**Bits**	**Default**	**Description**
MSI_MAP_CAP_ID (R)	7:0	0x8	Indicates a HyperTransport capability list item
MSI_MAP_CAP_PTR (R)	15:8	0x0	Points to the next capability list item
MSI_MAP_EN (R)	16	0x1	Always set to 1 to indicate that the MSI Mapping Capability is always enabled
MSI_MAP_FIXD (R)	17	0x1	Always set to 1 to indicate that this device only maps MSI interrupts with address 0xFEEx_xxxx onto HyperTransport interrupts and that the mapping range is not programmable
MSI_MAP_RSV (R)	26:18	0x0	Reserved for future use. This register controls no hardware
MSI_MAP_CAP_TYPE (R)	31:27	0x15	Indicates the MSI Mapping Capability

IOMMU_ADAPTER_ID_W - RW - 32 bits - nbconfigfunc2:0x68			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID_W	15:0	0x0	Sets the subsystem vendor ID register in the configuration header
SUBSYSTEM_ID_W	31:16	0x0	Sets the subsystem ID register in the configuration header

IOMMU_CONTROL_W - RW - 32 bits - nbconfigfunc2:0x6C			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_PIN_W	2:0	0x1	Sets the INTERRUPT_PIN register in the configuration header 0 = No legacy interrupts supported 1 = INTA 2 = INTB 3 = INTC 4 = INTD
MINOR_REV_ID_W	7:4	0x0	Sets the minor revision ID register in the configuration header
IO_TLBSUP_W	8	0x1	Sets the value of IO_TLBSUP in the IOMMU capability

L2CFG_INDEX - RW - 32 bits - nbconfigfunc2:0xF0			
Field Name	**Bits**	**Default**	**Description**
L2CFG_INDEX	7:0	0x0	
L2CFG_WR_EN	8	0x0	0=Disable writes to L2CFG_DATA 1=Enable writing to L2CFG_DATA

L2CFG_DATA - RW - 32 bits - nbconfigfunc2:0xF4			
Field Name	**Bits**	**Default**	**Description**
L2CFG_DATA	31:0	0x0	

L1CFG_INDEX - RW - 32 bits - nbconfigfunc2:0xF8			
Field Name	**Bits**	**Default**	**Description**
L1CFG_INDEX	15:0	0x0	
L1CFG_SEL	19:16	0x0	Selects the IOMMU L1 block that will be targeted by accesses to L1CFG_DATA 0 = GPP1 1 = GPP2 2 = SB 3 = GPP3a 4 = GPP3b (not used in SR5670) 5 = SBVC1
L1CFG_EN	31	0x0	0=Disable writes to L1CFG_DATA 1=Enable writing to L1CFG_DATA

L1CFG_DATA - RW - 32 bits - nbconfigfunc2:0xFC			
Field Name	**Bits**	**Default**	**Description**
L1CFG_DATA	31:0	0x0	

2.2.3 PCIECONFIGDEV Registers

PCIE_VENDOR_ID - RW - 16 bits - [pcieConfigDev[13:2]:0x0]			
Field Name	**Bits**	**Default**	**Description**
VENDOR_ID (R)	15:0	0x1002	Vendor Identifier. This 16-bit field identifies the manufacturer of the device: Advanced Micro Devices Inc.
Vendor Identification			

PCIE_DEVICE_ID - R - 16 bits - [pcieConfigDev[13:2]:0x2]			
Field Name	**Bits**	**Default**	**Description**
DEVICE_ID	15:0	0x0	Identifies the particular device. This identifier is allocated by the vendor. Refer to the Device ID table in Section 2.1.4 for details about the read-back value.
Device Identification			

PCIE_COMMAND - RW - 16 bits - [pcieConfigDev[13:2]:0x4]			
Field Name	**Bits**	**Default**	**Description**
IO_ACCESS_EN	0	0x0	Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses.State after RST# is 0. 0=Disable 1=Enable
MEM_ACCESS_EN	1	0x0	Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses. State after RST# is 0. 0=Disable 1=Enable
BUS_MASTER_EN	2	0x0	Controls the ability of a PCI Express Endpoint to issue Memory and I/O Read/Write Requests, and the ability of a Root or Switch Port to forward Memory and I/O Read/Write Requests in the upstream direction. 0=Disable 1=Enable
SPECIAL_CYCLE_EN (R)	3	0x0	Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
MEM_WRITE_INVALIDATE_EN (R)	4	0x0	Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
PAL_SNOOP_EN (R)	5	0x0	Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
PARITY_ERROR_RESPONSE	6	0x0	Parity Error Response. Default value of this field is 0. 0=Disable 1=Enable
AD_STEPPING (R)	7	0x0	Address and Data Stepping. Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable

SERR_EN	8	0x0	Enables the reporting of Non-fatal and Fatal errors detected by the device to the Root Complex. 0=Disable 1=Enable
FAST_B2B_EN (R)	9	0x0	Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
INT_DIS	10	0x0	Controls the ability of a PCI Express device to generate INTx interrupt Messages. When set, devices are prevented from generating INTx interrupt Messages. Default value 0 0=Enable 1=Disable
The Command register provides coarse control over a device's ability to generate and respond to PCI cycles.			

PCIE_STATUS - RW - 16 bits - [pcieConfigDev[13:2]:0x6]			
Field Name	**Bits**	**Default**	**Description**
INT_STATUS (R)	3	0x0	Indicates that an INTx interrupt Message is pending internally to the device.
CAP_LIST (R)	4	0x1	Indicates the presence of an extended capability list item. Since all PCI Express devices are required to implement the PCI Express capability structure, this bit must be set to 1.
PCI_66_EN (R)	5	0x0	Does not apply to PCI Express. Hardwired to 0.
UDF_EN (R)	6	0x0	User Defined Status Enable 0=Disable 1=Enable
FAST_BACK_CAPABLE (R)	7	0x0	Does not apply to PCI Express. Hardwired to 0.
MASTER_DATA_PARITY_ERROR (R)	8	0x0	This bit is set by Requestor if its Parity Error Enable bit is set and either of the following two conditions occurs: (1) Requestor receives a Completion marked poisoned (2) Requestor poisons a write Request 0=Inactive 1=Active
DEVSEL_TIMING (R)	10:9	0x0	Does not apply to PCI Express. Hardwired to 0.
SIGNAL_TARGET_ABORT (R)	11	0x0	This bit is set when a device completes a Request using Completer Abort Completion Status. 0=No Abort 1=Target Abort
RECEIVED_TARGET_ABORT (R)	12	0x0	This bit is set when a Requestor receives a Completion with Unsupported Request Completion Status. 0=Inactive 1=Active
RECEIVED_MASTER_ABORT (R)	13	0x0	This bit is set when a Requestor receives a Completion with Unsupported Request Completion Status. 0=Inactive 1=Active
SIGNALED_SYSTEM_ERROR	14	0x0	This bit must be set whenever the device asserts SERR#. 0=No Error 1=SERR assert
PARITY_ERROR_DETECTED (R)	15	0x0	This bit is set when a device sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1.
The Status register is used to record status information for PCI bus related events.			

PCIE_REVISION_ID - R - 8 bits - [pcieConfigDev[13:2]:0x8]			
Field Name	**Bits**	**Default**	**Description**
MINOR_REV_ID	3:0	0x0	Major revision ID. Set by the vendor.
MAJOR_REV_ID	7:4	0x0	Minor revision ID. Set by the vendor.

Specifies a device specific revision identifier. The value is chosen by the vendor.

PCIE_PROG_INTERFACE - R - 8 bits - [pcieConfigDev[13:2]:0x9]			
Field Name	**Bits**	**Default**	**Description**
PROG_INTERFACE	7:0	0x0	Unused (used only in test environments)
Register-Level Programming Interface Register			

PCIE_SUB_CLASS - R - 8 bits - [pcieConfigDev[13:2]:0xA]			
Field Name	**Bits**	**Default**	**Description**
SUB_CLASS	7:0	0x4	The Class Code register is read-only and is used with the Base Class Code to identify the specific type of device.
Sub Class Code Register			

PCIE_BASE_CLASS - R - 8 bits - [pcieConfigDev[13:2]:0xB]			
Field Name	**Bits**	**Default**	**Description**
BASE_CLASS	7:0	0x6	The Class Code register is read-only and is used to identify the generic function of the device.
Base Class Code Register			

PCIE_CACHE_LINE - RW - 8 bits - [pcieConfigDev[13:2]:0xC]			
Field Name	**Bits**	**Default**	**Description**
CACHE_LINE_SIZE	7:0	0x0	This read/write register specifies the system cacheline size in units of DWORDs.
Cache Line Size Register			

PCIE_LATENCY - RW - 8 bits - [pcieConfigDev[13:2]:0xD]			
Field Name	**Bits**	**Default**	**Description**
LATENCY_TIMER (R)	7:0	0x0	Primary/Master latency timer does not apply to PCI Express. Register is hardwired to 0.
Master Latency Timer Register			

PCIE_HEADER - RW - 8 bits - [pcieConfigDev[13:2]:0xE]			
Field Name	**Bits**	**Default**	**Description**
HEADER_TYPE (R)	6:0	0x1	Type 0 or Type 1 Configuration Space
DEVICE_TYPE (R)	7	0x0	Single function or multi function device 0=Single-Function Device 1=Multi-Function Device
Configuration Space Header			

PCIE_BIST - RW - 8 bits - [pcieConfigDev[13:2]:0xF]			
Field Name	**Bits**	**Default**	**Description**
BIST_COMP (R)	3:0	0x0	A value of 0 means the device has passed its test. Non-zero values mean the device failed. Device-specific failure codes can be encoded in the non-zero value.

BIST_STRT (R)	6	0x0	Write a 1 to invoke BIST. Device resets the bit when BIST is complete. Software should fail the device if BIST is not complete after 2 seconds.
BIST_CAP (R)	7	0x0	This bit is read-only and returns 1 the bridge supports BIST, otherwise 0 is returned
Built In Self Test Register used for control and status of built-in self tests			

PCIE_SUB_BUS_NUMBER_LATENCY - RW - 32 bits - [pcieConfigDev[13:2]:0x18]			
Field Name	**Bits**	**Default**	**Description**
PRIMARY_BUS	7:0	0x0	Primary Bus Number register recordsd the bus number of the PCI bus segment to which the primary interface of the bridge is connected.
SECONDARY_BUS	15:8	0x0	Secondary Bus Number register is used to record the bus number of the PCIe® bus segment to which the secondary interface of the brdige is connected.
SUB_BUS_NUM	23:16	0x0	Subordinate Bus Number Register is used to record the bus number of the highest numbered PCI bus segment which is behind the bridge.
SECONDARY_LATENCY_TIMER (R)	31:24	0x0	Register does not apply to PCI Express. Hardwired to 0.
Subordinate Bus Number Latency			

PCIE_IO_BASE_LIMIT - RW - 16 bits - [pcieConfigDev[13:2]:0x1C]			
Field Name	**Bits**	**Default**	**Description**
IO_BASE_TYPE (R)	3:0	0x1	I/O Base Addressing Type 0=16-bit 1=32-bit
IO_BASE	7:4	0x0	I/O Base Register
IO_LIMIT_TYPE (R)	11:8	0x1	I/O Limit Addressing Type 0=16-bit 1=32-bit
IO_LIMIT	15:12	0x0	I/O Limit Register
I/O Base Register Limit is used by the bridge to determine when to forward I/O transactions from one interface to the other.			

PCIE_SECONDARY_STATUS - RW - 16 bits - [pcieConfigDev[13:2]:0x1E]			
Field Name	**Bits**	**Default**	**Description**
CAP_LIST (R)	4	0x0	Indicates the presence of an extended capability list item. Since all PCI Express devices are required to implement the PCI Express capability structure, this bit must be set to 1.
PCI_66_EN (R)	5	0x0	Does not apply to PCI Express. Hardwired to 0.
UDF_EN (R)	6	0x0	User Defined Status Enable 0=Disable 1=Enable
FAST_BACK_CAPABLE (R)	7	0x0	Does not apply to PCI Express. Hardwired to 0.
MASTER_DATA_PARITY_ERROR	8	0x0	This bit is set by Requestor if its Parity Error Enable bit is set and either of the following two conditions occurs: (1) Requestor receives a Completion marked poisoned (2) Requestor poisons a write Request 0=No error 1=Parity error
DEVSEL_TIMING (R)	10:9	0x0	Does not apply to PCI Express. Hardwired to 0.
SIGNAL_TARGET_ABORT (R)	11	0x0	This bit is set when a device completes a Request using Completer Abort Completion Status. 0=No Abort 1=Target Abort asserted

RECEIVED_TARGET_ABORT	12	0x0	This bit is set when a Requestor receives a Completion with Unsupported Request Completion Status. 0=No CA Received 1=Received Completion Abort
RECEIVED_MASTER_ABORT	13	0x0	This bit is set when a Requestor receives a Completion with Unsupported Request Completion Status. 0=No UR Received 1=Received Unsupported Request
RECEIVED_SYSTEM_ERROR	14	0x0	This bit reports the detection of an system error on the secondary inteface of the bridge. 1 is assered if a system error has been detected. 0=No Error 1=Sent Error Meesage
PARITY_ERROR_DETECTED	15	0x0	This bit is set when a device sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1. 0=No Error 1=Received Poisoned TLP
Secondary Status Register. Its bits reflect status conditions of the secondary interface			

PCIE_MEM_BASE_LIMIT - RW - 32 bits - [pcieConfigDev[13:2]:0x20]			
Field Name	**Bits**	**Default**	**Description**
MEM_BASE_TYPE (R)	3:0	0x0	Memory Base Addressing Type 0=32-bit 1=64-bit
MEM_BASE_31_20	15:4	0x0	Memory Base Register
MEM_LIMIT_TYPE (R)	19:16	0x0	Memory Limit Addressing Type 0=32-bit 1=64-bit
MEM_LIMIT_31_20	31:20	0x0	Memory Limit Register
Memory Limit Register defines a memory mapped I/O address range which is used by the bridge to determine when to forward memory transactions from one interface to the other			

PCIE_PREF_BASE_LIMIT - RW - 32 bits - [pcieConfigDev[13:2]:0x24]			
Field Name	**Bits**	**Default**	**Description**
PREF_MEM_BASE_TYPE (R)	3:0	0x1	Prefetchable Memory Base Addressing Type 0=32-bit 1=64-bit
PREF_MEM_BASE_31_20	15:4	0x0	Prefetchable memory Base Register
PREF_MEM_LIMIT_TYPE (R)	19:16	0x1	Prefetchable Memory Limit Addressing Type 0=32-bit 1=64-bit
PREF_MEM_LIMIT_31_20	31:20	0x0	Prefetchable Memory Limit Register
Prefetchable Memory Base Limit indicates 64-bit addresses are supported.			

PCIE_PREF_BASE_UPPER - RW - 32 bits - [pcieConfigDev[13:2]:0x28]			
Field Name	**Bits**	**Default**	**Description**
PREF_BASE_UPPER	31:0	0x0	Upper 32 bits for 64-bit address.

PCIE_PREF_LIMIT_UPPER - RW - 32 bits - [pcieConfigDev[13:2]:0x2C]

Field Name	Bits	Default	Description
PREF_LIMIT_UPPER	31:0	0x0	Upper 32 bits for 64-bit address.

PCIE_IO_BASE_LIMIT_HI - RW - 32 bits - [pcieConfigDev[13:2]:0x30]			
Field Name	**Bits**	**Default**	**Description**
IO_BASE_31_16	15:0	0x0	Upper 16 bits for 32-bit address.
IO_LIMIT_31_16	31:16	0x0	Upper 16 bits for 32-bit address.

PCIE_IRQ_BRIDGE_CNTL - RW - 16 bits - [pcieConfigDev[13:2]:0x3E]			
Field Name	**Bits**	**Default**	**Description**
PARITY_RESPONSE_EN	0	0x0	Parity Error Response Enable controls the response to Poisoned TLPs.
SERR_EN	1	0x0	System Error Enable controls the forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary
ISA_EN	2	0x0	ISA Enable modifies the response by the bridge to ISA I/O addresses.
VGA_EN	3	0x0	VGA Enable modifies the response by the bridge to VGA compatible addresses.
VGA_DEC	4	0x0	Enables the bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 kB.
MASTER_ABORT_MODE (R)	5	0x0	Master Abort Mode does not apply to PCI Express. Hardwired to 0.
SECONDARY_BUS_RESET	6	0x0	Secondary Bus Reset triggers a hot reset on the corresponding PCI Express Port. 0=Run 1=Reset
FAST_B2B_EN (R)	7	0x0	Fast Back-to-Back Transactions Enable does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
Bridge Control Register			

PCIE_CAP_PTR - RW - 32 bits - [pcieConfigDev[13:2]:0x34]			
Field Name	**Bits**	**Default**	**Description**
CAP_PTR (R)	7:0	0x50	Pointer to a linked list of additional capabilities implemented by this device. 50=Point to PM Capability
Capability Pointer			

PCIE_INTERRUPT_LINE - RW - 8 bits - [pcieConfigDev[13:2]:0x3C]			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_LINE	7:0	0xff	Interrupt Line register communicates interrupt line routing information.
Interrupt Line Register			

PCIE_INTERRUPT_PIN - RW - 8 bits - [pcieConfigDev[13:2]:0x3D]			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_PIN	7:0	0x0	The Interrupt Pin is a read-only register that identifies the legacy interrupt Message(s) the device (or device function) uses. Note: Bits [7:3] of this field are hardwired to 0.
Interrupt Pin Register			

PCIE_EXT_BRIDGE_CNTL - RW - 8 bits - [pcieConfigDev[13:2]:0x40]			
Field Name	**Bits**	**Default**	**Description**
IO_PORT_80_EN	0	0x0	Register to enable IO port 80 decoding.
External Bridge Control Register			

PCIE_PMI_CAP_LIST - R - 16 bits - [pcieConfigDev[13:2]:0x50]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	7:0	0x1	Capability ID Must be set to 01h 1=PCIe® Power Management Registers
NEXT_PTR (R)	15:8	0x58	Next Capability Pointer
Power Management Capbility List			

PCIE_PMI_CAP - RW - 16 bits - [pcieConfigDev[13:2]:0x52]			
Field Name	**Bits**	**Default**	**Description**
VERSION (R)	2:0	0x3	Version 3=PMI Spec 1.2
PME_CLOCK (R)	3	0x0	Does not apply to PCI Express. Hardwired to 0.
DEV_SPECIFIC_INIT (R)	5	0x0	Device Specific Initialization
AUX_CURRENT	8:6	0x0	AUX Current
D1_SUPPORT (R)	9	0x0	D1 Support 1=Support D1 PM State.
D2_SUPPORT (R)	10	0x0	D2 Support 1=Support D2 PM State.
PME_SUPPORT (R)	15:11	0x0	For a device, this indicates the power states in which the device may generate a PME.
Power Management Capabilities Register			

PCIE_PMI_STATUS_CNTL - RW - 32 bits - [pcieConfigDev[13:2]:0x54]			
Field Name	**Bits**	**Default**	**Description**
POWER_STATE	1:0	0x0	Power State
NO_SOFT_RESET (R)	3	0x0	No Soft Reset
PME_EN	8	0x0	PME Enable
DATA_SELECT (R)	12:9	0x0	Data Select
DATA_SCALE (R)	14:13	0x0	Data Scale
PME_STATUS	15	0x0	PME Status
B2_B3_SUPPORT (R)	22	0x0	B2/B3 Support Does not apply to PCI Express. Hardwired to 0.
BUS_PWR_EN (R)	23	0x0	Bus Power/Clock Control Enable Does not apply to PCI Express. Hardwired to 0.
PMI_DATA (R)	31:24	0x0	Data
Power Management Status/Control Register			

PCIE_CAP_LIST - R - 16 bits - [pcieConfigDev[13:2]:0x58]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	7:0	0x10	Indicates the PCI Express Capability structure. This field must return a Capability ID of 10h indicating that this is a PCI Express Capability structure. 10=PCI Express capable
NEXT_PTR (R)	15:8	0xa0	Next Capability Pointer. The offset to the next PCI capability structure or 00h if no other items exist in the linked list of capabilities.
The PCI Express Capability List register enumerates the PCI Express Capability structure in the PCI 2.3 configuration space capability list.			

PCIE_CAP - RW - 16 bits - [pcieConfigDev[13:2]:0x5A]			
Field Name	**Bits**	**Default**	**Description**
VERSION (R)	3:0	0x2	Indicates PCI-SIG defined PCI Express capability structure version number. 0=PCI Express Cap Version
DEVICE_TYPE (R)	7:4	0x4	Indicates the type of PCI Express logical device. 0=PCI Express Endpoint 1=Legacy PCI Express Endpoint 4=PCI Express Root Complex
SLOT_IMPLEMENTED	8	0x0	Indicates that the PCI Express Link associated with this Port is connected to a slot
INT_MESSAGE_NUM (R)	13:9	0x0	Interrupt Message Number.
The PCI Express Capabilities register identifies PCI Express device type and associated capabilities.			

PCIE_DEVICE_CAP - RW - 32 bits - [pcieConfigDev[13:2]:0x5C]			
Field Name	**Bits**	**Default**	**Description**
MAX_PAYLOAD_SUPPORT (R)	2:0	0x0	Indicates the maximum payload size that the device can support for TLPs. 0=128B size
PHANTOM_FUNC (R)	4:3	0x0	Indicates the support for use of unclaimed function numbers to extend the number of outstanding transactions allowed by logically combining unclaimed function numbers with the Tag identifier. 0=No Phantom Functions
EXTENDED_TAG (R)	5	0x1	Indicates the maximum supported size of the Tag field as a Requester. 0=5 Bit Tag Supported 1=8 Bit Tag Supported
L0S_ACCEPTABLE_LATENCY (R)	8:6	0x0	Indicates the acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state.
L1_ACCEPTABLE_LATENCY (R)	11:9	0x0	This field indicates the acceptable latency that an Endpoint can withstand due to the transition from L1 state to the L0 state.
ROLE_BASED_ERR_REPORTING (R)	15	0x0	This field indicates the function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification 1.0a. 0=Role-Based Error Reporting Disabled 1=Role-Based Error Reporting Enabled
CAPTURED_SLOT_POWER_LIMIT (R)	25:18	0x0	(Upstream Ports only) In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot.
CAPTURED_SLOT_POWER_SCALE (R)	27:26	0x0	Specifies the scale used for the Slot Power Limit Value.

FLR_CAPABLE (R)	28	0x0	Indicates that a device is capable of initiating Function Level Resets.
The Device Capabilities register identifies PCI Express device specific capabilities.			

PCIE_DEVICE_CNTL - RW - 16 bits - [pcieConfigDev[13:2]:0x60]			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR_EN	0	0x0	Controls reporting of correctable errors. Default value of this field is 0. 0=Disable 1=Enable
NON_FATAL_ERR_EN	1	0x0	Controls reporting of Non-fatal errors. Default value of this field is 0. 0=Disable 1=Enable
FATAL_ERR_EN	2	0x0	Controls reporting of Fatal errors. Default value of this field is 0. 0=Disable 1=Enable
USR_REPORT_EN	3	0x0	Enables reporting of Unsupported Requests when set. Default value of this field is 0. 0=Disable 1=Enable
RELAXED_ORD_EN	4	0x1	If this bit is set, the device is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering. Default value of this bit is 1. 0=Disable 1=Enable
MAX_PAYLOAD_SIZE (R)	7:5	0x0	Sets the maximum TLP payload size for the device. Default value of this field is 000b. 0=128B size
EXTENDED_TAG_EN	8	0x0	When set, this bit enables a device to use an 8-bit Tag field as a requester. If the bit is cleared, the device is restricted to a 5-bit Tag field. Default value of this field is 0. 0=Disable 1=Enable
PHANTOM_FUNC_EN (R)	9	0x0	Enables a device to use unclaimed functions as Phantom Functions to extend the number of outstanding transaction identifiers. If the bit is cleared, the device is not allowed to use Phantom Functions. 0=Disable 1=Enable
AUX_POWER_PM_EN (R)	10	0x0	Enables a device to draw AUX power independent of PME AUX power. 0=Disable 1=Enable
NO_SNOOP_EN	11	0x1	If this bit is set to 1, the device is permitted to set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency. Default value of this bit is 1. 0=Disable 1=Enable
MAX_REQUEST_SIZE (R)	14:12	0x0	Sets the maximum Read Request size for the Device as a Requester. Default value of this field is 010b. 0=128B size

BRIDGE_CFG_RETRY_EN (R)	15	0x0	This field enables PCI Express to PCI/PCI-X bridges to return Configuration Request Retry Status (CRS) in response to configuration requests that target devices below the bridge. 0=Disable 1=Enable
The Device Control register controls PCI Express device specific parameters.			

PCIE_DEVICE_STATUS - RW - 16 bits - [pcieConfigDev[13:2]:0x62]			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR	0	0x0	Indicates status of correctable errors detected.
NON_FATAL_ERR	1	0x0	Indicates status of Nonfatal errors detected.
FATAL_ERR	2	0x0	Indicates status of Fatal errors detected.
USR_DETECTED	3	0x0	Indicates that the device received an Unsupported Request.
AUX_PWR	4	0x0	Devices that require AUX power report this bit as set if AUX power is detected by the device.
TRANSACTIONS_PEND (R)	5	0x0	Endpoints:This bit when set indicates that the device has issued Non-Posted Requests which have not been completed. Root and Switch Ports: This bit when set indicates that a Port has issued Non-Posted Requests on its own behalf (using the Port's own Requester ID) which have not been completed.
The Device Status register provides information about PCI Express device specific parameters.			

PCIE_LINK_CAP - RW - 32 bits - [pcieConfigDev[13:2]:0x64]			
Field Name	**Bits**	**Default**	**Description**
LINK_SPEED (R)	3:0	0x1	Indicates the maximum Link speed of the given PCI Express Link. 1=2.5 Gb/s 2=5.0 Gb/s
LINK_WIDTH (R)	9:4	0x0	Indicates the maximum width of the given PCI Express Link. 1=x1 2=x2 4=x4 8=x8 12=x12 16=x16 32=x32
PM_SUPPORT (R)	11:10	0x3	Indicates the level of ASPM supported on the given PCI Express Link.
L0S_EXIT_LATENCY (R)	14:12	0x1	Indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete the transition from L0s to L0.
L1_EXIT_LATENCY (R)	17:15	0x2	Indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete the transition from L0s to L0.
CLOCK_POWER_MANAGEMENT (R)	18	0x0	Indicates, in the component tolerates removal of REFCLK via the CLKREQ# mechanism, when the Link is in L1 and L23Ready.
SURPRISE_DOWN_ERR_REPORTING (R)	19	0x0	Indicates if the component supports the detecting and reporting of a Surprise Down error condition.
DL_ACTIVE_REPORTING_CAPABLE (R)	20	0x0	Indicates if the component supports the reporting of DL_Active state of the DLLSM.
LINK_BW_NOTIFICATION_CAP (R)	21	0x0	Indicates if the component supports the Link Bandwidth Notification status and interrupt mechanisms.
PORT_NUMBER (R)	31:24	0x0	Indicates the PCI Express Port number for the given PCI Express Link.
The Link Capabilities register identifies PCI Express Link specific capabilities.			

PCIE_LINK_CNTL - RW - 16 bits - [pcieConfigDev[13:2]:0x68]			
Field Name	**Bits**	**Default**	**Description**
PM_CONTROL	1:0	0x0	Controls the level of ASPM supported on the given PCI Express Link. Defined encodings are as follows: 00b=Disabled 01b=L0s Entry Enabled 10b=L1 Entry Enabled 11b=L0s and L1 Entry Enabled
READ_CPL_BOUNDARY (R)	3	0x0	Read Completion Boundary. Indicates the RCB value for the Root Port 0=64 Byte 1=128 Byte
LINK_DIS	4	0x0	Disables the Link when set to 1b. Default value of this field is 0b.
RETRAIN_LINK (W)	5	0x0	A write of 1b to this bit initiates Link retraining by directing the Physical Layer LTSSM to the Recovery state. Reads of this bit always return 0b.
COMMON_CLOCK_CFG	6	0x0	Indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. The default value of this field is 0b.
EXTENDED_SYNC	7	0x0	Forces the transmission of 4096 FTS ordered sets in the L0s state followed by a single SKP ordered set
CLOCK_POWER_MANAGEMENT_EN	8	0x0	Determines if device is permitted to use CLKREQ# signal to power manage link clock.
HW_AUTONOMOUS_WIDTH_DISABLE	9	0x0	When set to 1, this bit disables hardware from changing the link width for reasons other than attempting to correct an unreliable link operation by reducing link width.
LINK_BW_MANAGEMENT_INT_EN	10	0x0	Enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been set.
LINK_AUTONOMOUS_BW_INT_EN	11	0x0	Enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been set.
The Link Control register controls PCI Express Link specific parameters.			

PCIE_LINK_STATUS - RW - 16 bits - [pcieConfigDev[13:2]:0x6A]			
Field Name	**Bits**	**Default**	**Description**
CURRENT_LINK_SPEED (R)	3:0	0x1	Indicates the negotiated Link speed of the given PCI Express Link 1=2.5 Gb/s 2=5.0 Gb/s

NEGOTIATED_LINK_WIDTH (R)	9:4	0x0	Indicates the negotiated width of the given PCI Express Link. The defined encodings are as follows: 000001b x1 000010b x2 000100b x4 001000b x8 001100b x12 010000b x16 100000b x32 All other encodings are reserved. 1=x1 2=x2 4=x4 8=x8 12=x12 16=x16 32=x32
LINK_TRAINING (R)	11	0x0	This read-only bit indicates that Link training is in progress (Physical Layer LTSSM in Configuration or Recovery state) or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit once Link training is complete.
SLOT_CLOCK_CFG (R)	12	0x1	Indicates that the component uses the same physical reference clock that the platform provides on the connector. If the device uses an independent clock irrespective of the presence of a reference on the connector, this bit must be clear. 0=Diff Clock 1=Same Clock
DL_ACTIVE (R)	13	0x0	indicates the status of the Data Link Control and Management State Machine. It returns 1b to indicate DL_Active state, 0b otherwise.
LINK_BW_MANAGEMENT_STATUS	14	0x0	This bit is set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: (1) A Link retraining has completed following a write of 1b to the Retrain Link bit. (2) Hardware has changed the Link speed of width to attenmpt to correct unreliable Link operation, either through an LTSSM timeout or a higer level process.
LINK_AUTONOMOUS_BW_STATUS	15	0x0	This bit is set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation.
The Link Status register provides information about PCI Express Link specific parameters.			

PCIE_SLOT_CAP - RW - 32 bits - [pcieConfigDev[13:2]:0x6C]			
Field Name	**Bits**	**Default**	**Description**
ATTN_BUTTON_PRESENT (R)	0	0x0	Indicates that an Attention Button is implemented on the chassis for this slot
PWR_CONTROLLER_PRESENT (R)	1	0x0	Indicates that a Power Controller is implemented for this slot.
MRL_SENSOR_PRESENT (R)	2	0x0	Indicates that an Manually-operated Retention Latch Sensor is implemented on the chassis for this slot.
ATTN_INDICATOR_PRESENT (R)	3	0x0	Indicates that an Attention Indicator is implemented on the chassis for this slot.
PWR_INDICATOR_PRESENT (R)	4	0x0	Indicates that a Power Indicator is implemented on the chassis for this slot
HOTPLUG_SURPRISE	5	0x0	Indicates that a device present in this slot might be removed from the system without any prior notification.

HOTPLUG_CAPABLE	6	0x0	Indicates that this slot is capable of supporting Hot-Plug operations.
SLOT_PWR_LIMIT_VALUE	14:7	0x0	In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot
SLOT_PWR_LIMIT_SCALE	16:15	0x0	Specifies the scale used for the Slot Power Limit Value
ELECTROMECH_INTERLOCK_PRESENT (R)	17	0x0	Indicates that an Electromechanical Interlock is implemented on the chassis for this slot.
NO_COMMAND_COMPLETED_SUPPORTED (R)	18	0x1	Indicates that this slot does not generate software notification when an issued command is completed by the Hot-Plug Controller.
PHYSICAL_SLOT_NUM	31:19	0x0	This hardware initialized field indicates the physical slot number attached to this Port.
The Slot Capabilities register identifies PCI Express slot specific capabilities.			

PCIE_SLOT_CNTL - RW - 16 bits - [pcieConfigDev[13:2]:0x70]			
Field Name	**Bits**	**Default**	**Description**
ATTN_BUTTON_PRESSED_EN	0	0x0	Enables the generation of Hot-Plug interrupt or wakeup event on an attention button pressed event.
PWR_FAULT_DETECTED_EN	1	0x0	Enables software notification on a power fault event
MRL_SENSOR_CHANGED_EN	2	0x0	Enables software notification on a MRL sensor change event
PRESENCE_DETECT_CHANGED_EN	3	0x0	This bit is set when the value reported in the Presence Detect State bit is changed.
COMMAND_COMPLETED_INTR_EN	4	0x0	Enables the generation of Hot-Plug interrupt when a command is completed by the Hot-Plug Controller.
HOTPLUG_INTR_EN	5	0x0	Enables generation of Hot-Plug interrupt on enabled Hot-Plug events.
ATTN_INDICATOR_CNTL	7:6	0x0	Reads to this register return the current state of the Attention Indicator. Writes to this register set the Attention Indicator.
PWR_INDICATOR_CNTL	9:8	0x0	Reads to this register return the current state of the Power Indicator. Writes to this register set the Power Indicator.
PWR_CONTROLLER_CNTL	10	0x0	When read this register returns the current state of the Power applied to the slot. When written sets the power state of the slot per the defined encodings.
ELECTROMECH_INTERLOCK_CNTL	11	0x0	If an electromechanical interlock is implemented, a write of 1b causes the state of the interlock to toggle.
DL_STATE_CHANGED_EN	12	0x0	If the Data Link Layer Link Active Capability is implemented, this bit, when set, enables software notification when the Data Link Layer Link Active Reporting bit is changed.
The Slot Control register controls PCI Express Slot specific parameters.			

PCIE_SLOT_STATUS - RW - 16 bits - [pcieConfigDev[13:2]:0x72]			
Field Name	**Bits**	**Default**	**Description**
ATTN_BUTTON_PRESSED	0	0x0	This bit is set when the attention button is pressed.
PWR_FAULT_DETECTED	1	0x0	This bit is set when the power controller detects a power fault at this slot
MRL_SENSOR_CHANGED	2	0x0	This bit is set when a MRL sensor state change is detected.
PRESENCE_DETECT_CHANGED	3	0x0	This bit is set when the value reported in the Presence Detect State bit is changed.
COMMAND_COMPLETED	4	0x0	This bit is set when the Hot-Plug Controller completes an issued command.
MRL_SENSOR_STATE	5	0x0	This bit reports the status of the MRL sensor
PRESENCE_DETECT_STATE	6	0x0	Indicates the presence of an adapter in the slot.
ELECTROMECH_INTERLOCK_STATUS	7	0x0	Indicates the status of the Electromechanical Interlock.
DL_STATE_CHANGED	8	0x0	This bit is set when the value reported in the Data Link Layer Link Active bit of the Link Status register is changed.
The Slot Status register provides information about PCI Express Slot specific parameters.			

PCIE_ROOT_CNTL - RW - 16 bits - [pcieConfigDev[13:2]:0x74]			
Field Name	**Bits**	**Default**	**Description**
SERR_ON_CORR_ERR_EN	0	0x0	System Error on Correctable Error Enable. If set this bit indicates that a System Error should be generated if a correctable error is reported by any of the devices in the hierarchy associated with this Root Port.
SERR_ON_NONFATAL_ERR_EN	1	0x0	System Error on Non-Fatal Error Enable. If set this bit indicates that a System Error should be generated if a Non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port.
SERR_ON_FATAL_ERR_EN	2	0x0	System Error on Fatal Error Enable. If set this bit indicates that a System Error should be generated if a Fatal error is reported by any of the devices in the hierarchy associated with this Root Port.
PM_INTERRUPT_EN	3	0x0	PME Interrupt Enable. This bit when set enables interrupt generation upon receipt of a PME Message.
CRS_SOFTWARE_VISIBILITY_EN	4	0x0	Enables the Root Port to return Configuration Request Retry Status Completion Status to software.
The Root Control register controls PCI Express Root Complex specific parameters.			

PCIE_ROOT_CAP - RW - 16 bits - [pcieConfigDev[13:2]:0x76]			
Field Name	**Bits**	**Default**	**Description**
CRS_SOFTWARE_VISIBILITY (R)	0	0x1	Indicates the Root Port is capable of returning Configuration Request Retry Status (CRS) Completion Status to software.
The Root Capabilities register identifies PCI Express Root Complex specific capabilities.			

PCIE_ROOT_STATUS - RW - 32 bits - [pcieConfigDev[13:2]:0x78]			
Field Name	**Bits**	**Default**	**Description**
PME_REQUESTOR_ID (R)	15:0	0x0	Indicates the PCI requestor ID of the last PME requestor.
PME_STATUS	16	0x0	Indicates that PME was asserted by the requestor ID indicated in the PME Requestor ID field.
PME_PENDING (R)	17	0x0	This read-only bit indicates that another PME is pending when the PME Status bit is set.
The Root Status register provides information about PCI Express device specific parameters.			

PCIE_DEVICE_CAP2 - RW - 32 bits - [pcieConfigDev[13:2]:0x7C]			
Field Name	**Bits**	**Default**	**Description**
CPL_TIMEOUT_RANGE_SUPPORTED (R)	3:0	0x0	PCIe® completion timeout range supported
CPL_TIMEOUT_DIS_SUPPORTED (R)	4	0x0	PCIe completion timeout disabled supported
ARI_FORWARDING_SUPPORTED (R)	5	0x0	ARI Forwarding supported
The Device Capabilities 2 register identifies PCI Express device specific capabilities.			

PCIE_DEVICE_CNTL2 - RW - 16 bits - [pcieConfigDev[13:2]:0x80]			
Field Name	**Bits**	**Default**	**Description**
CPL_TIMEOUT_VALUE	3:0	0x0	PCIe® completion timeout value
CPL_TIMEOUT_DIS	4	0x0	Disables PCIe completion timeout
ARI_FORWARDING_EN	5	0x0	Enables ARI Forwarding
The Device Control 2 register controls PCI Express device specific parameters.			

PCIE_DEVICE_STATUS2 - RW - 16 bits - [pcieConfigDev[13:2]:0x82]			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	15:0	0x0	Reserved
The Device Status 2 register provides information about PCI Express device specific parameters.			

PCIE_LINK_CAP2 - RW - 32 bits - [pcieConfigDev[13:2]:0x84]			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	31:0	0x0	Reserved
The Link Capabilities 2 register identifies PCI Express Link specific capabilities.			

PCIE_LINK_CNTL2 - RW - 16 bits - [pcieConfigDev[13:2]:0x88]			
Field Name	**Bits**	**Default**	**Description**
TARGET_LINK_SPEED	3:0	0x1	The upper limit on the operational speed. This field restricts the data rate values advertised by an upstream component.
ENTER_COMPLIANCE	4	0x0	Forces a port's transmitter to enter Compliance.
HW_AUTONOMOUS_SPEED_DISABLE	5	0x0	Controls the component's ability to autonomously direct changes in link speed.
SELECTABLE_DEEMPHASIS (R)	6	0x0	Selectable de-emphasis (in GEN 2 data rate) 0 = -6dB 1 = -3.6dB
XMIT_MARGIN	9:7	0x0	Controls the value of the non-deemphasized voltage level at the transmitter pins
ENTER_MOD_COMPLIANCE	10	0x0	LTSSM transmits modified compliance pattern in Polling.Compliance if this bit is set to 1.
COMPLIANCE_SOS	11	0x0	When set to 1, the LTSSM is required to send SOS perioldically in between the (modified) compliance patterns.
COMPLIANCE_DEEMPHASIS	12	0x0	Sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the `enter compliance' bit being 1b. When the link is operating at 2.5 GT/s, the setting of this bit has no effect. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. 0=-6 dB 1=-3dB
The Link Control 2 register controls PCI Express Link specific parameters.			

PCIE_LINK_STATUS2 - RW - 16 bits - [pcieConfigDev[13:2]:0x8A]			
Field Name	**Bits**	**Default**	**Description**
CUR_DEEMPHASIS_LEVEL (R)	0	0x0	When the link is operating at 5GT/s speed, this bit reflects the level of de-emphasis.
The Link Status 2 register provides information about PCI Express Link specific parameters.			

PCIE_SLOT_CAP2 - RW - 32 bits - [pcieConfigDev[13:2]:0x8C]			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	31:0	0x0	Reserved
The Slot Capabilities 2 register identifies PCI Express slot specific capabilities.			

PCIE_SLOT_CNTL2 - RW - 16 bits - [pcieConfigDev[13:2]:0x90]			
Field Name	**Bits**	**Default**	**Description**

RESERVED (R)	15:0	0x0	Reserved
The Slot Control 2 register controls PCI Express Slot specific parameters.			

PCIE_SLOT_STATUS2 - RW - 16 bits - [pcieConfigDev[13:2]:0x92]			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	15:0	0x0	Reserved
The Slot Status 2 register provides information about PCI Express Slot specific parameters.			

PCIE_MSI_CAP_LIST - R - 16 bits - [pcieConfigDev[13:2]:0xA0]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0x5	Register identifies if a device function is MSI capable
NEXT_PTR	15:8	0xb0	Pointer to the next item on the capabilities list
Message Signaled Interrupt Capability Registers			

PCIE_MSI_MSG_CNTL - RW - 16 bits - [pcieConfigDev[13:2]:0xA2]			
Field Name	**Bits**	**Default**	**Description**
MSI_EN	0	0x0	Enables MSI messaging 0=Disable 1=Enable
MSI_MULTI_CAP (R)	3:1	0x0	Multiple Message Capable register is read to determine the number of requested messages. 0=1 message allocated 1=2 messages allocated 2=4 messages allocated 3=8 messages allocated 4=16 messages allocated 5=32 messages allocated 6=Reserved 7=Reserved
MSI_MULTI_EN	6:4	0x0	Multiple Message Enable register is written to indicate the number of allocated messages. 0=1 message allocated 1=2 messages allocated 2=4 messages allocated 3=8 messages allocated 4=16 messages allocated 5=32 messages allocated 6=Reserved 7=Reserved
MSI_64BIT (R)	7	0x0	Signifies if a device function is capable of generating a 64-bit message address 0=Not capable of generating 1 64-bit message address 1=Capable of generating 1 64-bit message address
Message Signaled Interrupts Control Register			

PCIE_MSI_MSG_ADDR_LO - RW - 32 bits - [pcieConfigDev[13:2]:0xA4]			
Field Name	**Bits**	**Default**	**Description**
MSI_MSG_ADDR_LO	31:2	0x0	Message Lower Address. Use lower 32-bits of address
Message Lower Address			

PCIE_MSI_MSG_ADDR_HI - RW - 32 bits - [pcieConfigDev[13:2]:0xA8]			
Field Name	**Bits**	**Default**	**Description**
MSI_MSG_ADDR_HI (R)	31:0	0x0	Message Upper Address. Use upper 32-bit of address
Message Upper Address			

PCIE_MSI_MSG_DATA_64 - RW - 16 bits - [pcieConfigDev[13:2]:0xAC]			
Field Name	**Bits**	**Default**	**Description**
MSI_DATA_64 (R)	15:0	0x0	Message Data. System specified.
64-bit MSI Message Data			

PCIE_MSI_MSG_DATA - RW - 32 bits - [pcieConfigDev[13:2]:0xA8]			
Field Name	**Bits**	**Default**	**Description**
MSI_DATA	15:0	0x0	Message Data. System specified.
MSI Message Data			

PCIE_SSID_CAP_LIST - R - 32 bits - [pcieConfigDev[13:2]:0xB0]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	7:0	0xd	Capability ID
NEXT_PTR (R)	15:8	0xb8	Pointer to next capability register
Subsystem ID Capability List			

PCIE_SSID_ID - R - 32 bits - [pcieConfigDev[13:2]:0xB4]			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID	15:0	0x0	Subsystem Vendor ID
SUBSYSTEM_ID	31:16	0x0	Subsystem ID
Subsystem ID			

PCIE_MSI_MAP_CAP_LIST - R - 32 bits - [pcieConfigDev[13:2]:0xB8]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	7:0	0x8	Identifies this as a HyperTransport capability list item.
NEXT_PTR (R)	15:8	0x0	Pointer to the next item in the capabilities list. Must be NULL for the final item in the list. This field is read only.
EN (R)	16	0x1	Indicates if the mapping is active.
FIXD (R)	17	0x1	Indicates if the programming address is fixed.
CAP_TYPE (R)	31:27	0x15	Indicates this as the MSI Mapping Capability block.
MSI Mapping Capability Register			

PCIE_PORT_INDEX - RW - 32 bits - [pcieConfigDev[13:2]:0xE0]			
Field Name	**Bits**	**Default**	**Description**
PCIE_INDEX	7:0	0x0	Index of bifdecp
Index register for the PCI Express port indirect registers			

PCIE_PORT_DATA - RW - 32 bits - [pcieConfigDev[13:2]:0xE4]			
Field Name	**Bits**	**Default**	**Description**
PCIE_DATA	31:0	0x0	Data of bifdecp

Data register for the PCI Express port indirect registers

PCIE_VENDOR_SPECIFIC_ENH_CAP_LIST - R - 32 bits - [pcieConfigDev[13:2]:0x100]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0xb	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x110	Contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.
Vendor Specific Capability			

PCIE_VENDOR_SPECIFIC_HDR - R - 32 bits - [pcieConfigDev[13:2]:0x104]			
Field Name	**Bits**	**Default**	**Description**
VSEC_ID	15:0	0x1	Vendor-defined ID number.
VSEC_REV	19:16	0x1	Vendor-defined revision number.
VSEC_LENGTH	31:20	0x10	Number of bytes in the entire VSEC structure.
Vendor Specific Header			

PCIE_VENDOR_SPECIFIC1 - RW - 32 bits - [pcieConfigDev[13:2]:0x108]			
Field Name	**Bits**	**Default**	**Description**
SCRATCH	31:0	0x0	PCIe® scratch register.
Vendor-Specific Scratch Register 1			

PCIE_VENDOR_SPECIFIC2 - RW - 32 bits - [pcieConfigDev[13:2]:0x10C]			
Field Name	**Bits**	**Default**	**Description**
SCRATCH	31:0	0x0	PCI® scratch register.
Vendor-Specific Scratch Register 2			

PCIE_VC_ENH_CAP_LIST - R - 32 bits - [pcieConfigDev[13:2]:0x110]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0x2	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x140	Contains the offset to the next PCI Express® capability structure or 000h if no other items exist in the linked list of capabilities.
Virtual Channel Enhanced Capability Header			

PCIE_PORT_VC_CAP_REG1 - R - 32 bits - [pcieConfigDev[13:2]:0x114]			
Field Name	**Bits**	**Default**	**Description**
EXT_VC_COUNT	2:0	0x0	Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. This field is valid for all devices.

LOW_PRIORITY_EXT_VC_COUNT	6:4	0x0	Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC group
REF_CLK	9:8	0x0	Indicates the reference clock for Virtual Channels that support time-based WRR Port Arbitration.
PORT_ARB_TABLE_ENTRY_SIZE	11:10	0x0	Indicates the size (in bits) of Port Arbitration table entry in the device.
Port VC Capability Register 1			

PCIE_PORT_VC_CAP_REG2 - R - 32 bits - [pcieConfigDev[13:2]:0x118]			
Field Name	**Bits**	**Default**	**Description**
VC_ARB_CAP	7:0	0x0	Indicates the types of VC Arbitration supported by the device for the Low Priority Virtual Channel group
VC_ARB_TABLE_OFFSET	31:24	0x0	Indicates the location of the VC Arbitration Table.
Port VC Capability Register 2			

PCIE_PORT_VC_CNTL - RW - 16 bits - [pcieConfigDev[13:2]:0x11C]			
Field Name	**Bits**	**Default**	**Description**
LOAD_VC_ARB_TABLE (R)	0	0x0	Used for software to update the VC Arbitration Table.
VC_ARB_SELECT	3:1	0x0	Used for software to configure the VC arbitration by selecting one of the supported VC Arbitration schemes
Port VC Control Register			

PCIE_PORT_VC_STATUS - R - 16 bits - [pcieConfigDev[13:2]:0x11E]			
Field Name	**Bits**	**Default**	**Description**
VC_ARB_TABLE_STATUS	0	0x0	Indicates the coherency status of the VC Arbitration Table
Port VC Status Register			

PCIE_VC0_RESOURCE_CAP - R - 32 bits - [pcieConfigDev[13:2]:0x120]			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_CAP	7:0	0x1	Indicates types of Port Arbitration supported by the VC resource.
REJECT_SNOOP_TRANS	15	0x0	When set to zero, transactions with or without the No Snoop bit set within the TLP Header are allowed on this VC
MAX_TIME_SLOTS	21:16	0x0	Indicates the maximum number of time slots that the VC resource is capable of supporting
PORT_ARB_TABLE_OFFSET	31:24	0x0	Indicates the location of the Port Arbitration Table associated with the VC resource.
VC0 Resource Capability Register			

PCIE_VC0_RESOURCE_CNTL - RW - 32 bits - [pcieConfigDev[13:2]:0x124]			
Field Name	**Bits**	**Default**	**Description**
TC_VC_MAP_TC0 (R)	0	0x1	Indicates the TCs that are mapped to the VC resource
TC_VC_MAP_TC1_7	7:1	0x7f	Indicates the TCs that are mapped to the VC resource
LOAD_PORT_ARB_TABLE (R)	16	0x0	Updates the Port Arbitration logic from the Port Arbitration Table for the VC resource.
PORT_ARB_SELECT	19:17	0x0	Configures the VC resource to provide a particular Port Arbitration service.
VC_ID (R)	26:24	0x0	Assigns a VC ID to the VC resource
VC_ENABLE (R)	31	0x1	Enables a Virtual Channel.
VC0 Resource Control Register			

PCIE_VC0_RESOURCE_STATUS - R - 16 bits - [pcieConfigDev[13:2]:0x12A]			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_TABLE_STATUS	0	0x0	Indicates the coherency status of the Port Arbitration Table associated with the VC resource
VC_NEGOTIATION_PENDING	1	0x1	Indicates whether the Virtual Channel negotiation (initialization or disabling) is in pending state
VC0 Resource Status Register			

PCIE_VC1_RESOURCE_CAP - R - 32 bits - [pcieConfigDev[13:2]:0x12C]			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_CAP	7:0	0x1	Indicates types of Port Arbitration supported by the VC resource.
REJECT_SNOOP_TRANS	15	0x0	When set to zero, transactions with or without the No Snoop bit set within the TLP Header are allowed on this VC
MAX_TIME_SLOTS	21:16	0x0	Indicates the maximum number of time slots that the VC resource is capable of supporting
PORT_ARB_TABLE_OFFSET	31:24	0x0	Indicates the location of the Port Arbitration Table associated with the VC resource.
VC1 Resource Capability Register			

PCIE_VC1_RESOURCE_CNTL - RW - 32 bits - [pcieConfigDev[13:2]:0x130]			
Field Name	**Bits**	**Default**	**Description**
TC_VC_MAP_TC0 (R)	0	0x0	Indicates the TCs that are mapped to the VC resource
TC_VC_MAP_TC1_7	7:1	0x0	Indicates the TCs that are mapped to the VC resource
LOAD_PORT_ARB_TABLE (R)	16	0x0	Updates the Port Arbitration logic from the Port Arbitration Table for the VC resource.
PORT_ARB_SELECT	19:17	0x0	Configures the VC resource to provide a particular Port Arbitration service.
VC_ID	26:24	0x0	Assigns a VC ID to the VC resource
VC_ENABLE	31	0x0	Enables a Virtual Channel.
VC1 Resource Control Register			

PCIE_VC1_RESOURCE_STATUS - R - 16 bits - [pcieConfigDev[13:2]:0x136]			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_TABLE_STATUS	0	0x0	Indicates the coherency status of the Port Arbitration Table associated with the VC resource
VC_NEGOTIATION_PENDING	1	0x1	Indicates whether the Virtual Channel negotiation (initialization or disabling) is in pending state
VC1 Resource Status Register			

PCIE_DEV_SERIAL_NUM_ENH_CAP_LIST - R - 32 bits - [pcieConfigDev[13:2]:0x140]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	15:0	0x3	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER (R)	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR (R)	31:20	0x150	Contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.

Device Serial Number Enhanced Capability header

PCIE_DEV_SERIAL_NUM_DW1 - R - 32 bits - [pcieConfigDev[13:2]:0x144]			
Field Name	**Bits**	**Default**	**Description**
SERIAL_NUMBER_LO	31:0	0x0	Lower 32-bits of IEEE defined 64-bit extended unique identifier. (EUI-64)
PCI Express Device Serial Number (1st DW)			

PCIE_DEV_SERIAL_NUM_DW2 - R - 32 bits - [pcieConfigDev[13:2]:0x148]			
Field Name	**Bits**	**Default**	**Description**
SERIAL_NUMBER_HI	31:0	0x0	Upper 32-bits of IEEE defined 64-bit extended unique identifier. (EUI-64)
PCI Express Device Serial Number (2nd DW)			

PCIE_ADV_ERR_RPT_ENH_CAP_LIST - R - 32 bits - [pcieConfigDev[13:2]:0x150]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	15:0	0x1	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER (R)	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR (R)	31:20	0x190	Contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.
Advanced Error Reporting Enhanced Capability header			

PCIE_UNCORR_ERR_STATUS - RW - 32 bits - [pcieConfigDev[13:2]:0x154]			
Field Name	**Bits**	**Default**	**Description**
DLP_ERR_STATUS	4	0x0	Data Link Protocol Error Status *
SURPDN_ERR_STATUS (R)	5	0x0	Surprise Down Error Status
PSN_ERR_STATUS	12	0x0	Poisoned TLP Status *
FC_ERR_STATUS (R)	13	0x0	Flow Control Protocol Error Status
CPL_TIMEOUT_STATUS	14	0x0	Completion Timeout Status *
CPL_ABORT_ERR_STATUS	15	0x0	Completer Abort Status *
UNEXP_CPL_STATUS	16	0x0	Unexpected Completion Status *
RCV_OVFL_STATUS (R)	17	0x0	Receiver Overflow Status
MAL_TLP_STATUS	18	0x0	Malformed TLP Status *
ECRC_ERR_STATUS	19	0x0	ECRC Error Status *
UNSUPP_REQ_ERR_STATUS	20	0x0	Unsupported Request Error Status *
ACS_VIOLATION_STATUS	21	0x0	ACS Violation Error Status *
* The contents of this register are preserved across a warm reset and are cleared by a cold reset. The Uncorrectable Error Status register reports error status of individual error sources on a PCI Express device.			

PCIE_UNCORR_ERR_MASK - RW - 32 bits - [pcieConfigDev[13:2]:0x158]			
Field Name	**Bits**	**Default**	**Description**
DLP_ERR_MASK	4	0x0	Data Link Protocol Error Mask
SURPDN_ERR_MASK (R)	5	0x0	Surprise Down Error Mask
PSN_ERR_MASK	12	0x0	Poisoned TLP Mask
FC_ERR_MASK (R)	13	0x0	Flow Control Protocol Error Mask
CPL_TIMEOUT_MASK	14	0x0	Completion Timeout Mask
CPL_ABORT_ERR_MASK	15	0x0	Completer Abort Mask
UNEXP_CPL_MASK	16	0x0	Unexpected Completion Mask
RCV_OVFL_MASK (R)	17	0x0	Receiver Overflow Mask
MAL_TLP_MASK	18	0x0	Malformed TLP Mask

ECRC_ERR_MASK	19	0x0	ECRC Error Mask
UNSUPP_REQ_ERR_MASK	20	0x0	Unsupported Request Error Mask
ACS_VIOLATION_MASK	21	0x0	ACS Violation Mask
The Uncorrectable Error Mask register controls reporting of individual errors by the device to the PCI Express Root Complex via a PCI Express error Message.			

PCIE_UNCORR_ERR_SEVERITY - RW - 32 bits - [pcieConfigDev[13:2]:0x15C]			
Field Name	**Bits**	**Default**	**Description**
DLP_ERR_SEVERITY	4	0x1	Data Link Protocol Error Severity
SURPDN_ERR_SEVERITY (R)	5	0x1	Surprise Down Error Severity
PSN_ERR_SEVERITY	12	0x0	Poisoned TLP Severity
FC_ERR_SEVERITY (R)	13	0x1	Flow Control Protocol Error Severity
CPL_TIMEOUT_SEVERITY	14	0x0	Completion Timeout Error Severity
CPL_ABORT_ERR_SEVERITY	15	0x0	Completer Abort Error Severity
UNEXP_CPL_SEVERITY	16	0x0	Unexpected Completion Error Severity
RCV_OVFL_SEVERITY (R)	17	0x1	Receiver Overflow Error Severity
MAL_TLP_SEVERITY	18	0x1	Malformed TLP Severity
ECRC_ERR_SEVERITY	19	0x0	ECRC Error Severity
UNSUPP_REQ_ERR_SEVERITY	20	0x0	Unsupported Request Error Severity
ACS_VIOLATION_SEVERITY	21	0x0	ACS Violation Severity
The Uncorrectable Error Severity register controls whether an individual error is reported as a Nonfatal or Fatal error.			

PCIE_CORR_ERR_STATUS - RW - 32 bits - [pcieConfigDev[13:2]:0x160]			
Field Name	**Bits**	**Default**	**Description**
RCV_ERR_STATUS	0	0x0	Receiver Error Status *
BAD_TLP_STATUS	6	0x0	Bad TLP Status *
BAD_DLLP_STATUS	7	0x0	Bad DLLP Status *
REPLAY_NUM_ROLLOVER_STATUS	8	0x0	REPLAY_NUM Rollover Status *
REPLAY_TIMER_TIMEOUT_STATUS	12	0x0	Replay Timer Timeout Status *
ADVISORY_NONFATAL_ERR_STATUS	13	0x0	Advisory Non-Fatal Status *
* The contents of this register are preserved across a warm reset and are cleared by a cold reset. The Correctable Error Status register reports error status of individual correctable error sources on a PCI Express device.			

PCIE_CORR_ERR_MASK - RW - 32 bits - [pcieConfigDev[13:2]:0x164]			
Field Name	**Bits**	**Default**	**Description**
RCV_ERR_MASK	0	0x0	Receiver Error Mask
BAD_TLP_MASK	6	0x0	Bad TLP Mask
BAD_DLLP_MASK	7	0x0	Bad DLLP Mask
REPLAY_NUM_ROLLOVER_MASK	8	0x0	REPLAY_NUM Rollover Mask
REPLAY_TIMER_TIMEOUT_MASK	12	0x0	Replay Timer Timeout Mask
ADVISORY_NONFATAL_ERR_MASK	13	0x1	Advisory Non-Fatal Mask
The Correctable Error Mask register controls reporting of individual correctable errors by device to the PCI Express Root Complex via a PCI Express error Message.			

PCIE_ADV_ERR_CAP_CNTL - RW - 32 bits - [pcieConfigDev[13:2]:0x168]			
Field Name	**Bits**	**Default**	**Description**
FIRST_ERR_PTR (R)	4:0	0x0	The First Error Pointer is a read-only register that identifies the bit position of the first error reported in the Uncorrectable Error Status register. The contents of this register are preserved across a warm reset and are cleared by a cold reset.
ECRC_GEN_CAP (R)	5	0x0	Indicates that the device is capable of generating ECRC
ECRC_GEN_EN (RW)	6	0x0	Enables ECRC generation. Default value of this field is 0.
ECRC_CHECK_CAP (R)	7	0x0	Indicates that the device is capable of checking ECRC
ECRC_CHECK_EN (RW)	8	0x0	Enables ECRC checking. Default value of this field is 0.
Advanced Error Capabilities and Control Register			

PCIE_HDR_LOG0 - R - 32 bits - [pcieConfigDev[13:2]:0x16C]			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 1st DW The contents of this register are preserved across a warm reset and are cleared by a cold reset.
Header Log Register captures the Header for the TLP corresponding to a detected error			

PCIE_HDR_LOG1 - R - 32 bits - [pcieConfigDev[13:2]:0x170]			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 2nd DW The contents of this register are preserved across a warm reset and are cleared by a cold reset.
Header Log Register			

PCIE_HDR_LOG2 - R - 32 bits - [pcieConfigDev[13:2]:0x174]			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 3rd DW The contents of this register are preserved across a warm reset and are cleared by a cold reset.
Header Log Register			

PCIE_HDR_LOG3 - R - 32 bits - [pcieConfigDev[13:2]:0x178]			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 4th DW The contents of this register are preserved across a warm reset and are cleared by a cold reset.
Header Log Register			

PCIE_ROOT_ERR_CMD - RW - 32 bits - [pcieConfigDev[13:2]:0x17C]			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR_REP_EN	0	0x0	Correctable Error Reporting Enable. When set this bit enables the generation of an interrupt when a correctable error is reported by any of the devices in the hierarchy associated with this Root Port.
NONFATAL_ERR_REP_EN	1	0x0	Non-Fatal Error Reporting Enable. When set this bit enables the generation of an interrupt when a Non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port.
FATAL_ERR_REP_EN	2	0x0	Fatal Error Reporting Enable. When set this bit enables the generation of an interrupt when a Fatal error is reported by any of the devices in the hierarchy associated with this Root Port.
Root Error Command Register			

PCIE_ROOT_ERR_STATUS - RW - 32 bits - [pcieConfigDev[13:2]:0x180]			
Field Name	**Bits**	**Default**	**Description**
ERR_CORR_RCVD	0	0x0	Set when a correctable error Message is received and this bit is not already set. Default value of this field is 0. *
MULT_ERR_CORR_RCVD	1	0x0	Set when a correctable error Message is received and ERR_COR Received is already set. Default value of this field is 0. *

ERR_FATAL_NONFATAL_RCVD	2	0x0	Set when either a Fatal or a Non-fatal error Message is received and this bit is not already set. Default value of this field is 0. *
MULT_ERR_FATAL_NONFATAL_RCVD	3	0x0	Set when either a Fatal or a Non-fatal error is received and ERR_FATAL/NONFATAL Received is already set. Default value of this field is 0. *
FIRST_UNCORRECTABLE_FATAL	4	0x0	Set to 1b when the first Uncorrectable error Message received is for a Fatal error. Default value of this field is 0. *
NONFATAL_ERROR_MSG_RCVD	5	0x0	Set to 1b when one or more Non-Fatal Uncorrectable error Messages have been received. Default value of this field is 0. *
FATAL_ERROR_MSG_RCVD	6	0x0	Set to 1b when one or more Fatal Uncorrectable error Messages have been received. Default value of this field is 0. *
ADV_ERR_INT_MSG_NUM (R)	31:27	0x0	Advanced Error Interrupt Message Number
* The contents of this register are preserved across a warm reset and are cleared by a cold reset.			
Root Error Status Register			

PCIE_ERR_SRC_ID - RW - 32 bits - [pcieConfigDev[13:2]:0x184]			
Field Name	**Bits**	**Default**	**Description**
ERR_COR_SRC_ID (R)	15:0	0x0	Loaded with the Requestor ID indicated in the received ERR_COR Message when the ERR_COR Received register is not already set. Default value of this field is 0. *
ERR_FATAL_NONFATAL_SRC_ID (R)	31:16	0x0	Loaded with the Requestor ID indicated in the received ERR_FATAL or ERR_NONFATAL Message when the ERR_FATAL/NONFATAL Received register is not already set. Default value of this field is 0. *
* The contents of this register are preserved across a warm reset and are cleared by a cold reset.			
The Error Source Identification register identifies the source (Requestor ID) of first correctable and uncorrectable (Non-fatal/Fatal) errors reported in the Root Error Status register.			

PCIE_ACS_ENH_CAP_LIST - R - 32 bits - [pcieConfigDev[13:2]:0x190]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0xd	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x0	This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.
ACS Enhanced Capability header			

PCIE_ACS_CAP - R - 16 bits - [pcieConfigDev[13:2]:0x194]			
Field Name	**Bits**	**Default**	**Description**
SOURCE_VALIDATION	0	0x0	Indicates that the component implements ACS Source Validation.
TRANSLATION_BLOCKING	1	0x0	Indicates that the component implements ACS Translation Blocking.
P2P_REQUEST_REDIRECT	2	0x0	Indicates that the component implements ACS P2P Request Redirect.
P2P_COMPLETION_REDIRECT	3	0x0	Indicates that the component implements ACS P2P Completion Redirect.
UPSTREAM_FORWARDING	4	0x0	Indicates that the component implements ACS Upstream Forwarding.
P2P_EGRESS_CONTROL	5	0x0	Indicates that the component implements ACS P2P Egress Control.

DIRECT_TRANSLATED_P2P	6	0x0	Indicates that the component implements ACS Direct Translated P2P.
EGRESS_CONTROL_VECTOR_SIZE	15:8	0x0	Encodings 01h-FFh directly indicate the number of applicable bits in the Egress Control Vector; the encoding 00h indicates 256 bits.
ACS Capability register			

PCIE_ACS_CNTL - RW - 16 bits - [pcieConfigDev[13:2]:0x196]			
Field Name	**Bits**	**Default**	**Description**
SOURCE_VALIDATION_EN	0	0x0	When set, the component validates the Bus Number from the Requester ID of Upstream Requests against the secondary / subordinate Bus Numbers.
TRANSLATION_BLOCKING_EN	1	0x0	When set, the component blocks all Upstream Memory Requests whose Address Translation field is not set to the default value.
P2P_REQUEST_REDIRECT_EN	2	0x0	In conjunction with ACS P2P Egress Control and ACS Direct Translated P2P mechanisms, determines when the component redirects P2P Requests Upstream.
P2P_COMPLETION_REDIRECT_EN	3	0x0	Determines when the component redirects P2P Completions Upstream; applicable only to Read Completions whose Relaxed Ordering Attribute is clear.
UPSTREAM_FORWARDING_EN	4	0x0	When set, the component forwards Upstream any Request or Completion TLPs it receives that were redirected Upstream by a component lower in the hierarchy.
P2P_EGRESS_CONTROL_EN (R)	5	0x0	In conjunction with the Egress Control Vector plus the ACS P2P Request Redirect and ACS Direct Translated P2P mechanisms, determines when to allow, disallow, or redirect P2P Requests.
DIRECT_TRANSLATED_P2P_EN	6	0x0	When set, overrides the ACS P2P Request Redirect and ACS P2P Egress Control mechanisms with P2P Memory Requests whose Address Translation field indicates a Translated address.
ACS Control register			

2.2.4 CLKCONFIG Registers

CLK_VENDOR_ID - R - 16 bits - clkconfig:0x0			
Field Name	**Bits**	**Default**	**Description**
VENDOR_ID	15:0	0x1002	Vendor Identifier. This 16-bit field identifies the manufacturer of the device: Advanced Micro Devices Inc.

CLK_DEVICE_ID - R - 16 bits - clkconfig:0x2			
Field Name	**Bits**	**Default**	**Description**
DEVICE_ID	15:0	0x5A22	Device Identifier. This 16-bit field is assigned by the device manufacturer and identifies the type of device

CLK_COMMAND - RW - 16 bits - clkconfig:0x4			
Field Name	**Bits**	**Default**	**Description**
IO_ACCESS_EN (R)	0	0x0	I/O Access Enable This register controls no hardware. This function does not respond to I/O cycles.
MEM_ACCESS_EN (R)	1	0x0	Memory Access Enable This register controls no hardware. This function does not respond to memory cycles.
BUS_MASTER_EN (R)	2	0x0	Bus Master Enable This register controls no hardware. This function does not generate its own DMA requests.
RESERVED_RO_3 (R)	3	0x0	Reserved for future use. This register controls no hardware
RESERVED_RO_4 (R)	4	0x0	Reserved for future use. This register controls no hardware
RESERVED_RO_5 (R)	5	0x0	Reserved for future use. This register controls no hardware
PARITY_ERROR_EN (R)	6	0x0	Parity Error Response This bit is always 0 because this function does not log errors in the master data error register.
Reserved0 (R)	7	0x0	Reserved for future use. This register controls no hardware
SERR_EN (R)	8	0x0	System Error Enable This register controls no hardware. This function does not generate system errors
RESERVED_RO_9 (R)	9	0x0	Reserved for future use. This register controls no hardware
INTERRUPT_DISABLE (R)	10	0x0	Interrupt Disable This register controls no hardware. This function does not generate interrupt requests.
Reserved (R)	15:11	0x0	Reserved for future use. This register controls no hardware

CLK_STATUS - RW - 16 bits - clkconfig:0x6			
Field Name	**Bits**	**Default**	**Description**
Reserved_2_0 (R)	2:0	0x0	Reserved for future use. This register controls no hardware
INTERRUPT_STATUS (R)	3	0x0	Interrupt Status This bit is always 0 because this function does not generate interrupts
CAP_LIST (R)	4	0x0	Capabilities List This bit is clear to indicate that this function does not support a capability list
RESERVED_RO_5 (R)	5	0x0	Reserved for future use. This register controls no hardware
Reserved (R)	6	0x0	Reserved for future use. This register controls no hardware
RESERVED_RO_7 (R)	7	0x0	Reserved for future use. This register controls no hardware

MASTER_DATA_ERROR (R)	8	0x0	Master Data Error This function does not set the master data error status bit because it does not accept dma read responses.
RESERVED_RO_10_9 (R)	10:9	0x0	Reserved for future use. This register controls no hardware
SIGNAL_TARGET_ABORT (R)	11	0x0	Signaled Target Abort This bit is always 0 because this function does not terminate transactions with target aborts.
RECEIVED_TARGET_ABORT (R)	12	0x0	Received Target Abort This bit is always 0 because this function is never the master of a transaction.
RECEIVED_MASTER_ABORT (R)	13	0x0	Received Master Abort This bit is always 0 because this function is never the master of a transaction.
SIGNALED_SYSTEM_ERROR (R)	14	0x0	Signaled System Error This bit is always 0 because this function is never signals system error.
DATA_ERROR_DETECTED (R)	15	0x0	Data Error Detected This bit is always 0 because this function is never the target of a transaction and thus cannot receive poisoned data

CLK_REVISION_ID - R - 8 bits - clkconfig:0x8			
Field Name	**Bits**	**Default**	**Description**
MINOR_REV_ID	3:0	0x0	Identifies stepping number of the function.
MAJOR_REV_ID	7:4	0x1	Identifies revision number of the function.

CLK_REGPROG_INF - R - 8 bits - clkconfig:0x9			
Field Name	**Bits**	**Default**	**Description**
REG_LEVEL_PROG_INF	7:0	0x0	Indicates a Host bridge function

CLK_SUB_CLASS - R - 8 bits - clkconfig:0xA			
Field Name	**Bits**	**Default**	**Description**
Reserved	6:0	0x0	Reserved for future use. This register controls no hardware.
SUB_CLASS_INF	7	0x0	Indicates a Host bridge function

CLK_BASE_CODE - R - 8 bits - clkconfig:0xB			
Field Name	**Bits**	**Default**	**Description**
BASE_CLASS_CODE	7:0	0x6	Indicates a Bridge function

CLK_CACHE_LINE - R - 8 bits - clkconfig:0xC			
Field Name	**Bits**	**Default**	**Description**
RESERVED_RO	7:0	0x0	Reserved for future use. This register controls no hardware.

CLK_LATENCY - RW - 8 bits - clkconfig:0xD			
Field Name	**Bits**	**Default**	**Description**
RESERVED_RO (R)	7:0	0x0	Reserved for future use. This register controls no hardware.

CLK_HEADER - R - 8 bits - clkconfig:0xE			
Field Name	**Bits**	**Default**	**Description**
HEADER_TYPE	6:0	0x0	Indicates that Type 00 Configuration Space Header format is supported
DEVICE_TYPE	7	0x1	Indicates a multi-function device 0=Single-Function Device 1=Multi-Function Device

CLK_BIST - R - 8 bits - clkconfig:0xF			
Field Name	**Bits**	**Default**	**Description**
RESERVED_RO	7:0	0x0	Reserved for future use. This register controls no hardware.

CLK_BAR1_RCRB - RW - 32 bits - clkconfig:0x14			
Field Name	**Bits**	**Default**	**Description**
MEM_IO (R)	0	0x0	Reserved for future use. This register controls no hardware.
TYPE (R)	2:1	0x0	Reserved for future use. This register controls no hardware.
PREFETCH_EN (R)	3	0x0	Reserved for future use. This register controls no hardware.
Reserved	11:4	0x0	Reserved for future use. This register controls no hardware.
RCRB_BASE (R)	31:12	0x0	Reserved for future use. This register controls no hardware.

CLK_ADAPTER_ID - R - 32 bits - clkconfig:0x2C			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID	15:0	0x1002	Subsystem vendor ID. This is the same subsystem vendor ID shown in device 0 function 0.
SUBSYSTEM_ID	31:16	0x5A10	Subsystem ID. This is the same subsystem ID shown in device 0 function 0.

CLK_CAPABILITIES_PTR - R - 32 bits - clkconfig:0x34			
Field Name	**Bits**	**Default**	**Description**
CAP_PTR	7:0	0x0	Reserved for future use. This register controls no hardware.
Reserved	31:8	0x0	Reserved for future use. This register controls no hardware.

CLK_INTERRUPT_LINE - RW - 8 bits - clkconfig:0x3C			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_LINE	7:0	0x0	This register is for read-write for software purposes but controls no hardware

CLK_INTERRUPT_PIN - R - 8 bits - clkconfig:0x3D			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_PIN	7:0	0x0	This register is always 0 to indicate that no legacy interrupts are supported from this function.

OSC_CONTROL - RW - 32 bits - clkconfig:0x40			
Field Name	**Bits**	**Default**	**Description**
OSC_EN	0	0x1	Reserved for future use. This register controls no hardware. Possible values: 0=Disable 1=Enable
XTAL_LOW_GAIN	1	0x0	Reserved for future use. This register controls no hardware. Possible values: 0=High Gain 1=Low Gain
Reserved0 (R)	3	0x0	Reserved for future use. This register controls no hardware.
CPU_STOP_ENABLE	4	0x0	Reserved for future use. This register controls no hardware. Possible values: 0=Disable 1=Enable
DC_STOP_ENABLE	5	0x0	Reserved for future use. This register controls no hardware.
GPP1_REFCLK_OE_TOGGLE	6	0x0	Reserved for future use. This register controls no hardware.
GPP3a_REFCLK_OE_TOGGLE	7	0x0	Reserved for future use. This register controls no hardware.
SB_REFCLK_OE_TOGGLE	8	0x0	Reserved for future use. This register controls no hardware.
Reserved1 (R)	11	0x0	Reserved for future use. This register controls no hardware.
CPUCLK_SE_OE_TOGGLE	12	0x0	Reserved for future use. This register controls no hardware.
CPUCLK_DIFF_OE_TOGGLE	13	0x0	Reserved for future use. This register controls no hardware.
REF_14M_OE_TOGGLE	14	0x0	Reserved for future use. This register controls no hardware.
ON_CHIP_CLOCK_GENERATOR (R)	18	0x0	Reserved for future use. This register controls no hardware. Possible values: 0=External clock 1=Internal clock
SYSCLK_OE_TOGGLE	19	0x0	Reserved for future use. This register controls no hardware.
MEMCLK_OE_TOGGLE	20	0x0	Reserved for future use. This register controls no hardware.

CPLL_CONTROL - RW - 32 bits - clkconfig:0x44			
Field Name	**Bits**	**Default**	**Description**
CPLL_REFSEL	0	0x0	Reserved for future use. This register controls no hardware.
CPLL_REF_DELAY	1	0x0	Reserved for future use. This register controls no hardware.
CPLL_VCO_DELAY	2	0x0	Reserved for future use. This register controls no hardware.
CPLL_SKEW4X	5:3	0x0	Reserved for future use. This register controls no hardware.
CPLL_SKEW2X	8:6	0x0	Reserved for future use. This register controls no hardware.
CPLL_SKEW1X_CORE	11:9	0x0	Reserved for future use. This register controls no hardware.
CPLL_CTL	16:12	0x0	Reserved for future use. This register controls no hardware.
CDLL_FREQ_SEL	20:17	0x0	Reserved for future use. This register controls no hardware.
CPLL_LF_MODE	24:21	0x0	Reserved for future use. This register controls no hardware.
RESERVED	27:25	0x0	Reserved for future use. This register controls no hardware.
CPLL_MODE	31:28	0x0	Reserved for future use. This register controls no hardware.

clk_top_pwm4_ctrl - RW - 32 bits - clkconfig:0x4C			
Field Name	**Bits**	**Default**	**Description**
ct_pwm4_en	0	0x0	Enable PWM function for PWM_GPIO4
ct_pwm4_NumberOfCyclesInPeriod	12:1	0x0	Sets the PWM period in 10ns increments
ct_pwm4_NumberOfHighCyclesInPeriod	24:13	0x0	Sets the number of 10ns increments within the PWM period where the output is high
ct_pwm4_io_oe	25	0x0	Enable PWM_GPIO4 to output in PWM mode

This register is for PWM_GPIO4 PWM functionality

clk_top_pwm5_ctrl - RW - 32 bits - clkconfig:0x50			
Field Name	**Bits**	**Default**	**Description**
ct_pwm5_en	0	0x0	Enable PWM function for PWM_GPIO5
ct_pwm5_NumberOfCyclesInPeriod	12:1	0x0	Sets the PWM period in 10ns increments
ct_pwm5_NumberOfHighCyclesInPeriod	24:13	0x0	Sets the number of 10ns increments within the PWM period where the output is high
ct_pwm5_io_oe	25	0x0	Enable PWM_GPIO5 to output in PWM mode

This register is for PWM_GPIO5 PWM functionality

clk_top_pwm6_ctrl - RW - 32 bits - clkconfig:0x54			
Field Name	**Bits**	**Default**	**Description**
ct_pwm6_en	0	0x0	Enable PWM function for PWM_GPIO6
ct_pwm6_NumberOfCyclesInPeriod	12:1	0x0	Sets the PWM period in 10ns increments
ct_pwm6_NumberOfHighCyclesInPeriod	24:13	0x0	Sets the number of 10ns increments within the PWM period where the output is high
ct_pwm6_io_oe	25	0x0	Enable PWM_GPIO6 to output in PWM mode

This register is for PWM_GPIO6 PWM functionality

MC_CLK_CNTRL - RW - 16 bits - clkconfig:0x58			
Field Name	**Bits**	**Default**	**Description**
MC_CLKSPEED	1:0	0x0	Reserved for future use. This register controls no hardware. Possible values: 0=66 MHz 1=100 MHz 2=133 MHz 3=Undefined
MC_USE_CLKSPEED	2	0x0	Reserved for future use. This register controls no hardware. Possible values: 0=Use fronside bus clk speed 1=Use MC_CLKSPEED value

DELAY_SET_IOC_CCLK - RW - 32 bits - clkconfig:0x5C			
Field Name	**Bits**	**Default**	**Description**
DELAY_SET_ioc_cclk_mst	4:0	0x2	Reserved for future use. This register controls no hardware.
DELAY_SET_ioc_cclk_slv	9:5	0x2	Reserved for future use. This register controls no hardware.

MC_CLK_INDEX - RW - 32 bits - clkconfig:0x60			
Field Name	**Bits**	**Default**	**Description**

MC_CLK_IND_ADDR	17:0	0x0	Bits [17:16] select the memory space being accessed. Write 2'b00 to access MCU RAM memory. Write 2'b01 to access MCU iRAM memory. Write 2'b11 to access MCU Configuration memory. Bits [15:0] are used to select a byte address in each of the three memory spaces.
spare_31_18 (R)	31:18	0x0	

This register is used for writing the address of the micro-controller's (MCU) memory space

MC_CLK_DATA - RW - 32 bits - clkconfig:0x64			
Field Name	**Bits**	**Default**	**Description**
MC_CLK_IND_DATA	31:0	0x0	A write to this register will write 4 bytes beginning at the address MC_CLK_INDEX[15:0] A read from this register will return 4 bytes beginning at the address MC_CLK_INDEX[15:0]

CT_DISABLE_BIU - RW - 32 bits - clkconfig:0x68			
Field Name	**Bits**	**Default**	**Description**
BIU_NB1_CPUSTOP_DIS	0	0x1	Reserved for future use. This register controls no hardware.
BIU_NB2_CPUSTOP_DIS	1	0x1	Reserved for future use. This register controls no hardware.
BIU_CCLK_C3	2	0x1	Reserved for future use. This register controls no hardware.
BIU_MCLK_C3	3	0x1	Reserved for future use. This register controls no hardware.
BIU_CCLK_IO_PAD	4	0x1	Reserved for future use. This register controls no hardware.
SYNC_DBL_FLP_EN	5	0x0	Reserved for future use. This register controls no hardware.
DELAY_SET_gpp_cclk	10:6	0x2	Reserved for future use. This register controls no hardware.
DELAY_SET_gpp_mclk	15:11	0x2	Reserved for future use. This register controls no hardware.
iCFG_CT_DISABLE_BIU_IO_CCLK4X_P	16	0x1	Reserved for future use. This register controls no hardware.
iCFG_CT_DISABLE_BIU_IO_CCLK4X_N	17	0x1	Reserved for future use. This register controls no hardware.

PLL_VOLTAGE_REG_CNTL - RW - 32 bits - clkconfig:0x6C			
Field Name	**Bits**	**Default**	**Description**
NB_RSBEN	0	0x0	Reserved for future use. This register controls no hardware.
NB_REG_OVERRIDE	1	0x0	Reserved for future use. This register controls no hardware.
NB_RBGADJ	7:4	0x8	Reserved for future use. This register controls no hardware.

CPLL_CONTROL3 - RW - 32 bits - clkconfig:0x70			
Field Name	**Bits**	**Default**	**Description**
DLL_BIAS	2:0	0x1	Reserved for future use. This register controls no hardware.
DLL_CPP	4:3	0x0	Reserved for future use. This register controls no hardware.
DLL_CPN	6:5	0x0	Reserved for future use. This register controls no hardware.
VCOREF	8:7	0x0	Reserved for future use. This register controls no hardware.
CALREF	10:9	0x0	Reserved for future use. This register controls no hardware.
SKEW_REF	12:11	0x0	Reserved for future use. This register controls no hardware.
SKEW_FB	14:13	0x0	Reserved for future use. This register controls no hardware.
REF_DELAY	19:15	0x0	Reserved for future use. This register controls no hardware.
FB_DELAY	24:20	0x0	Reserved for future use. This register controls no hardware.
RESERVED	31:25	0x1	Reserved for future use. This register controls no hardware.

GC_CLK_CNTRL - RW - 8 bits - clkconfig:0x74			
Field Name	**Bits**	**Default**	**Description**
CG_BCLKSTATE	0	0x0	Reserved for future use. This register controls no hardware. Possible values: 0=Run 1=Allow GC Shutdown Sequence
GC_STATE (R)	4:3	0x0	Reserved for future use. This register controls no hardware. Possible values: 0=GC has transitioned to D0 1= 2= 3=GC has transitioned to suspend and 61us later all BCLK in the GC will stop
STOP_GC_REQ (R)	5	0x0	Reserved for future use. This register controls no hardware. Possible values: 0=GC has not stopped its clocks 1=GCs clocks will stop within 61us

SCRATCH_1_CLKCFG - RW - 32 bits - clkconfig:0x78			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_1	31:0	0x0	Can write and read to this register but it controls nothing.

Scratch register for the clkconfig register space

SCRATCH_2_CLKCFG - RW - 32 bits - clkconfig:0x7C			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_2	31:0	0x0	Can write and read to this register but it controls nothing.

MC_DATA_DLL_CNTRL_A - RW - 32 bits - clkconfig:0x80			
Field Name	**Bits**	**Default**	**Description**
DLL_DA_IN_TRIM0	3:0	0x0	Reserved for future use. This register controls no hardware.
DLL_DA_OUT_TRIM0	7:4	0x0	Reserved for future use. This register controls no hardware.
DLL_DA_IN_TRIM1	11:8	0x0	Reserved for future use. This register controls no hardware.
DLL_DA_OUT_TRIM1	15:12	0x0	Reserved for future use. This register controls no hardware.
DLL_DA_IN_TRIM2	19:16	0x0	Reserved for future use. This register controls no hardware.
DLL_DA_OUT_TRIM2	23:20	0x0	Reserved for future use. This register controls no hardware.
DLL_DA_IN_TRIM3	27:24	0x0	Reserved for future use. This register controls no hardware.
DLL_DA_OUT_TRIM3	31:28	0x0	Reserved for future use. This register controls no hardware.

SCRATCH_CLKCFG - RW - 32 bits - clkconfig:0x84			
Field Name	**Bits**	**Default**	**Description**
SCRATCH	31:0	0x0	Can write and read to this register, but it controls nothing.
Scratch Register for the CLKCFG register space.			

MC_ACMD_DLL_CNTRL_A - RW - 8 bits - clkconfig:0x88			
Field Name	**Bits**	**Default**	**Description**
DLL_CA_IN_TRIM	3:0	0x0	Reserved for future use. This register controls no hardware.
DLL_CA_OUT_TRIM	7:4	0x0	Reserved for future use. This register controls no hardware.

MC_ACMD_DLL_CNTRL_B - RW - 8 bits - clkconfig:0x89			
Field Name	**Bits**	**Default**	**Description**
DLL_CB_IN_TRIM	3:0	0x0	Reserved for future use. This register controls no hardware.
DLL_CB_OUT_TRIM	7:4	0x0	Reserved for future use. This register controls no hardware.

CLKGATE_DISABLE2 - RW - 32 bits - clkconfig:0x8C			
Field Name	**Bits**	**Default**	**Description**
CLKGATE_DIS_MCB	0	0x1	Reserved for future use. This register controls no hardware.
CLKGATE_DIS_MCGR	1	0x1	Reserved for future use. This register controls no hardware.
CLKGATE_DIS_MCSQA	2	0x1	Reserved for future use. This register controls no hardware.
CLKGATE_DIS_MCSQB	3	0x1	Reserved for future use. This register controls no hardware.
CLKGATE_DIS_MCIOA	4	0x1	Reserved for future use. This register controls no hardware.
CLKGATE_DIS_MCIOB	5	0x1	Reserved for future use. This register controls no hardware.
CLKGATE_DIS_BIU_NB1ACLK	8	0x1	Reserved for future use. This register controls no hardware.
CLKGATE_DIS_BIU_NB1BCLK	9	0x1	Reserved for future use. This register controls no hardware.
CLKDATE_DIS_BIU_MEMA	10	0x1	Reserved for future use. This register controls no hardware.
CLKDATE_DIS_BIU_MEMB	11	0x1	Reserved for future use. This register controls no hardware.
CLKGATE_DIS_BIU_PAD	12	0x1	Reserved for future use. This register controls no hardware.
CLKGATE_DIS_IOC_CCLK_MST	13	0x1	Disable clock gating for LCLK going to IOC master branch
CLKGATE_DIS_IOC_CCLK_SLV	14	0x1	Disable clock gating for LCLK going to IOC slave branch
CLKGATE_DIS_BIU_IOPLL4X	18	0x1	Reserved for future use. This register controls no hardware.
GPP1_SCLK_DISABLE	20	0x0	Reserved for future use. This register controls no hardware.
GPP1_DISPCLK_DISABLE	21	0x0	Reserved for future use. This register controls no hardware.
CFG_CT_DISABLE_MCCLK1X_SVL	22	0x1	Reserved for future use. This register controls no hardware.
CFG_CT_DISABLE_MCCLK1X_M2C	23	0x1	Reserved for future use. This register controls no hardware.
iCFG_CT_DISABLE_CCLK_BIF	24	0x1	Reserved for future use. This register controls no hardware.
CFG_CT_DISABLE_MCLK_BIF	25	0x1	Reserved for future use. This register controls no hardware.
MC_DELAY_TIMER_EXTEND	30	0x0	Reserved for future use. This register controls no hardware.

HOTPLUG_BLINK_RATE - RW - 32 bits - clkconfig:0x90			
Field Name	**Bits**	**Default**	**Description**
HOTPLUG_BLINK_RATE	2:0	0x0	This register controls the blink rate for blinking hot-plug output indicators. 0x0 = 1.00Hz 0x1 = 1.25Hz 0x2 = 1.50Hz 0x3 = 1.75Hz 0x4 = 2.00Hz All other encodings are reserved

CLKGATE_DISABLE - RW - 32 bits - clkconfig:0x94			
Field Name	**Bits**	**Default**	**Description**

CLKGATE_DIS_MCA	0	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
CPUCLK_STOP_MISC	1	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
CLKGATE_DIS_MC1	2	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
CLKGATE_DIS_MC2	3	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
DIS_CPUCLK_STOP_BIU	4	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
SPARE_7	7	0x0	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
ENABLE_ANALOG_DLLs	8	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Disable 1=Enable
CLKGATE_DIS_RAMCLK	9	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
CLKGATE_DIS_BIU_MEM	10	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
CLKGATE_DIS_BIU_NB1CLK	11	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
CLKGATE_DIS_BIU_NB2CLK	12	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
CLKGATE_DIS_PCIE_GPCLK	13	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
CLKGATE_DIS_PCIE_GCLK	14	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
CLKGATE_DIS_PCIE_SBCLK	15	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
CLKGATE_DIS_GPP1_TXCLK	16	0x1	Disable clock gating for PCIE GPP1 dynamic LCLK branch 0=Enable 1=Disable

CLKGATE_DIS_GPP_TXCLK	17	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
CLKGATE_DIS_SB_TXCLK	18	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
CLKGATE_DIS_GPP1_TXCLK_L0S	19	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
CLKGATE_DIS_SB_TXCLK_L0S	20	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
CLKGATE_DIS_GPP3a_TXCLK_L0S	21	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
CLKGATE_DIS_GPP1_CCLK	22	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
CLKGATE_DIS_GPP1_MCLK	23	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
CLKGATE_DIS_GPPSB_CCLK	24	0x1	Disables clock gating for PCIe® Southbridge dynamic LCLK branch. 0=Enable 1=Disable
CLKGATE_DIS_GPPSB_MCLK	25	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
CLKGATE_DIS_CFG_S1X	28	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
CLKGATE_DIS_CFG_B1X	29	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable
DEEP_S1_DISABLE	30	0x1	Reserved for future use. This register controls no hardware. Possibel values: 0=Enable 1=Disable

CPLL_CONTROL2 - RW - 32 bits - clkconfig:0x98			
Field Name	**Bits**	**Default**	**Description**
CPLL_SKEW1XA	2:0	0x0	Reserved for future use. This register controls no hardware.
CPLL_SKEW1XB	5:3	0x0	Reserved for future use. This register controls no hardware.
CPLL_IOBUFSEL	6	0x1	Reserved for future use. This register controls no hardware.
CPLL_SPARE	11:7	0x0	Reserved for future use. This register controls no hardware.
CPLL_FLOAT	16:12	0x0	Reserved for future use. This register controls no hardware.
RESERVED	20:17	0x0	Reserved for future use. This register controls no hardware.
CPLL_CP_RB (R)	24:21	0x0	Reserved for future use. This register controls no hardware.

CPLL_VCO_MODE_RB (R)	26:25	0x0	Reserved for future use. This register controls no hardware.
CPLL_FWDIV_RB (R)	28:27	0x0	Reserved for future use. This register controls no hardware.
STRAP_FREQ_SPEED (R)	31:29	0x0	Reserved for future use. This register controls no hardware.

PCIE_DEVICE_SERIAL_NO_0 - RW - 32 bits - clkconfig:0x9C			
Field Name	**Bits**	**Default**	**Description**
PCIE_DEVICE_SERIAL_NO_0	31:0	0x0	The value in this register is reflected in bits 31:0 of the PCIe® Device Serial Number register located within each PCIe bridge

PCIE_DEVICE_SERIAL_NO_1 - RW - 32 bits - clkconfig:0xA0			
Field Name	**Bits**	**Default**	**Description**
PCIE_DEVICE_SERIAL_NO_1	31:0	0x0	The value in this register is reflected in bits 63:32 of the PCIe Serial Number register located within each PCIe bridge

clk_top_pwm1_ctrl - RW - 32 bits - clkconfig:0xB0			
Field Name	**Bits**	**Default**	**Description**
ct_pwm1_NumberOfCyclesInPeriod	11:0	0x0	Enable PWM function for PWM_GPIO1
ct_pwm1_NumberOfHighCyclesInPeriod	23:12	0x0	Sets the PWM period in 10ns increments
ct_pwm1_en	24	0x0	Sets the number of 10ns increments within the PWM period where the output is high
ct_pwm1_io_oe	25	0x0	Enable PWM_GPIO1 to output in PWM mode
This register is for PWM_GPIO1 PWM functionality			

clk_top_pwm2_ctrl - RW - 32 bits - clkconfig:0xB4			
Field Name	**Bits**	**Default**	**Description**
ct_pwm2_NumberOfCyclesInPeriod	11:0	0x0	Enable PWM function for PWM_GPIO2
ct_pwm2_NumberOfHighCyclesInPeriod	23:12	0x0	Sets the PWM period in 10ns increments
ct_pwm2_en	24	0x0	Sets the number of 10ns increments within the PWM period where the output is high
ct_pwm2_io_oe	25	0x0	Enable PWM_GPIO2 to output in PWM mode
This register is for PWM_GPIO2 PWM functionality			

clk_top_test_ctrl - RW - 32 bits - clkconfig:0xB8			
Field Name	**Bits**	**Default**	**Description**
ct_test_clk_sel	5:0	0x0	Select test clock
ct_test_clk_en	6	0x0	Enable test clock output
ct_test_clk_oe	7	0x0	Reserved for future use. This register controls no hardware
ct_test_clk_spare	31:16	0x0	Reserved for future use. This register controls no hardware
Test clock output control			

NBCLK_IO_CONTROL - RW - 32 bits - clkconfig:0xBC			
Field Name	**Bits**	**Default**	**Description**
SYSCLK_SP	1:0	0x3	Reserved for future use. This register controls no hardware
SYSCLK_SPB	3:2	0x3	Reserved for future use. This register controls no hardware

SYSCLK_SRP	5:4	0x3	Reserved for future use. This register controls no hardware
SYSCLK_SRPB	7:6	0x3	Reserved for future use. This register controls no hardware
SYS_FBCLKOUT_SP	9:8	0x3	Reserved for future use. This register controls no hardware
SYS_FBCLKOUT_SPB	11:10	0x3	Reserved for future use. This register controls no hardware
SYS_FBCLKOUT_SRP	13:12	0x3	Reserved for future use. This register controls no hardware
SYS_FBCLKOUT_SRPB	15:14	0x3	Reserved for future use. This register controls no hardware
IOSPLL_IPWDN	16	0x0	Reserved for future use. This register controls no hardware
IOSPLL_IBYPASS	17	0x0	Reserved for future use. This register controls no hardware
IOSPLL_IREF_DELAY	18	0x0	Reserved for future use. This register controls no hardware
IOSPLL_IVCO_DELAY	19	0x0	Reserved for future use. This register controls no hardware
IOSPLL_IICP	21:20	0x1	Reserved for future use. This register controls no hardware
IOSPLL_ICPBW	22	0x0	Reserved for future use. This register controls no hardware
IOSPLL_IVCOBW	23	0x0	Reserved for future use. This register controls no hardware
IOSPLL_ISKEW_4X	24	0x0	Reserved for future use. This register controls no hardware
IOSPLL_IPLL_CNTL	31:28	0x0	Reserved for future use. This register controls no hardware

CLK_TOP_THERMAL_ALERT_INTR_EN - RW - 32 bits - clkconfig:0xC0			
Field Name	**Bits**	**Default**	**Description**
THERMAL_ALERT_INTR_EN	0	0x0	Reserved for future use. This register controls no hardware
spare_1_31	31:1	0x0	Reserved for future use. This register controls no hardware

CLK_TOP_THERMAL_ALERT_STATUS - RW - 32 bits - clkconfig:0xC4			
Field Name	**Bits**	**Default**	**Description**
THERMAL_ALERT_STATUS	0	0x0	Reserved for future use. This register controls no hardware
spare_1_31	31:1	0x0	Reserved for future use. This register controls no hardware

CLK_TOP_THERMAL_ALERT_WAIT_WINDOW - RW - 32 bits - clkconfig:0xC8			
Field Name	**Bits**	**Default**	**Description**
THERMAL_ALERT_WAIT_WINDOW	29:0	0x0	Reserved for future use. This register controls no hardware
spare_30_31	31:30	0x0	Reserved for future use. This register controls no hardware

clk_top_pwm3_ctrl - RW - 32 bits - clkconfig:0xCC			
Field Name	**Bits**	**Default**	**Description**
ct_pwm3_en	0	0x0	Enable PWM function for PWM_GPIO3
ct_pwm3_NumberOfCyclesInPeriod	12:1	0x0	Sets the PWM period in 10ns increments
ct_pwm3_NumberOfHighCyclesInPeriod	24:13	0x0	Sets the number of 10ns increments within the PWM period where the output is high
ct_pwm3_io_oe	25	0x0	Enable PWM_GPIO3 to output in PWM mode
This register is for PWM_GPIO3 PWM functionality			

clk_top_spare_pll - RW - 32 bits - clkconfig:0xD0			
Field Name	**Bits**	**Default**	**Description**
ct_spare_pll_ctl	31:0	0x0	Reserved for future use. This register controls no hardware.

CLK_CFG_HTPLL_CNTL - RW - 32 bits - clkconfig:0xD4			
Field Name	**Bits**	**Default**	**Description**
CLK_CFG_HTPLL_IPCP	2:0	0x4	Reserved for future use. This register controls no hardware.
CLK_CFG_HTPLL_IDB1CLK0SC	5:3	0x5	Reserved for future use. This register controls no hardware.
CLK_CFG_HTPLL_IDB1CLK3SC	8:6	0x5	Reserved for future use. This register controls no hardware.
CLK_CFG_HTPLL_IDB4CLKSC	11:9	0x5	Reserved for future use. This register controls no hardware.
CLK_CFG_HTPLL_ITXCLKSC	14:12	0x7	Reserved for future use. This register controls no hardware.
CLK_CFG_HTPLL_IVCO_MODE	16:15	0x0	Reserved for future use. This register controls no hardware.
CLK_CFG_HTPLL_IPLL_CTL	21:17	0x0	Reserved for future use. This register controls no hardware.
CLK_CFG_HTPLL_ITMONEN	22	0x0	Reserved for future use. This register controls no hardware.
CLK_CFG_HTPLL_PWDN	23	0x0	Reserved for future use. This register controls no hardware.
iCFG_HT_HTPLL_ITXCLKINV	24	0x0	Reserved for future use. This register controls no hardware.
iCFG_HT_HTPLL_ICLK0SEL	25	0x0	Reserved for future use. This register controls no hardware.
iCFG_HT_HTPLL_ICLK3SEL	26	0x0	Reserved for future use. This register controls no hardware.
iCFG_HT_HTPLL_IVCOREF	28:27	0x0	Reserved for future use. This register controls no hardware.
iCFG_HT_HTPLL_ICALREF	30:29	0x0	Reserved for future use. This register controls no hardware.
iCFG_HT_HTPLL_ITSTCLK	31	0x0	Reserved for future use. This register controls no hardware.

CLK_HTPLL_CONTROL - RW - 32 bits - clkconfig:0xD8			
Field Name	**Bits**	**Default**	**Description**
htpll_control	31:0	0x54	Bits 9:0 - HTPLL_IBIAS Bit 10 - HTPLL_IBIAS_SEL Bits 12:11 - HTPLL_IBIAS_RD Bit 15 - Enable LCLK 2X mode Bits 31:16 - HTPLL_BACKUP

GPIO_ctrl - RW - 32 bits - clkconfig:0xDC			
Field Name	**Bits**	**Default**	**Description**
GPIO_1_OE	0	0x0	PCIE_RESET_GPIO1 pad output enable when GPIO17_OR is clear 1 - Output driver enabled 0 - Output driver disabled
GPIO_1_A	1	0x0	Indicates the input state of the PCIE_RESET_GPIO1 pad
GPIO_1_Y	2	0x0	PCIE_RESET_GPIO1 pad output value when GPIO17_OR is clear 1 - Drive logic 1 0 - Drive logic 0
GPIO_2_OE	4	0x0	PCIE_RESET_GPIO2 pad output enable when GPIO18_OR is clear 1 - Output driver enabled 0 - Output driver disabled
GPIO_2_A	5	0x0	Indicates the input state of the PCIE_RESET_GPIO2 pad
GPIO_2_Y	6	0x0	PCIE_RESET_GPIO2 pad output value when GPIO18_OR is clear 1 - Drive logic 1 0 - Drive logic 0
GPIO_3_OE	8	0x0	PCIE_RESET_GPIO3 pad output enable when GPIO19_OR is clear 1 - Output driver enabled 0 - Output driver disabled
GPIO_3_A	9	0x0	Indicates the input state of the PCIE_RESET_GPIO3 pad
GPIO_3_Y	10	0x0	PCIE_RESET_GPIO3 pad output value when GPIO19_OR is clear 1 - Drive logic 1 0 - Drive logic 0

GPIO_4_OE	12	0x0	PCIE_RESET_GPIO4 pad output enable when GPIO20_OR is clear 1 - Output driver enabled 0 - Output driver disabled
GPIO_4_A	13	0x0	Indicates the input state of the PCIE_RESET_GPIO4 pad
GPIO_4_Y	14	0x0	PCIE_RESET_GPIO4 pad output value when GPIO20_OR is clear 1 - Drive logic 1 0 - Drive logic 0
GPIO_5_OE	16	0x0	PCIE_RESET_GPIO5 pad output enable when GPIO21_OR is clear 1 - Output driver enabled 0 - Output driver disabled
GPIO_5_A	17	0x0	Indicates the input state of the PCIE_RESET_GPIO5 pad
GPIO_5_Y	18	0x0	PCIE_RESET_GPIO5 pad output value when GPIO21_OR is clear 1 - Drive logic 1 0 - Drive logic 0

PCIe Reset 1 to 5

CLK_TOP_SPARE_A - RW - 32 bits - clkconfig:0xE0			
Field Name	**Bits**	**Default**	**Description**
MCLK_SWITCH_GPP1_EN	0	0x0	After straps are finished loading, STRP_DATA is overrriden to drive 1'b0 until this bit is set to '1'. After that STRP_DATA can be used for any of its other purposes (PWM, GPIO, etc.)
spare_7_1	7:1	0x0	Bits 1 to 3 and 5 to 7 are reserved for future use and control no hardware. Bit 4 - Setting this register bit will freeze the HyperTransport host access interface going into the IOC. This register is intended to be set via JTAG or MCU only and may be used to help create atomic operations to indirect register spaces.
CFG_B1X_CPUSTOP_DIS	8	0x0	Reserved for future use. This register controls no hardware
CFG_S1X_CPUSTOP_DIS	9	0x0	Reserved for future use. This register controls no hardware
spare_15_10	15:10	0x0	
OSC_PU	16	0x1	PU setting for OSC pad output
OSC_PD	17	0x0	PD setting for OSC pad output
OSC_SRP	18	0x1	SRP setting for OSC pad output
OSC_SRN	19	0x1	SRN setting for OSC pad output
OSC_SP	23:20	0x4	SP setting for OSC pad output
OSC_SN	27:24	0x7	SN setting for OSC pad output
spare_31_28	31:28	0x0	Register bits to force off dynamic LCLK branches for PCIe® Bit 28 - LCLK_GPP1 Bit 29 - LCLK_GPP2 Bit 30 - LCLK_GPP3a Bit 31 - LCLK_GPP3b

CLK_TOP_SPARE_B - RW - 32 bits - clkconfig:0xE4			
Field Name	**Bits**	**Default**	**Description**
CLK_TOP_SPAREB	31:0	0x0	Reserved for future use. This register controls no hardware

CLK_TOP_SPARE_C - RW - 32 bits - clkconfig:0xE8			
Field Name	**Bits**	**Default**	**Description**

CLK_TOP_SPAREC	31:0	0x0	Bit 0 = Extend IOC PM timer Bits 1->7 Reserved for future use. This register controls no hardware Bit 8 = HTPLL_CTRL_VCTRLADC_EN Bit 9 = HTPLL_CTRL_LOCK_DETECT Bit 10 = HTPLL_CTRL_ENSAT Bit 11 = HTPLL_CTRL_FASTEN Bits 15:12 = HTPLL_CTRL_CVTRLADC Bit 25 = Enable clock gating for PCIE GPP3b dynamic LCLK branch Bit 26 = Enable clock gating for MCU 2nd dynamic LCLK branch Bit 27 = Enable clock gating for MCU dynamic LCLK branch Bit 28 = Enable clock gating for PCIE GPP2 dynamic LCLK branch Bit 29 = Enable clock gating for CFG 2nd dynamic LCLK branch Bit 30 = Enable clock gating for CFG dynamic LCLK branch Bit 31 = Enable clock gating for PCIE GPP3a dynamic LCLK branch

CLK_TOP_SPARE_D - RW - 32 bits - clkconfig:0xEC			
Field Name	**Bits**	**Default**	**Description**
CLK_TOP_SPARED (R)	31:0	0x0	Reserved for future use. This register controls no hardware

HOTPLUG_SPARE_0 - RW - 32 bits - clkconfig:0xF0			
Field Name	**Bits**	**Default**	**Description**
HOTPLUG_SPARE_0	31:0	0x0	This register is used to set the mapping between hot-plug I2C expanders and PCI Express bridges. See the programming guide for more details.

HOTPLUG_SPARE_1 - RW - 32 bits - clkconfig:0xF4			
Field Name	**Bits**	**Default**	**Description**
HOTPLUG_SPARE_1	31:0	0x0	This register is used to set the mapping between hot-plug I2C expanders and PCI Express bridges. See the programming guide for more details.

CFG_CT_CLKGATE_HTIU - RW - 32 bits - clkconfig:0xF8			
Field Name	**Bits**	**Default**	**Description**
DISABLE_CLKGATE_HTIU_LCLK_HTM	0	0x1	Disables clock gating on the htiu htm clock branch during HT link disconnection. This register should always be set to 1.
DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_HTM	1	0x1	Disables dynamic clock gating on the htiu htm clock branch.
DISABLE_CLKGATE_HTIU_LCLK_RP	2	0x1	Disables clock gating on the htiu rp clock branch during HT link disconnection. This register should always be set to 1.
DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_RP	3	0x1	Disables dynamic clock gating on the htiu rp clock branch.
DISABLE_CLKGATE_HTIU_LCLK_FCB	4	0x1	Disables clock gating on the htiu fcb clock branch during HT link disconnection. This register should always be set to 1.
DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_FCB	5	0x1	Disables dynamic clock gating on the htiu gcb clock branch.

DISABLE_CLKGATE_HTIU_LCLK_GCM	6	0x1	Disables clock gating on the htiu gcm clock branch during HT link disconnection. This register should always be set to 1.
DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_GCM	7	0x1	Disables dynamic clock gating on the htiu gcm clock branch.
DISABLE_CLKGATE_HTIU_LCLK_NB1	8	0x1	Disables clock gating on the htiu nb1 clock branch during HT link disconnection. This register should always be set to 1.
DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_NB1	9	0x1	Disables dynamic clock gating on the htiu nb1 clock branch.
DISABLE_CLKGATE_HTIU_LCLK_NB2	10	0x1	Disables clock gating on the htiu nb2 clock branch during HT link disconnection. This register should always be set to 1.
DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_NB2	11	0x1	Disables dynamic clock gating on the htiu nb2 clock branch.
ILF_MODE	13:12	0x0	Reserved for future use. This register controls no hardware

2.3 I/O Space Registers

2.3.1 PMM2REG Registers

PM2_CNTRL - RW - 32 bits - pmm2reg:0x0			
Field Name	**Bits**	**Default**	**Description**
ARB_DISABLE	0	0x0	Arbiter Disable: 0=System Arbiter enabled; arbiter can grant other bus masters in the system. 1=System Arbiter disabled and the Boot Processor has ownership of the system bus. 0=Enabled 1=Disabled
Power Control 2 Register - Required for ACPI Specification			

PM1_STATUS - RW - 32 bits - pmm2reg:0x4			
Field Name	**Bits**	**Default**	**Description**
BM_STS	4	0x0	Bus master status: 0=No bus busmaster event 1=Bus master event detect Write 1 to this bit to clear it. Write 0 has no effect.
Power Control 1 Register - Required for ACPI Specification			

2.4 Memory Mapped Space Registers

2.4.1 IOMMUMMREG Registers

IOMMU_MMIO_DEVTBL_BASE_0 - RW - 32 bits - iommummreg:0x0			
Field Name	**Bits**	**Default**	**Description**
DEV_TBL_SIZE	8:0	0x0	This field contains 1 less than the length of the device table, in multiples of 4K bytes. A minimum size of 0 corresponds to a 4K byte device table and a maximum size of 1FFh corresponds to a 2M byte device table.
Reserved1 (R)	11:9	0x0	Reserved for future use. This register controls no hardware
DEV_TBL_BASE_LO	31:12	0x0	Specifies address bits [31:12] of the 4Kbyte-aligned base address of the first level device table.

IOMMU_MMIO_DEVTBL_BASE_1 - RW - 32 bits - iommummreg:0x4			
Field Name	**Bits**	**Default**	**Description**
DEV_TBL_BASE_HI	19:0	0x0	Specifies address bits [51:32] of the 4Kbyte-aligned base address of the first level device table.
Reserved0 (R)	31:20	0x0	Reserved for future use. This register controls no hardware

IOMMU_MMIO_CMD_BASE_0 - RW - 32 bits - iommummreg:0x8			
Field Name	**Bits**	**Default**	**Description**
Reserved1 (R)	11:0	0x0	Reserved for future use. This register controls no hardware
COM_BASE_LO	31:12	0x0	Specifies address bits [31:12] of the base address of the command buffer. The base address programmed must be aligned to 4K bytes.

IOMMU_MMIO_CMD_BASE_1 - RW - 32 bits - iommummreg:0xC			
Field Name	**Bits**	**Default**	**Description**
COM_BASE_HI	19:0	0x0	Specifies address bits [51:32] of the base address of the command buffer. The base address programmed must be aligned to 4K bytes.
Reserved1 (R)	23:20	0x0	Reserved for future use. This register controls no hardware
COM_LEN	27:24	0x8	Specifies the length of the command buffer in power of 2 increments. The minimum size is 256 entries (4K bytes); values less than 1000b are reserved. 0000b - 0111b=Reserved 1000b=256 entries (4K bytes) 1001b=512 entries (8K bytes) ... 1111b=32768 entries (512K bytes)
Reserved0 (R)	31:28	0x0	Reserved for future use. This register controls no hardware

IOMMU_MMIO_EVENT_BASE_0 - RW - 32 bits - iommummreg:0x10			
Field Name	**Bits**	**Default**	**Description**
Reserved1 (R)	11:0	0x0	Reserved for future use. This register controls no hardware
EVENT_BASE_LO	31:12	0x0	Specifies address bits [31:12] of the base address of the event log. The base address programmed must be aligned to 4K bytes.

IOMMU_MMIO_EVENT_BASE_1 - RW - 32 bits - iommummreg:0x14			
Field Name	**Bits**	**Default**	**Description**
EVENT_BASE_HI	19:0	0x0	Specifies address bits [51:32] of the base address of the event log. The base address programmed must be aligned to 4K bytes.
Reserved1 (R)	23:20	0x0	Reserved for future use. This register controls no hardware
EVENT_LEN	27:24	0x8	Specifies the length of the event log in power of 2 increments. The minimum size is 256 entries (4K bytes); values less than 1000b are reserved. 0000b - 0111b=Reserved 1000b=256 entries (4K bytes) 1001b=512 entries (8K bytes) ... 1111b=32768 entries (512K bytes)
Reserved0 (R)	31:28	0x0	Reserved for future use. This register controls no hardware

IOMMU_MMIO_CNTRL_0 - RW - 32 bits - iommummreg:0x18			
Field Name	**Bits**	**Default**	**Description**
IOMMU_EN	0	0x0	1=IOMMU enabled. All upstream transactions are translated by the IOMMU. The Device Table Base Address Register [MMIO Offset 0000h] must be configured by software before setting this bit. 0=IOMMU is disabled and no upstream transactions are translated or remapped by the IOMMU. When disabled, the IOMMU reads no commands and creates no event log entries. Note: Software must configure EventLogEn and CmdBufEn.
HT_TUN_EN	1	0x0	1= Upstream traffic received by the HyperTransport™ tunnel is translated by the IOMMU. 0=Upstream traffic received by the HyperTransport tunnel is not translated by the IOMMU. The IOMMU ignores the state of this bit while IommuEn=0. See also the HtTunnel bit in the IOMMU Capability Header [Capability Offset 00h].

EVENT_LOG_EN	2	0x0	1=The Event Log Base Address Register [MMIO Offset 0010h] has been configured and all events detected are written to the event log when IommuEn has also been set. Writing a 1b to this bit when EventLogEn=1b has no effect. 0=Event logging is not enabled. Events are discarded when the event log is not enabled. When IommuEn=1b and software writes EventLogEn with 1b, the IOMMU clears the EventOverflow bit, and sets the EventLogRun bit in the IOMMU Status Register [MMIO Offset 2020h]. The IOMMU can now write new entries to the event log if there are usable entries available. Note: Software can read MMIO Offset 2020h[EventLogRun] to determine the status of event log writing by the IOMMU. Note: the fetching of command is independently controlled by CmdBufEn. Software note: The Event Log Base Address Register [MMIO Offset 0010h], the Event Log Head Pointer Register [MMIO Offset 2010h], and the Event Log Tail Pointer Register [MMIO Offset 2018h] must be set prior to enabling the event log.
EVENT_INT_EN	3	0x0	1=An interrupt is signalled when the EventLogInt bit is set in the IOMMU Status Register [MMIO Offset 2020h].
COM_WAIT_INTEN	4	0x0	1=An interrupt is signalled when MMIO Offset 2020h[ComWaitInt]=1.
INV_TIMEOUT	7:5	0x0	This field specifies the invalidation time-out for IOTLB invalidation requests. 000b=No time-out 001b=1 ms 010b=10 ms 011b=100 ms 100b=1 sec. 101b=10 sec. 110b 111b=Reserved
PASS_PW	8	0x0	This bit controls the state of the PassPW bit in the HyperTransport read request packet when the IOMMU issues I/O page table reads and device table reads on the HyperTransport link. 1=Request packet may pass posted requests. 0=Request packet may not pass posted requests.
RES_PASS_PW	9	0x0	This bit controls the state of the ResPassPW bit in the HyperTransport read request packet when the IOMMU issues I/O page table reads and device table reads on the HyperTransport link. 1=Response may pass posted requests. 0=Response may not pass posted requests.
COHERENT	10	0x1	This bit controls the state of the coherent bit in the HyperTransport read request packet when the IOMMU issues device table reads on the HyperTransport link. 1=Device table requests are snooped by the processor. 0=Device table requests are not snooped by the processor.
ISOC	11	0x0	This bit controls the state of the isochronous bit in the HyperTransport read request packet when the IOMMU issues I/O page table reads and device table reads on the HyperTransport link. 1=Request packet to use isochronous channel. 0=Request packet to use standard channel. Note: Platform firmware should set this bit to 1b for processors that support the isochronous channel.

CMD_BUF_EN	12	0x0	1=Start or restart command buffer processing. When CmdBufEn=1b and IommuEn=1b, the IOMMU starts fetching commands and sets MMIO Offset 2020h[CmdBufRun] to 1b. Writing a 1b to this bit when CmdBufRun=1b has no effect. 0=Halt command buffer processing. Writing a 0 to this bit causes the IOMMU to cease fetching new commands although commands previously fetched are completed. The IOMMU stops fetching commands upon reset and after errors as specified in Table 11. See also MMIO Offset 2020h[CmdBufRun]. Note: See IOMMU Status Register [MMIO Offset 2020h] to determine the status of command buffer processing. Note: Writing of event log entries is independently controlled by EventLogEn. Software note: The Command Buffer Base Address Register [MMIO Offset 0008h], the Command Buffer Head Pointer Register [MMIO Offset 2000h], and the Command Buffer Tail Pointer Register [MMIO Offset 2008h] must be set prior to enabling the IOMMU command buffer processor.
Reserved0 (R)	31:13	0x0	Reserved for future use. This register controls no hardware

IOMMU_MMIO_CNTRL_1 - RW - 32 bits - iommummreg:0x1C			
Field Name	**Bits**	**Default**	**Description**
Reserved0 (R)	31:0	0x0	Reserved for future use. This register controls no hardware

IOMMU_MMIO_EXCL_BASE_0 - RW - 32 bits - iommummreg:0x20			
Field Name	**Bits**	**Default**	**Description**
EX_EN	0	0x0	1=The exclusion range is enabled. 0=The exclusion range is disabled.
EX_ALLOW	1	0x0	1=All accesses to the exclusion range are forwarded untranslated. 0=The EX bit in the device table entry specifies if accesses to the exclusion range are translated.
Reserved0 (R)	11:2	0x0	Reserved for future use. This register controls no hardware
EXCL_BASE_LO	31:12	0x0	Specifies address bits [31:12] of the 4Kbyte-aligned base address of the exclusion range.

IOMMU_MMIO_EXCL_BASE_1 - RW - 32 bits - iommummreg:0x24			
Field Name	**Bits**	**Default**	**Description**
EXCL_BASE_HI	19:0	0x0	Specifies address bits [51:32] of the 4Kbyte-aligned base address of the exclusion range.
Reserved0 (R)	31:20	0x0	Reserved for future use. This register controls no hardware

IOMMU_MMIO_EXCL_LIM_0 - RW - 32 bits - iommummreg:0x28			
Field Name	**Bits**	**Default**	**Description**
Reserved0 (R)	11:0	0x0	Reserved for future use. This register controls no hardware
EXCL_LIMIT_LO	31:12	0x0	Specifies address bits [31:12] of the 4K byte limit of the exclusion range

IOMMU_MMIO_EXCL_LIM_1 - RW - 32 bits - iommummreg:0x2C			
Field Name	**Bits**	**Default**	**Description**
EXCL_LIMIT_HI	19:0	0x0	Specifies address bits [63:32] of the 4K byte limit of the exclusion range
Reserved0 (R)	31:20	0x0	Reserved for future use. This register controls no hardware

IOMMU_MMIO_CMD_BUF_HDPTR_0 - RW - 32 bits - iommummreg:0x2000			
Field Name	**Bits**	**Default**	**Description**
Reserved0 (R)	3:0	0x0	Reserved for future use. This register controls no hardware
CMD_HDPTR	18:4	0x0	Specifies the 128-bit aligned offset from the command buffer base address register of the next command to be fetched by the IOMMU. The IOMMU increments this register, rolling over to zero at the end of the buffer, after fetching and validating the command in the command buffer. After incrementing this register, the IOMMU cannot re-fetch the command from the buffer. If this register is written to by software while CmdBufRun=1b, the IOMMU behavior is undefined. If this register is set by software to a value outside the length specified by MMIO Offset 0008h[ComLen], the IOMMU behavior is undefined.
Reserved1 (R)	31:19	0x0	Reserved for future use. This register controls no hardware

IOMMU_MMIO_CMD_BUF_HDPTR_1 - RW - 32 bits - iommummreg:0x2004			
Field Name	**Bits**	**Default**	**Description**
Reserved0 (R)	31:0	0x0	Reserved for future use. This register controls no hardware

IOMMU_MMIO_CMD_BUF_TAILPTR_0 - RW - 32 bits - iommummreg:0x2008			
Field Name	**Bits**	**Default**	**Description**
Reserved0 (R)	3:0	0x0	Reserved for future use. This register controls no hardware

CMD_TAILPTR	18:4	0x0	Specifies the 128-bit aligned offset from the command buffer base address register of the next command to be written by the software. Software must increment this field, rolling over to zero at the end of the buffer, after writing a command to the command buffer. If software advances the tail pointer equal to or beyond the head pointer after adding one or more commands to the buffer, the IOMMU behavior is undefined. If software sets the command buffer tail pointer to an offset beyond the length of the command buffer, the IOMMU behavior is undefined.
Reserved1 (R)	31:19	0x0	Reserved for future use. This register controls no hardware

IOMMU_MMIO_CMD_BUF_TAILPTR_1 - RW - 32 bits - iommummreg:0x200C			
Field Name	**Bits**	**Default**	**Description**
Reserved0 (R)	31:0	0x0	Reserved for future use. This register controls no hardware

IOMMU_MMIO_EVENT_BUF_HDPTR_0 - RW - 32 bits - iommummreg:0x2010			
Field Name	**Bits**	**Default**	**Description**
Reserved0 (R)	3:0	0x0	Reserved for future use. This register controls no hardware
EVENT_HDPTR	18:4	0x0	Specifies the 128 bit aligned offset from the event log base address register that will be read next by software. Software must increment this field, rolling over at the end of the buffer, after reading an event from the event log. If software advances the head pointer beyond the tail pointer, the IOMMU behavior is undefined. If software sets the event log head pointer to an offset beyond the length of the event log, the IOMMU behavior is undefined.
Reserved1 (R)	31:19	0x0	Reserved for future use. This register controls no hardware

IOMMU_MMIO_EVENT_BUF_HDPTR_1 - RW - 32 bits - iommummreg:0x2014			
Field Name	**Bits**	**Default**	**Description**
Reserved0 (R)	31:0	0x0	Reserved for future use. This register controls no hardware

IOMMU_MMIO_EVENT_BUF_TAILPTR_0 - RW - 32 bits - iommummreg:0x2018			
Field Name	**Bits**	**Default**	**Description**
Reserved0 (R)	3:0	0x0	Reserved for future use. This register controls no hardware
EVENT_TAILPTR	18:4	0x0	Specifies the 128-bit aligned offset from the event log base address register that will be written next by the IOMMU when an event is detected. The IOMMU increments this register, rolling over at the end of the buffer, after writing an event to the event log. If this register is written while EventLogRun=1, the IOMMU behavior is undefined. If this register is set by software to a value outside the length specified by MMIO Offset 0010h[EventLen], the IOMMU behavior is undefined.
Reserved1 (R)	31:19	0x0	Reserved for future use. This register controls no hardware

IOMMU_MMIO_EVENT_BUF_TAILPTR_1 - RW - 32 bits - iommummreg:0x201C			
Field Name	**Bits**	**Default**	**Description**
Reserved0 (R)	31:0	0x0	Reserved for future use. This register controls no hardware

IOMMU_MMIO_STATUS_0 - RW - 32 bits - iommummreg:0x2020			
Field Name	**Bits**	**Default**	**Description**
EVENT_OVERFLOW	0	0x0	1=IOMMU event log overflow has occurred. This bit is set when a new event is to be written to the event log and there is no usable entry in the event log, causing the new event information to be discarded. An interrupt is generated when EventOverflow=1b and MMIO Offset 0018h[EventIntEn]=1b. No new event log entries are written while this bit is set.
EVENT_LOGINT	1	0x0	1=Event entry written to the event log by the IOMMU 0=No event entry written to the event log by the IOMMU. An interrupt is generated when EventLogInt=1b and MMIO Offset 0018h[EventIntEn]=1b.
COMWAIT_INT	2	0x0	1=COMPLETION_WAIT command completed. This bit is only set if the i bit is set in the COMPLETION_WAIT command. An interrupt is generated when ComWaitInt=1b and MMIO Offset 0018h[ComWaitIntEn]=1b.
EVENT_LOGRUN (R)	3	0x0	1=Events are logged as they occur. 0=Event reports are discarded without logging. When EventOverflow=1b, the IOMMU does not write new event log entries even when EventLogRun=1b. When halted, event logging is restarted by using MMIO Offset 0018h[EventLogEn].
CMD_BUFRUN (R)	4	0x0	1=Commands may be fetched from the command buffer. 0=IOMMU has stopped fetching new commands. The IOMMU freezes command processing after COMMAND_HARDWARE_ERROR or ILLEGAL_COMMAND_ERROR errors. When frozen, command fetching is restarted by using MMIO Offset 0018h[CmdBufEn].
Reserved1 (R)	31:5	0x0	Reserved for future use. This register controls no hardware

IOMMU_MMIO_STATUS_1 - RW - 32 bits - iommummreg:0x2024			
Field Name	**Bits**	**Default**	**Description**
Reserved0 (R)	31:0	0x0	Reserved for future use. This register controls no hardware

2.4.2 IOAPICMMREG Registers

IO_REGISTER_SELECT_INDEX - RW - 32 bits - ioapicmmreg:0x0			
Field Name	**Bits**	**Default**	**Description**
Indirect_Address_Offset	7:0	0x0	Register to select which indirect register has to be written

IO_WINDOW_REGISTER_DATA - RW - 32 bits - ioapicmmreg:0x10			
Field Name	**Bits**	**Default**	**Description**
Window	31:0	0x0	Data meant for indirect registers

IRQ_PIN_ASSERTION_REGISTER - RW - 32 bits - ioapicmmreg:0x20			
Field Name	**Bits**	**Default**	**Description**
Input_IRQ	7:0	0x0	This register will trigger an interrup associated with redirection entry table

EOI_REGISTER - W - 32 bits - ioapicmmreg:0x40			
Field Name	**Bits**	**Default**	**Description**
Vector	7:0	0x0	This register will clear the remote IRR bit in the redirection table entry for the corresponding interrupt vector

2.5 Indirect Space Registers

2.5.1 IOAPICCMISCIND Registers

FEATURES_ENABLE - RW - 32 bits - IOAPICCMISCIND:0x0			
Field Name	**Bits**	**Default**	**Description**
Ioapic_enable	0	0x0	This bit enables the IOAPIC
Ioapic_entries	1	0x0	This bit selects the 24 or 32 interrupt mode, 0 = 24, 1 = 32
Ioapic_id_ext_en	2	0x0	Extend id 4 or 8
Ioapic_c2wake_en	3	0x0	Setting this bit to 1 will send a wake pulse to IOC, each time an interrupt is sent
Ioapic_sb_feature_en	4	0x0	Setting this bit to 1 will send the masked interrupts back to IOC
Reserved (R)	31:5	0x0	

IOAPIC_CONF_LOWER - RW - 32 bits - IOAPICCMISCIND:0x1			
Field Name	**Bits**	**Default**	**Description**
Reserved (R)	2:0	0x0	
Mem_IO_Map	3	0x0	1 = memory map or 0 = IO map
Reserved1 (R)	7:4	0x0	
IOAPIC_Addr	31:8	0xfec000	Base address for IOAPIC bits 31 to 8, default to FEC000xx

IOAPIC_CONF_UPPER - RW - 32 bits - IOAPICCMISCIND:0x2			
Field Name	**Bits**	**Default**	**Description**
IOAPIC_Addr_Upper	31:0	0x0	Bits 63:32 of the IOAPIC base address

IOAPIC_INT_ROUTING_REGISTER1 - RW - 32 bits - IOAPICCMISCIND:0x3			
Field Name	**Bits**	**Default**	**Description**
D2ext_Intr_grp	2:0	0x0	MAP D2 external INT A/B/C/D to IOAPIC table/pins, if 32 interrupts then 0-7, if 24 interrupts then 0-5
Reserved (R)	3	0x0	
D2ext_Intr_swz	5:4	0x0	Swizzle D2 external INT A/B/C/D before maping to IOAPIC table/pins, 0=ABCD, 1=BCDA, 2=CDAB, 3=DABC
Reserved1 (R)	7:6	0x0	
D3ext_Intr_grp	10:8	0x0	MAP D3 external INT A/B/C/D to IOAPIC table/pins, if 32 interrupts then 0-7, if 24 interrupts then 0-5
Reserved2 (R)	11	0x0	
D3ext_Intr_swz	13:12	0x0	Swizzle D3 external INT A/B/C/D before maping to IOAPIC table/pins, 0=ABCD, 1=BCDA, 2=CDAB, 3=DABC
Reserved3 (R)	15:14	0x0	
D4ext_Intr_grp	18:16	0x0	MAP D4 external INT A/B/C/D to IOAPIC table/pins, if 32 interrupts then 0-7, if 24 interrupts then 0-5
Reserved4 (R)	19	0x0	
D4ext_Intr_swz	21:20	0x0	Swizzle D4 external INT A/B/C/D before maping to IOAPIC table/pins, 0=ABCD, 1=BCDA, 2=CDAB, 3=DABC
Reserved5 (R)	23:22	0x0	
D5ext_Intr_grp	26:24	0x0	MAP D5 external INT A/B/C/D to IOAPIC table/pins, if 32 interrupts then 0-7, if 24 interrupts then 0-5
Reserved6 (R)	27	0x0	

D5ext_Intr_swz	29:28	0x0	Swizzle D5 external INT A/B/C/D before maping to IOAPIC table/pins, 0=ABCD, 1=BCDA, 2=CDAB, 3=DABC
Reserved7 (R)	31:30	0x0	

IOAPIC_INT_ROUTING_REGISTER2 - RW - 32 bits - IOAPICCMISCIND:0x4			
Field Name	**Bits**	**Default**	**Description**
D6ext_Intr_grp	2:0	0x0	MAP D6 external INT A/B/C/D to IOAPIC table/pins, if 32 interrupts then 0-7, if 24 interrupts then 0-5
Reserved (R)	3	0x0	
D6ext_Intr_swz	5:4	0x0	Swizzle D6 external INT A/B/C/D before maping to IOAPIC table/pins, 0=ABCD, 1=BCDA, 2=CDAB, 3=DABC
Reserved1 (R)	7:6	0x0	
D7ext_Intr_grp	10:8	0x0	MAP D7 external INT A/B/C/D to IOAPIC table/pins, if 32 interrupts then 0-7, if 24 interrupts then 0-5
Reserved2 (R)	11	0x0	
D7ext_Intr_swz	13:12	0x0	Swizzle D7 external INT A/B/C/D before maping to IOAPIC table/pins, 0=ABCD, 1=BCDA, 2=CDAB, 3=DABC
Reserved3 (R)	15:14	0x0	
D9ext_Intr_grp	18:16	0x0	MAP D9 external INT A/B/C/D to IOAPIC table/pins, if 32 interrupts then 0-7, if 24 interrupts then 0-5
Reserved4 (R)	19	0x0	
D9ext_Intr_swz	21:20	0x0	Swizzle D9 external INT A/B/C/D before maping to IOAPIC table/pins, 0=ABCD, 1=BCDA, 2=CDAB, 3=DABC
Reserved5 (R)	23:22	0x0	
D10ext_Intr_grp	26:24	0x0	MAP D10 external INT A/B/C/D to IOAPIC table/pins, if 32 interrupts then 0-7, if 24 interrupts then 0-5
Reserved6 (R)	27	0x0	
D10ext_Intr_swz	29:28	0x0	Swizzle D10 external INT A/B/C/D before maping to IOAPIC table/pins, 0=ABCD, 1=BCDA, 2=CDAB, 3=DABC
Reserved7 (R)	31:30	0x0	

IOAPIC_INT_ROUTING_REGISTER3 - RW - 32 bits - IOAPICCMISCIND:0x5			
Field Name	**Bits**	**Default**	**Description**
D11ext_Intr_grp	2:0	0x0	MAP D11 external INT A/B/C/D to IOAPIC table/pins, if 32 interrupts then 0-7, if 24 interrupts then 0-5
Reserved (R)	3	0x0	
D11ext_Intr_swz	5:4	0x0	Swizzle D11 external INT A/B/C/D before maping to IOAPIC table/pins, 0=ABCD, 1=BCDA, 2=CDAB, 3=DABC
Reserved1 (R)	7:6	0x0	
D12ext_Intr_grp	10:8	0x0	MAP D12 external INT A/B/C/D to IOAPIC table/pins, if 32 interrupts then 0-7, if 24 interrupts then 0-5
Reserved2 (R)	11	0x0	
D12ext_Intr_swz	13:12	0x0	Swizzle D12 external INT A/B/C/D before maping to IOAPIC table/pins, 0=ABCD, 1=BCDA, 2=CDAB, 3=DABC
Reserved3 (R)	15:14	0x0	
D13ext_Intr_grp	18:16	0x0	MAP D13 external INT A/B/C/D to IOAPIC table/pins, if 32 interrupts then 0-7, if 24 interrupts then 0-5
Reserved4 (R)	19	0x0	
D13ext_Intr_swz	21:20	0x0	Swizzle D13 external INT A/B/C/D before maping to IOAPIC table/pins, 0=ABCD, 1=BCDA, 2=CDAB, 3=DABC
Reserved7 (R)	31:22	0x0	

IOAPIC_INT_ROUTING_REGISTER4 - RW - 32 bits - IOAPICCMISCIND:0x6

Field Name	Bits	Default	Description
D2int_Intr_map	4:0	0x0	Map D2 bridge interrupt to IOAPIC table/pin, if 32 interrupts then 0-31, if 24 interuppts then 0-23
Reserved1 (R)	7:5	0x0	
D3int_Intr_map	12:8	0x0	Map D3 bridge interrupt to IOAPIC table/pin, if 32 interrupts then 0-31, if 24 interuppts then 0-23
Reserved2 (R)	15:13	0x0	
D4int_Intr_map	20:16	0x0	Map D4 bridge interrupt to IOAPIC table/pin, if 32 interrupts then 0-31, if 24 interuppts then 0-23
Reserved3 (R)	23:21	0x0	
D5int_Intr_map	28:24	0x0	Map D5 bridge interrupt to IOAPIC table/pin, if 32 interrupts then 0-31, if 24 interuppts then 0-23
Reserved4 (R)	31:29	0x0	

IOAPIC_INT_ROUTING_REGISTER5 - RW - 32 bits - IOAPICCMISCIND:0x7			
Field Name	**Bits**	**Default**	**Description**
D6int_Intr_map	4:0	0x0	Map D6 bridge interrupt to IOAPIC table/pin, if 32 interrupts then 0-31, if 24 interuppts then 0-23
Reserved1 (R)	7:5	0x0	
D7int_Intr_map	12:8	0x0	Map D7 bridge interrupt to IOAPIC table/pin, if 32 interrupts then 0-31, if 24 interuppts then 0-23
Reserved2 (R)	15:13	0x0	
D8int_Intr_map	20:16	0x0	Map D8 bridge interrupt to IOAPIC table/pin, if 32 interrupts then 0-31, if 24 interuppts then 0-23
Reserved3 (R)	23:21	0x0	
D9int_Intr_map	28:24	0x0	Map D9 bridge interrupt to IOAPIC table/pin, if 32 interrupts then 0-31, if 24 interuppts then 0-23
Reserved4 (R)	31:29	0x0	

IOAPIC_INT_ROUTING_REGISTER6 - RW - 32 bits - IOAPICCMISCIND:0x8			
Field Name	**Bits**	**Default**	**Description**
D10int_Intr_map	4:0	0x0	Map D10 bridge interrupt to IOAPIC table/pin, if 32 interrupts then 0-31, if 24 interuppts then 0-23
Reserved1 (R)	7:5	0x0	
D11int_Intr_map	12:8	0x0	Map D11 bridge interrupt to IOAPIC table/pin, if 32 interrupts then 0-31, if 24 interuppts then 0-23
Reserved2 (R)	15:13	0x0	
D12int_Intr_map	20:16	0x0	Map D12 bridge interrupt to IOAPIC table/pin, if 32 interrupts then 0-31, if 24 interuppts then 0-23
Reserved3 (R)	23:21	0x0	
D13int_Intr_map	28:24	0x0	Map D13 bridge interrupt to IOAPIC table/pin, if 32 interrupts then 0-31, if 24 interuppts then 0-23
Reserved4 (R)	31:29	0x0	

IOAPIC_INT_ROUTING_REGISTER7 - RW - 32 bits - IOAPICCMISCIND:0x9			
Field Name	**Bits**	**Default**	**Description**
HT_Intr_map	4:0	0x0	Map HT internal interrupt to IOAPIC table/pin, if 32 interrupts then 0-31, if 24 interuppts then 0-23
Reserved1 (R)	7:5	0x0	
IOMMU_Intr_map	12:8	0x0	Map IOMMU internal interrupt to IOAPIC table/pin, if 32 interrupts then 0-31, if 24 interuppts then 0-23
Reserved2 (R)	31:13	0x0	

IOAPIC_SERIAL_IRQ_STATUS - R - 32 bits - IOAPICCMISCIND:0xA			
Field Name	**Bits**	**Default**	**Description**
Internal_irq_sts	31:0	0x0	Debug bus, Shows the status of the 32 IOAPIC interrupt table/pins

2.5.2 IOAPICMMISCIND Registers

IOAPIC_ID_REGISTER - RW - 32 bits - IOAPICMMISCIND:0x0			
Field Name	**Bits**	**Default**	**Description**
Reserved0	23:0	0x0	
ID	27:24	0x0	IOAPIC device ID
EXT_ID	31:28	0x0	Extended device ID. Writable Only if IOAPIC_ID_EXT_EN is set.

IOAPIC_VERSION_REGISTER - RW - 32 bits - IOAPICMMISCIND:0x1			
Field Name	**Bits**	**Default**	**Description**
Version	7:0	0x0	PCI 2.2 compliant
Reserved1	14:8	0x0	
PRQ	15	0x0	IRQ pin assertion supported
Max_Redirection_Entries (R)	23:16	0x0	Defaults to indicate 24 entries but can be changed to 32 entries via IOAPIC entries
Reserved	31:24	0x0	

IOAPIC_ARBITRATION_REGISTER - RW - 32 bits - IOAPICMMISCIND:0x2			
Field Name	**Bits**	**Default**	**Description**
Reserved2 (R)	23:0	0x0	
Arbitration_ID	27:24	0x0	Arbitration ID not really used
Reserved (R)	31:28	0x0	

NOTE: To avoid repetition, the two register tables below each represents 32 similar registers respectively (with the “n” in the field names running from 0 to 31), i.e., they represent REDIRECTION_TABLE_ENTRY_LOW_0 to REDIRECTION_TABLE_ENTRY_LOW_31 and REDIRECTION_TABLE_ENTRY_HIGH_0 to REDIRECTION_TABLE_ENTRY_HIGH_31.

Their addresses are in sequential order with the “low” and “high” alternating, starting with 0x10 and 0x11 for REDIRECTION_TABLE_ENTRY_LOW_0 and REDIRECTION_TABLE_ENTRY_HIGH_0 respectively, and ending with 0x4E and 0x4F for REDIRECTION_TABLE_ENTRY_LOW_31 and REDIRECTION_TABLE_ENTRY_HIGH_31 respectively.

REDIRECTION_TABLE_ENTRY_LOW_[31:0] - RW - 32 bits - IOAPICMMISCIND:0x10-0x4E			
Field Name	**Bits**	**Default**	**Description**
Vector_n	7:0	0x0	Interrupt vector associated with this interrupt
Delivery_Mode_n	10:8	0x0	Three bits fixed, 0- lowest 1-priority
Destination_Mode_n	11	0x0	0-Physical or 1-logical
Delivery_status_n (R)	12	0x0	0-idle 1-send pending
Interrupt_Pin_Polarity_n	13	0x0	0-high 1-low
Remote_IRR_n (R)	14	0x0	used only for level triggered, set when message delivered, cleared by EOI
Trigger_Mode_n	15	0x0	0-edge, 1-level
Mask_n	16	0x1	Write 0 to unmask
Reserved (R)	31:17	0x0	

REDIRECTION_TABLE_ENTRY_HIGH_[31:0] - RW - 32 bits - IOAPICMMISCIND:0x11-0x4F			
Field Name	**Bits**	**Default**	**Description**
Reserved (R)	23:0	0x0	
Destination_id_n	31:24	0x0	Bits 19-12 of the address field of the interrupt message

2.5.3 PCIEIND Registers

PCIE_RESERVED - R - 32 bits - PCIEIND:0x0			
Field Name	**Bits**	**Default**	**Description**
PCIE_RESERVED	31:0	0xffffffff	Reserved
Reserved			

PCIE_SCRATCH - RW - 32 bits - PCIEIND:0x1			
Field Name	**Bits**	**Default**	**Description**
PCIE_SCRATCH	31:0	0x0	Software test register
Software test register			

PCIE_HW_DEBUG - RW - 32 bits - PCIEIND:0x2			
Field Name	**Bits**	**Default**	**Description**
HW_00_DEBUG	0	0x0	Ignores DLLPs during L1 so that TXCLK can be turned off.
HW_01_DEBUG	1	0x0	Enable Replay Number Rolloever ECO
HW_02_DEBUG	2	0x0	REGS_POISONED_ADVISORY_NONFATAL_ERR_EN
HW_03_DEBUG	3	0x0	Enables the PLL power down when all lanes are inactive. It should be on in GPP.
HW_04_DEBUG	4	0x0	Bit [4]
HW_05_DEBUG	5	0x0	Bit [5]
HW_06_DEBUG	6	0x0	Bit [6]
HW_07_DEBUG	7	0x0	Bit [7]
HW_08_DEBUG	8	0x0	Turns on the BUG fix for the race problem between LC wakeup from L1 and PLL calibration in GEN2.
HW_09_DEBUG	9	0x0	Bit [9]
HW_10_DEBUG	10	0x0	Bit [10]
HW_11_DEBUG	11	0x0	Bit [11]
HW_12_DEBUG	12	0x0	Bit [12]
HW_13_DEBUG	13	0x0	Bit [13]
HW_14_DEBUG	14	0x0	Bit [14]
HW_15_DEBUG	15	0x0	Selects between the chip power state [1] and the software power state [0]
Hardware debug register			

PCIE_RX_NUM_NAK - R - 32 bits - PCIEIND:0xE			
Field Name	**Bits**	**Default**	**Description**
RX_NUM_NAK	31:0	0x0	Total number of naks received
Num naks received			

PCIE_RX_NUM_NAK_GENERATED - R - 32 bits - PCIEIND:0xF			
Field Name	**Bits**	**Default**	**Description**
RX_NUM_NAK_GENERATED	31:0	0x0	Total number of naks generated
Num naks generated			

PCIE_CNTL - RW - 32 bits - PCIEIND:0x10			
Field Name	**Bits**	**Default**	**Description**
HWINIT_WR_LOCK	0	0x0	Hardware write lock 0=HWInit registers unlocked 1=Lock HWInit registers
UR_ERR_REPORT_DIS	7	0x0	UR error reporting disable for TX
PCIE_HT_NP_MEM_WRITE	9	0x0	Memory write mapping enable
RX_SB_ADJ_PAYLOAD_SIZE	12:10	0x2	SB payload size 2=16 bytes 3=32 bytes 4=64 bytes
RX_RCB_REORDER_EN	16	0x1	RCB ordering enable 0=No re-ordering 1=Re-ordering
RX_RCB_INVALID_SIZE_DIS	17	0x1	RCB invalid size disable
RX_RCB_UNEXP_CPL_DIS	18	0x0	RCB unexpect cpl disable
RX_RCB_CPL_TIMEOUT_TEST_MODE	19	0x0	RCB cpl timeout test mode
RX_RCB_CHANNEL_ORDERING	20	0x0	GPP1 and GPP2 only. 1=Completion reordering within Snooped/Non-Snooped channel 0=Completion reordering both channels together (default)
RX_RCB_WRONG_ATTR_DIS	21	0x1	RCB invalid attributes check for received completions disable
RX_RCB_WRONG_FUNCNUM_DIS	22	0x1	RCB invalid function number check for received completions disable
LC_PREVENT_SPD_CHG_OVERLAP	23	0x1	Don't allow two speed change requests in opposite directions during the same clock cycle.
TX_CPL_DEBUG	29:24	0x0	CPL debug
RX_CPL_POSTED_REQ_ORD_EN	31	0x1	CPL request ordering enable 0=Disable RX request ordering 1=Enable RX request ordering
PCIExpress control register			

PCIE_CONFIG_CNTL - RW - 32 bits - PCIEIND:0x11			
Field Name	**Bits**	**Default**	**Description**
DYN_CLK_LATENCY	3:0	0x7	Dynamic Clock Latency
PCIExpress Configuration Control Register			

PCIE_DEBUG_CNTL - RW - 32 bits - PCIEIND:0x12			
Field Name	**Bits**	**Default**	**Description**
DEBUG_PORT_EN	7:0	0x1	Debug Bus Port Enable 1=port A 2=port B 4=port C 8=port D 16=port E 32=port F 64=port G 128=port H
DEBUG_SELECT	8	0x0	Debug Bus Select. For additional muxing (e.g. VC0 vs. VC1)

DEBUG_LANE_EN	31:16	0x1	Debug Lane Enable lane0=1 lane1=2 lane2=4 lane3=8 lane4=16 lane5=32 lane6=64 lane7=128 lane8=256 lane9=512 lane10=1024 lane11=2048 lane12=4096 lane13=8192 lane14=16384 lane15=32768
Debug Bus Control Register			

PCIE_RTR_CPL_TIMEOUT_STATUS - RW - 32 bits - PCIEIND:0x13			
Field Name	**Bits**	**Default**	**Description**
CI_SLV_R_RTR_ERROR	0	0x0	Slave req interface. 1 indicates slv RTR was de-asserted for more than the # of cycles programmed in the CNTL register, this bit remains asserted until it is cleared by writing a 1
CI_MST_R_RTR_ERROR	1	0x0	Master req interface. 1 indicates mst req RTR was de-asserted for more than the # of cycles programmed in the CNTL register, this bit remains asserted until it is cleared by writing a 1
CI_MST_C_RTR_ERROR	2	0x0	Master completion interface. 1 indicates mst cpl RTR was de-asserted for more than the # of cycles programmed in the CNTL register, this bit remains asserted until it is cleared by writing a 1
REG_R_RTR_ERROR	3	0x0	Register req interface. 1 indicates reg req RTR was de-asserted for more than the # of cycles programmed in the CNTL register, this bit remains asserted until it is cleared by writing a 1
TX_SLVCPL_TIMEOUT_ERROR	4	0x0	Slave completion interface. 1 indicates slv cpl hasn't been received for more than the # of cycles programmed in the CNTL register, this bit remains asserted until it is cleared by writing a 1. For RC this bit is for the Snoop channel.
TX_SLVCPL_NS_TIMEOUT_ERROR	5	0x0	Slave completion interface. 1 indicates slv cpl hasn't been received for more than the # of cycles programmed in the CNTL register, this bit remains asserted until it is cleared by writing a 1. For RC this bit is for the Non-Snoop channel.
CI_SLV_R_RTR_STATUS (R)	16	0x0	
CI_MST_R_RTR_STATUS (R)	17	0x0	
CI_MST_C_RTR_STATUS (R)	18	0x0	
REG_R_RTR_STATUS (R)	19	0x0	
TX_SLVCPL_TIMEOUT_STATUS (R)	20	0x0	
TX_SLVCPL_NS_TIMEOUT_STATUS (R)	21	0x0	
Status register for rtr/cpl timeout			

PCIE_CI_SLV_R_RTR_TIMEOUT_CNTL - RW - 32 bits - PCIEIND:0x14			
Field Name	**Bits**	**Default**	**Description**
CI_SLV_R_RTR_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the slv req RTR timer

CI_SLV_R_RTR_TIMEOUT_VALUE	31:4	0xffff	Value that indicates the # of cycles (in SLV_R_CLK) how long the RTR must be de-asserted before an error is flagged. This value is [31:4]. Bits [3:0] are zero. The min # of cylces is 0x10 (programming this field to 0x1)
Control register for slave request RTR timeout			

PCIE_CI_MST_R_RTR_TIMEOUT_CNTL - RW - 32 bits - PCIEIND:0x15			
Field Name	**Bits**	**Default**	**Description**
CI_MST_R_RTR_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the master req RTR timer
CI_MST_R_RTR_TIMEOUT_VALUE	31:4	0xffff	Value that indicates the # of cycles (in MST_R_CLK) how long the RTR must be de-asserted before an error is flagged. This value is [31:4], bits [3:0] are zero. The min # of cylces is 0x10 (programming this field to 0x1)
Control register for master request RTR timeout			

PCIE_CI_MST_C_RTR_TIMEOUT_CNTL - RW - 32 bits - PCIEIND:0x16			
Field Name	**Bits**	**Default**	**Description**
CI_MST_C_RTR_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the master cpl RTR timer
CI_MST_C_RTR_TIMEOUT_VALUE	31:4	0xffff	Value that indicates the # of cycles (in MST_C_CLK) how long the RTR must be de-asserted before an error is flagged. ; This value is [31:4], bits [3:0] are zero. The min # of cylces is 0x10 (programming this field to 0x1)
Control register for master completion RTR timeout			

PCIE_REG_R_RTR_TIMEOUT_CNTL - RW - 32 bits - PCIEIND:0x17			
Field Name	**Bits**	**Default**	**Description**
REG_R_RTR_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the register req RTR timer
REG_R_RTR_TIMEOUT_VALUE	31:4	0xffff	Value that indicates the # of cycles (in REG_R_CLK) how long the RTR must be de-asserted before an error is flagged. This value is [31:4], bits [3:0] are zero. The min # of cylces is 0x10 (programming this field to 0x1)
Control register for register request RTR timeout			

PCIE_TX_SLVCPL_TIMEOUT_CNTL - RW - 32 bits - PCIEIND:0x18			
Field Name	**Bits**	**Default**	**Description**
TX_SLVCPL_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the slave cpl timer
TX_SLVCPL_TIMEOUT_VC	3	0x0	Controls which virtual channel to monitor the cpl 0=VC0 1=VC1
TX_SLVCPL_TIMEOUT_VALUE	31:4	0xffff	Value that indicates the # of cycles (in SLV_C_CLK/SLV_S_CCLK) how long to wait for cpl before an error is flagged. This value is [31:4], bits [3:0] are zero. The min # of cylces is 0x10 (programming this field to 0x1)
Control register for slave completion timeout - snoop channel for RC			

PCIE_TX_SLVCPL_NS_TIMEOUT_CNTL - RW - 32 bits - PCIEIND:0x19			
Field Name	**Bits**	**Default**	**Description**
TX_SLVCPL_NS_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the slave cpl timer

TX_SLVCPL_NS_TIMEOUT_VC	3	0x0	Controls which channel to monitor the cpl 0=VC0 1=VC1
TX_SLVCPL_NS_TIMEOUT_VALUE	31:4	0xffff0	Value that indicates the # of cycles (in SLV_C_CLK/SLV_S_CCLK) how long to wait for cpl before an error is flagged. This value is [31:4], bits [3:0] are zero. The min # of cylces is 0x10 (programming this field to 0x1)
Control register for slave completion timeout - non-snoop channel			

PCIE_CNTL2 - RW - 32 bits - PCIEIND:0x1C			
Field Name	**Bits**	**Default**	**Description**
TX_ARB_ROUND_ROBIN_EN	0	0x0	TX round-robin arbitration enabled - for RC only
TX_ARB_SLV_LIMIT	5:1	0x0	TX slave arbitration limit
TX_ARB_MST_LIMIT	10:6	0x0	TX master arbitration limit

PCIE_CI_CNTL - RW - 32 bits - PCIEIND:0x20			
Field Name	**Bits**	**Default**	**Description**
CI_SLAVE_SPLIT_MODE	2	0x0	0=RC - Full completions from Channel A or B 1=RC - Completions split on Channel A and B evenly
CI_SLAVE_GEN_USR_DIS	3	0x0	Sends USR for invalid addresses 0=Sends USR for invalid addresses 1=Disables slave from sending USR, and instead sends a successful CMPLT_D with dummy data.
CI_MST_CMPL_DUMMY_DATA	4	0x1	0xDEADBEEF or 0xFFFFFFFF 0=0xDEADBEEF 1=0xFFFFFFFF
CI_SLV_RC_RD_REQ_SIZE	7:6	0x1	Slave read requests supported size to client. 0=32/64 byte requests supported 1=64 byte requests only 2=16/32/64
CI_SLV_ORDERING_DIS	8	0x0	Disables slave ordering logic 0=Enable slave ordering logic 1=Disable slave ordering logic
CI_RC_ORDERING_DIS	9	0x0	Disables RC ordering logic 0=Enable RC ordering logic 1=Disable RC ordering logic
CI_SLV_CPL_ALLOC_DIS	10	0x0	Slave CPL buffer is sub-divided or not 0=Slave CPL buffer is sub-divided between ports based on number of lanes active 1=Slave CPL buffer is not sub-divided
CI_SLV_CPL_ALLOC_MODE	11	0x0	Slave Cpl buffer method for sub-division 0=Dynamic 1=Register limits CI_SLV_CPL_STATIC_ALLOC_LIMIT_(N)S
TX_SLV_CPL_DELAY_EN	13	0x0	Enables Delay on Slave Completion Data path. RC only
TX_SLV_CPL_DELAY_TIMER	23:14	0x0	Delay timeout. Effective delay = 7 * TIMER * SLV_S_C_CLK_period
CI_SLV_REQ_DELAY_EN	24	0x0	Enables Delay on Slave Request path
CI_SLV_REQ_DELAY_TIMER	30:25	0x0	Delay timeout. Effective delay = 4 * TIMER * SLV_R_CLK_period
Chip interface control register			

PCIE_BUS_CNTL - RW - 32 bits - PCIEIND:0x21			
Field Name	**Bits**	**Default**	**Description**
BUS_DBL_RESYNC	0	0x1	Double flop the sync module. 0=Normal 1=Add extra resynchronizing clock
PMI_INT_DIS	6	0x0	PMI Interrupt Disable 0=Normal 1=Disable
IMMEDIATE_PMI_DIS	7	0x0	Immediate PMI Disable 0=Enable 1=Disable
PCI Express Bus Control Register			

PCIE_LC_STATE6 - R - 32 bits - PCIEIND:0x22			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE24	5:0	0x0	24th previous state
LC_PREV_STATE25	13:8	0x0	25th previous state
LC_PREV_STATE26	21:16	0x0	26th previous state
LC_PREV_STATE27	29:24	0x0	27th previous state
Link Control State Registers			

PCIE_LC_STATE7 - R - 32 bits - PCIEIND:0x23			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE28	5:0	0x0	28th previous state
LC_PREV_STATE29	13:8	0x0	29th previous state
LC_PREV_STATE30	21:16	0x0	30th previous state
LC_PREV_STATE31	29:24	0x0	31st previous state
Link Control State Registers			

PCIE_LC_STATE8 - R - 32 bits - PCIEIND:0x24			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE32	5:0	0x0	32nd previous state
LC_PREV_STATE33	13:8	0x0	33rd previous state
LC_PREV_STATE34	21:16	0x0	34th previous state
LC_PREV_STATE35	29:24	0x0	35th previous state
Link Control State Registers			

PCIE_LC_STATE9 - R - 32 bits - PCIEIND:0x25			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE36	5:0	0x0	36th previous state
LC_PREV_STATE37	13:8	0x0	37th previous state
LC_PREV_STATE38	21:16	0x0	38th previous state
LC_PREV_STATE39	29:24	0x0	39th previous state
Link Control State Registers			

PCIE_LC_STATE10 - R - 32 bits - PCIEIND:0x26			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE40	5:0	0x0	40th previous state
LC_PREV_STATE41	13:8	0x0	41st previous state

LC_PREV_STATE42	21:16	0x0	42nd previous state
LC_PREV_STATE43	29:24	0x0	43rd previous state
Link Control State Registers			

PCIE_LC_STATE11 - R - 32 bits - PCIEIND:0x27			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE44	5:0	0x0	44th previous state
LC_PREV_STATE45	13:8	0x0	45th previous state
LC_PREV_STATE46	21:16	0x0	46th previous state
LC_PREV_STATE47	29:24	0x0	47th previous state
Link Control State Registers			

PCIE_LC_STATUS1 - R - 32 bits - PCIEIND:0x28			
Field Name	**Bits**	**Default**	**Description**
LC_REVERSE_RCVR	0	0x0	Receiver reversal status. When asserted, received data is reversed (i.e. logical lane 0 is not received on physical lane 0)
LC_REVERSE_XMIT	1	0x0	Tranmitter reversal status. When asserted, transmitted data is reversed (i.e. logical lane 0 is not transmitted on physical lane 0).
LC_OPERATING_LINK_WIDTH	4:2	0x0	Current width of the Link.
LC_DETECTED_LINK_WIDTH	7:5	0x0	Detected width of the Link. This identifies the maximum possible link width that is physically allowed.
Link Control Status Register 1			

PCIE_LC_STATUS2 - R - 32 bits - PCIEIND:0x29			
Field Name	**Bits**	**Default**	**Description**
LC_TOTAL_INACTIVE_LANES	15:0	0x0	Lanes that are not being used.
LC_TURN_ON_LANE	31:16	0x0	Lanes that are available for link width negotiation. Not all available lanes will always be used (the actual number depends on lanes supported by the other end of the link).
Link Control Status Register 2			

PCIE_WPR_CNTL - RW - 32 bits - PCIEIND:0x30			
Field Name	**Bits**	**Default**	**Description**
WPR_RESET_HOT_RST_EN	0	0x1	Enables Hot Reset feature.
WPR_RESET_LNK_DWN_EN	1	0x0	Enables Link down reset feature.
WPR_RESET_LNK_DIS_EN	2	0x1	Enables Link disable reset feature.
WPR_RESET_COR_EN	3	0x0	Enables external CORE reset feature.
WPR_RESET_REG_EN	4	0x0	Enables external REGISTER reset feature.
WPR_RESET_STY_EN	5	0x0	Enables external Stickybit Register reset feature.
WPR_RESET_PHY_EN	6	0x0	Enables external PHY reset feature.
WPR Control Register			

PCIE_RX_LAST_TLP0 - R - 32 bits - PCIEIND:0x31			
Field Name	**Bits**	**Default**	**Description**
RX_LAST_TLP0	31:0	0x0	Bits [31:0]
Last received TLP			

PCIE_RX_LAST_TLP1 - R - 32 bits - PCIEIND:0x32			
Field Name	**Bits**	**Default**	**Description**
RX_LAST_TLP1	31:0	0x0	Bits [63:32]
Last received TLP			

PCIE_RX_LAST_TLP2 - R - 32 bits - PCIEIND:0x33			
Field Name	**Bits**	**Default**	**Description**
RX_LAST_TLP2	31:0	0x0	Bits [95:64]
Last received TLP			

PCIE_RX_LAST_TLP3 - R - 32 bits - PCIEIND:0x34			
Field Name	**Bits**	**Default**	**Description**
RX_LAST_TLP3	31:0	0x0	Bits [127:96]
Last received TLP			

PCIE_TX_LAST_TLP0 - R - 32 bits - PCIEIND:0x35			
Field Name	**Bits**	**Default**	**Description**
TX_LAST_TLP0	31:0	0x0	Bits [31:0]
Last transmitted TLP			

PCIE_TX_LAST_TLP1 - R - 32 bits - PCIEIND:0x36			
Field Name	**Bits**	**Default**	**Description**
TX_LAST_TLP1	31:0	0x0	Bits [63:32]
Last transmitted TLP			

PCIE_TX_LAST_TLP2 - R - 32 bits - PCIEIND:0x37			
Field Name	**Bits**	**Default**	**Description**
TX_LAST_TLP2	31:0	0x0	Bits [95:64]
Last transmitted TLP			

PCIE_TX_LAST_TLP3 - R - 32 bits - PCIEIND:0x38			
Field Name	**Bits**	**Default**	**Description**
TX_LAST_TLP3	31:0	0x0	Bits [127:96]
Last transmitted TLP			

PCIE_I2C_DEBUG_BUS - R - 32 bits - PCIEIND:0x39			
Field Name	**Bits**	**Default**	**Description**
DEBUG_SEL_BLK1	5:0	0x0	Sets Debug Bus Block ID for Debug Block1.
DEBUG_SEL_BLK2	11:6	0x0	Sets Debug Bus Block ID for Debug Block2.
DEBUG_MUX_BLK1	17:12	0x0	Sets Debug mux number for Debug Block1.
DEBUG_MUX_BLK2	23:18	0x0	Sets Debug mux to Debug Block2.
DEBUG_BUS_BLK1	24	0x0	Sets upper/lower debug port for Debug Block1.
DEBUG_BUS_BLK2	25	0x0	Upper/lower debug port for Debug Block2.

DEBUG_EN	26	0x0	Enables debug daisy chain.
DEBUG_MULTIBLOCK_EN	27	0x0	Enables multiple debug blocks.
DEBUG_RESERVE	31:28	0x0	Reserved.
I2C Backdoor Debug Bus Control.			

PCIE_I2C_REG_ADDR_EXPAND - RW - 32 bits - PCIEIND:0x3A			
Field Name	**Bits**	**Default**	**Description**
I2C_REG_ADDR (R)	16:0	0x0	Read-only register for reading back the accessing register address
BDI2C_CPLDATA_RTN_EXPAND	20:17	0x0	Retime the cpl_valid for crossing clock domain from REC_C_CLK to REG_R_CLK in I2C backdoor
BDREG_CPLDATA_RTN_EXPAND	24:21	0x3	Retime the REG_READ_REQUEST for crossing clock domain from REG_C_CLK to REG_R_CLK in REG_SYNC.
I2C Register Address Expand			

PCIE_I2C_REG_DATA - R - 32 bits - PCIEIND:0x3B			
Field Name	**Bits**	**Default**	**Description**
I2C_REG_DATA	31:0	0x0	Register write/read data.

PCIE_CFG_CNTL - RW - 32 bits - PCIEIND:0x3C			
Field Name	**Bits**	**Default**	**Description**
CFG_EN_DEC_TO_GEN2_HIDDEN_REG	0	0x0	Enables decoding of GEN2 hidden registers
CFG_EN_DEC_TO_HIDDEN_REG	1	0x0	Enables decoding of hidden registers (excluding GEN2)
Configuration space control register			

PCIE_P_CNTL - RW - 32 bits - PCIEIND:0x40			
Field Name	**Bits**	**Default**	**Description**
P_PWRDN_EN	0	0x0	Enables powering down transmitter and receiver pads along with PLL macros
P_SYMALIGN_MODE	1	0x0	Data Valid generation bit iMODE = 0 (Relax Mode): Update its symbol right away when detect any bit shift, i.e. data_valid will always assert. iMODE = 1 (Aggressive Mode): Need confirmation before muxing out the data 0=Relax Mode - Update symbol lock right away when detected bit shifts without waiting for confirmation 1=Aggressive Mode - Always need confirmation for asserting Data Valid
P_ENABLE_PLL_LOCKING_IN_QUICKSIM	2	0x0	Enables actual PLL locking time (30us) when QUICKSIM=1 for simulation purpose. 0=PLL locking time is minimal when QUICKSIM=1 1=Enable normal PLL locking time when QUICKSIM=1
P_PLL_PWRDN_IN_L1L23	3	0x0	Enables PLL powerdown in L1 or L23 Ready states (only if all the associated LC's are in Sates L1 / L23 corresponding to 4 / 2 lanes based on mpConfig and architecture) 0=PLL is always running regardless of Link States 1=PLL will be turned off during L1

P_PLL_BUF_PDNB	4	0x1	Disables 10X clock pad on a per PLL basis (should be 1'b0 in order to activate this powersafe feature) 0=Enable PLL Buffer to power down during L1 1=Always keep PLL Buffer running
P_TXCLK_SND_PWRDN	5	0x0	Enables powering down TXCLK clock pads on the transmit side. Each clock pad corresponds to logic associated with 4 lanes.
P_TXCLK_RCV_PWRDN	6	0x0	Enables powering down TXCLK clock pads on the receive side. Each clock pad corresponds to logic associated with 4 lanes.
B_PG2RX_CR_EN_MODE	7	0x0	PHY's CDR Locking (CR_EN) mode 0=CR_EN is LTSSM driven. 1=CR_EN is PHY driven, based on P90_BRX_ELEC_IDLE_ASYNC
P_MASK_RCVR_EIDLE_EN	8	0x0	Enables EIDLE mask for powered down receivers. 0=Don't intercept ELEC_IDLE in power down 1=Intercept ELEC_IDLE in RX power down
P_PLL_PDNB	9	0x1	Enables PLL only (not the buffer) to power down in L1 or L23ready states. 0=Enable PLL to power down during L1 1=Always keep PLL running
P_SYMALIGN_HW_DEBUG	10	0x0	Enable continual impendence calibration ECO
P_ELASTDESKEW_HW_DEBUG	11	0x0	Enable Data truncation in lanedemux ECO
P_ALLOW_PRX_FRONTEND_SHUTOFF	12	0x0	Enables PHY's RX FRONTEND to shut off during L1 when PLL power down is enabled. 0=RX Frontend is always power on 1=RX Frontend is shutoff during L1 when PLL power down is enabled
P_ALWAYS_USE_FAST_TXCLK	13	0x0	Bypasses TXCLK_SWITCH and uses 500MHz TXCLK from PLL for both GEN1 and GEN2 speed. 0=TXCLK will be either 250MHz or 500MHz depends on port speeds 1=Bypass TXCLK_SWITCH and always use 500MHz TXCLK
P_ELEC_IDLE_MODE	15:14	0x0	Electrical Idle Mode for PI (Physical Layer). 0=GEN1 - entry:PHY, exit:PHY; GEN2 - entry:infer, exit:PHY 1=GEN1 - entry:infer, exit:PHY; GEN2 - entry:infer, exit PHY 2=GEN1 - entry:PHY, exit:PHY; GEN2 - entry:PHY, exit:PHY 3=Reserved
P_CLK_SWITCH_MODE	17:16	0x0	TXCLK Clock Speed Switch mode. 0=None - switch anytime and bypass skid buffer 1=Wait TX idle - switch when TX is idle 2=Enable skid buffer - switch anytime and enable skid buffer 3=Reserved
P_RXEN_GATER	27:24	0x2	Clock cycle delay for muxing back RXCLK when RX_EN is re-asserted again.
PHY Control Register			

PCIE_P_BUF_STATUS - RW - 32 bits - PCIEIND:0x41			
Field Name	**Bits**	**Default**	**Description**
P_OVERFLOW_ERR	15:0	0x0	Buffer Overflow Status - one bit per lane (RW1C)
P_UNDERFLOW_ERR	31:16	0x0	Buffer Underflow Status - one bit per lane (RW1C)
PHY BUFFER STATUS REGISTER			

PCIE_P_DECODER_STATUS - RW - 32 bits - PCIEIND:0x42			
Field Name	**Bits**	**Default**	**Description**

P_DECODE_ERR	15:0	0x0	Decode Error Status - one bit per lane (RW1C)
PHY DECODER STATUS REGISTER			

PCIE_P_MISC_STATUS - RW - 32 bits - PCIEIND:0x43			
Field Name	**Bits**	**Default**	**Description**
P_DESKEW_ERR	7:0	0x0	Deskew Error Status. One bit per port (RW1C)
P_SYMUNLOCK_ERR	31:16	0x0	Symbol Unlock Status. One bit per lane (RW1C)
Miscellaneous Status Register			

PCIE_P_PLL_CNTL - RW - 32 bits - PCIEIND:0x44			
Field Name	**Bits**	**Default**	**Description**
P_VCOREF	1:0	0x0	Controls the signal generation used in calibrating PLLs 0=OFF 1=VDD/4 2=VDD/2 3=3VDD/4
P_CALREF	3:2	0x0	Controls the signal generation used in calibrating PLLs 0=OFF 1=VDD/2 2=2VDD/3 3=5VDD/6
PHY PLL CONTROL REGISTER			

PCIE_P_RCV_L0S_FTS_DET - RW - 32 bits - PCIEIND:0x50			
Field Name	**Bits**	**Default**	**Description**
P_RCV_L0S_FTS_DET_MIN (R)	7:0	0xff	Minimum number of FTS order set detected during RCV L0s
P_RCV_L0S_FTS_DET_MAX (R)	15:8	0x0	Maximum number of FTS order set detected during RCV L0s
Number of FTS order set detected during RCV L0s (write to reset)			

PCIE_P_IMP_CNTL_STRENGTH - RW - 32 bits - PCIEIND:0x60			
Field Name	**Bits**	**Default**	**Description**
P_TX_STR_CNTL_READ_BACK (R)	3:0	0x0	Stores the readback value of current controller
P_TX_IMP_CNTL_READ_BACK (R)	7:4	0x0	Stores the readback value of TX impedance controller
P_RX_IMP_CNTL_READ_BACK (R)	11:8	0x0	Stores the readback value of RX impedance controller
P_TX_STR_CNTL	19:16	0x7	Sets the initial default current strength to 4'b0111
P_TX_IMP_CNTL	23:20	0x6	Default TX impedance control value
P_RX_IMP_CNTL	27:24	0x6	Default RX impedance control value
P_PAD_MANUAL_OVERRIDE	31	0x0	Enables Current and Impedance control values to override 0=Allow normal impedance compensation operation 1=Default to manual settings
PHY IMPEDANCE CONTROL STRENGTH REGISTER			

PCIE_P_IMP_CNTL_UPDATE - RW - 32 bits - PCIEIND:0x61			
Field Name	**Bits**	**Default**	**Description**
P_IMP_PAD_UPDATE_RATE	4:0	0xe	PAD's update interval 0=PHY130 default 0xf 1=PHY90 default 0xe
P_IMP_PAD_SAMPLE_DELAY	12:8	0x1	Sampling window
P_IMP_PAD_INC_THRESHOLD	20:16	0x18	Incremental resolution
P_IMP_PAD_DEC_THRESHOLD	28:24	0x8	Decremental resolution

Impedance PAD defaults

PCIE_P_STR_CNTL_UPDATE - RW - 32 bits - PCIEIND:0x62			
Field Name	**Bits**	**Default**	**Description**
P_STR_PAD_UPDATE_RATE	4:0	0xf	PAD's update interval 0=PHY130 default 0xf 1=PHY90 default 0xe
P_STR_PAD_SAMPLE_DELAY	12:8	0x1	Sampling window
P_STR_PAD_INC_THRESHOLD	20:16	0x18	Incremental resolution
P_STR_PAD_DEC_THRESHOLD	28:24	0x8	Decremental resolution
Current PAD defaults			

PCIE_P_PAD_MISC_CNTL - RW - 32 bits - PCIEIND:0x63			
Field Name	**Bits**	**Default**	**Description**
P_PAD_I_DUMMYOUT (R)	0	0x0	Input from analog - 0 if PMOS cur is stronger
P_PAD_IMP_DUMMYOUT (R)	1	0x0	Input from analog - 0 if PMOS imp is stronger
P_PAD_IMP_TESTOUT (R)	2	0x0	Input from analog - 1 if NMOS imp is stronger
P_PLLCAL_INC_LOWER_PHASE	6:4	0x1	0=0us 1=1us 2=2us 3=4us 4=8us 5=12us 6=16us 7=24us
Pad Miscellaneous Control Registers			

PCIE_P_PAD_FORCE_EN - RW - 32 bits - PCIEIND:0x64			
Field Name	**Bits**	**Default**	**Description**
B_PTX_PDNB_FEN	7:0	0x0	Forces B_PTX_PDNB to enable TX pad
B_PRX_PDNB_FEN	15:8	0x0	Forces B_PRX_RDNB to enable RX pad
B_PPLL_PDNB_FEN	19:16	0x0	Forces B_PPLL_PDNB to enable PLL
B_PPLL_BUF_PDNB_FEN	23:20	0x0	Forces B_PPLL_BUF_PDNB to enable 10x driver in PLL
B_PI_DREN_FEN	24	0x0	Forces B_PI_DREN to enable current calibration pad
B_PBG_PDNB_FEN	25	0x0	Forces B_PBG_PDNB to enable Bandgap circuit in current calibration pad
B_PIMP_TX_PDNB_FEN	26	0x0	Forces B_PIMP_TX_PDNB to enable TX impedance calibration pad
B_PIMP_RX_PDNB_FEN	27	0x0	Forces B_PIMP_RX_PDNB to enable RX impedance calibration pad
Powerdown enable signals used by the wrapper			

PCIE_P_PAD_FORCE_DIS - RW - 32 bits - PCIEIND:0x65			
Field Name	**Bits**	**Default**	**Description**
B_PTX_PDNB_FDIS	7:0	0x0	Forces B_PTX_PDNB to disable TX pad
B_PRX_PDNB_FDIS	15:8	0x0	Forces B_PRX_PDNB to disable RX pad
B_PPLL_PDNB_FDIS	19:16	0x0	Forces B_PPLL_PDNB to disable PLL
B_PPLL_BUF_PDNB_FDIS	23:20	0x0	Forces B_PPLL_BUF_PDNB to disable 10x driver in PLL
B_PI_DREN_FDIS	24	0x0	Forces B_PI_DREN to disable current calibration pad
B_PBG_PDNB_FDIS	25	0x0	Forces B_PBG_PDNB to disable Bandgap circuit in current calibration pad
B_PIMP_TX_PDNB_FDIS	26	0x0	Forces B_PIMP_TX_PDNB to disable TX impedance calibration pad

B_PIMP_RX_PDNB_FDIS	27	0x0	Forces B_PIMP_TX_PDNB to disable RX impedance calibration pad
Powerdown disable signals used by the wrapper			

PCIE_STRAP_MISC - RW - 32 bits - PCIEIND:0xC0			
Field Name	**Bits**	**Default**	**Description**
STRAP_LINK_CONFIG	3:0	0x0	Provides an override for STRAP_LINK_CONFIG
RESERVED1 (R)	4	0x0	
STRAP_BYPASS_SCRAMBLER	6	0x0	Provides an override for STRAP_BYPASS_SCRAMBLER
STRAP_PHY_RCVRDET_3NF	7	0x0	Provides an override for STRAP_PHY_RCVRDET_3NF
STRAP_F0_AER_EN	8	0x0	Provides an override for STRAP_F0_AER_EN
STRAP_F0_EN	9	0x0	Provides an override for STRAP_F0_EN
STRAP_F0_MSI_EN	10	0x0	Provides an override for STRAP_F0_MSI_EN
STRAP_F0_VC_EN	11	0x0	Provides an override for STRAP_F0_VC_EN
STRAP_F0_LEGACY_DEVICE_TYPE_EN	12	0x0	Provides an override for STRAP_F0_LEGACY_DEVICE_TYPE_EN
STRAP_FIRST_RCVD_ERR_LOG	23	0x0	Provides an override for STRAP_FIRST_RCVD_ERR_LOG 0=FIRST DETECTED ERROR LOGGING 1=FIRST RECEIVED ERROR LOGGING
STRAP_CLK_PM_EN	24	0x0	Provides an override for STRAP_CLK_PM_EN
STRAP_ECN1P1_EN	25	0x0	Provides an override for STRAP_ECN1P1_EN
STRAP_EXT_VC_COUNT	26	0x0	Provides an override for STRAP_EXT_VC_COUNT
RESERVED2 (R)	27	0x0	
STRAP_REVERSE_ALL	28	0x0	Provides an override for STRAP_REVERSE_ALL
STRAP_MST_ADR64_EN	29	0x0	Provides an override for STRAP_MST_ADR64_EN
Misc strap loadable register values			

PCIE_STRAP_MISC2 - RW - 32 bits - PCIEIND:0xC1			
Field Name	**Bits**	**Default**	**Description**
STRAP_LINK_BW_NOTIFICATION_CAP_EN	0	0x0	STRAP_LINK_BW_NOTIFICATION_CAP_EN
STRAP_GEN2_COMPLIANCE	1	0x0	Provides an override for STRAP_GEN2_COMPLIANCE
STRAP_MSTCPL_TIMEOUT_EN	2	0x0	Provides an override for STRAP_MSTCPL_TIMEOUT_EN
Misc strap loadable register values 2			

PCIE_STRAP_PI - RW - 32 bits - PCIEIND:0xC2			
Field Name	**Bits**	**Default**	**Description**
STRAP_QUICKSIM_START	0	0x0	Provides an override for STRAP_QUICKSIM_START
STRAP_BACKGROUND_IMP_CAL	1	0x0	Provides an override for STRAP_BACKGROUND_IMP_CAL
STRAP_IMP_MANUAL_OVERRIDE	2	0x0	Provides an override for STRAP_IMP_MANUAL_OVERRIDE
STRAP_PAD_RX_MANUAL_IMPEDANCE	6:3	0x0	Provides an override for STRAP_PAD_RX_MANUAL_IMPEDANCE
STRAP_PAD_TX_MANUAL_IMPEDANCE	10:7	0x0	Provides an override for STRAP_PAD_TX_MANUAL_IMPEDANCE
STRAP_STAGGER_CNTL	16:15	0x0	Provides an override for STRAP_STAGGER_CNTL
STRAP_TX_PDNB_MODE	17	0x0	Provides an override for STRAP_TX_PDNB_MODE
STRAP_VCO_MODE	19:18	0x0	Provides an override for STRAP_VCO_MODE
STRAP_INC_PLLCAL_PHASE	24:21	0x0	Provides an override for STRAP_INC_PLLCAL_PHASE
STRAP_PHY_RX_INCAL_FORCE	25	0x0	Provides an override for STRAP_PHY_RX_INCAL_FORCE
STRAP_TEST_TOGGLE_PATTERN	28	0x0	Provides an override for STRAP_TEST_TOGGLE_PATTERN
STRAP_TEST_TOGGLE_MODE	29	0x0	Provides an override for STRAP_TEST_TOGGLE_MODE
Misc PI strap loadable register values			

PCIE_B_P90_CNTL - RW - 32 bits - PCIEIND:0xC3

Field Name	Bits	Default	Description
B_P90IMP_BACKUP	3:0	0x0	Impedance Control Backup
B_P90PLL_BACKUP	31:12	0x0	PLL Control Backup

PCIE_STRAP_I2C_BD - RW - 32 bits - PCIEIND:0xC4			
Field Name	**Bits**	**Default**	**Description**
STRAP_BIF_I2C_SLV_ADR	6:0	0x0	Provides an override for STRAP_BIF_I2C_SLV_ADR
STRAP_BIF_DBG_I2C_EN	7	0x0	Provides an override for STRAP_BIF_DBG_I2C_EN
I2C Straps			

PCIE_P90RX_PRBS10_CNTL - RW - 32 bits - PCIEIND:0xC6			
Field Name	**Bits**	**Default**	**Description**
P90RX_PRBS10_CLR	15:0	0x0	Clears PRBS10_ERRCNT on lane[x]
P90TX_PRBS10_EN	31:16	0x0	Enables PRBS10 checker on lane[x]

PCIE_P90_BRX_PRBS10_ER - R - 32 bits - PCIEIND:0xC7			
Field Name	**Bits**	**Default**	**Description**
P90_BRX_PRBS10_ER	15:0	0x0	Status bit indicates that a PRBS10 error has occured on lane[x]

PCIE_PRBS_CLR - RW - 32 bits - PCIEIND:0xC8			
Field Name	**Bits**	**Default**	**Description**
PRBS_CLR	15:0	0x0	Clears PRBS_ERRCNT_x on lane[x]
PRBS_CHECKER_DEBUG_BUS_SELECT	19:16	0x0	Selects prbs_chk debug signals of different lanes 0=Checker 0 debug bus 1=Checker 1 debug bus 2=Etc

PCIE_PRBS_STATUS1 - R - 32 bits - PCIEIND:0xC9			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRSTAT	15:0	0x0	Status bit indicates that a PRBS23 error has occured on lane[x]
PRBS_LOCKED	31:16	0x0	Status bit indicates that the PRBS pattern has locked on lane[x]

PCIE_PRBS_STATUS2 - R - 32 bits - PCIEIND:0xCA			
Field Name	**Bits**	**Default**	**Description**
PRBS_BITCNT_DONE	15:0	0x0	Indicates that the PRBS test finished in non-free-run mode for lane[x]

PCIE_PRBS_FREERUN - RW - 32 bits - PCIEIND:0xCB			
Field Name	**Bits**	**Default**	**Description**
PRBS_FREERUN	15:0	0x0	The PRBS23 error checker is free running on lane[x]

PCIE_PRBS_MISC - RW - 32 bits - PCIEIND:0xCC			
Field Name	**Bits**	**Default**	**Description**
PRBS_EN	0	0x0	Enables the prbs generator and checkers 0=PRBS GEN disable 1=PRBS GEN enable
PRBS_TEST_MODE	2:1	0x0	Sets different test modes: 0=00 - PRBS23 1=01 - PRBS31 2=10 - COUNTER 3=11 - USER DEFINED
PRBS_USER_PATTERN_TOGGLE	3	0x0	Toggles two 8-bit user-defined patterns in 8-bit mode. The 1st pattern is in PRBS_USER_PATTERN[7:0] and the 2nd pattern is in PRBS_USER_PATTERN[15:8]. 0=0 - Replicate user pattern1 1=1 - Toggle user pattern1 and pattern2
PRBS_8BIT_SEL	4	0x0	Sets the 8bit and 10bit modes: 0=0 - 10 BIT 1=1 - 8 BIT
PRBS_COMMA_NUM	6:5	0x0	Programs the number of COMMA symbols in prbs_gen for recovering bit lock in 8-bit mode. 0=00 - 4 1=01 - 8 2=10 - 16 3=11 - 32
PRBS_LOCK_CNT	11:7	0x0	Programs the number of clock cycles for prbs checker to setup bit lock.
PRBS_GEN2_SPEED	15	0x0	Programs the signal speed: 0=0 - GEN1 speed 1=1 - GEN2 speed
PRBS_CHK_ERR_MASK	31:16	0x0	Masks PRBS_CHK_ERR output of prbs_chk for lane[x].
PRBS Miscellaneous Control Register			

PCIE_PRBS_USER_PATTERN - RW - 32 bits - PCIEIND:0xCD			
Field Name	**Bits**	**Default**	**Description**
PRBS_USER_PATTERN	29:0	0x0	30-bit PRBS User Defined Pattern

PCIE_PRBS_LO_BITCNT - RW - 32 bits - PCIEIND:0xCE			
Field Name	**Bits**	**Default**	**Description**
PRBS_LO_BITCNT	31:0	0x0	Number of bits to check by the PRBS23 error checkers.

PCIE_PRBS_HI_BITCNT - RW - 32 bits - PCIEIND:0xCF			
Field Name	**Bits**	**Default**	**Description**

PRBS_HI_BITCNT	7:0	0x0	Number of bits to check by the PRBS23 error checkers.

PCIE_PRBS_ERRCNT_0 - R - 32 bits - PCIEIND:0xD0			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_0	31:0	0x0	Number of errors detected on lane 0.

PCIE_PRBS_ERRCNT_1 - R - 32 bits - PCIEIND:0xD1			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_1	31:0	0x0	Number of errors detected on lane 1.

PCIE_PRBS_ERRCNT_2 - R - 32 bits - PCIEIND:0xD2			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_2	31:0	0x0	Number of errors detected on lane 2.

PCIE_PRBS_ERRCNT_3 - R - 32 bits - PCIEIND:0xD3			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_3	31:0	0x0	Number of errors detected on lane 3.

PCIE_PRBS_ERRCNT_4 - R - 32 bits - PCIEIND:0xD4			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_4	31:0	0x0	Number of errors detected on lane 4.

PCIE_PRBS_ERRCNT_5 - R - 32 bits - PCIEIND:0xD5			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_5	31:0	0x0	Number of errors detected on lane 5.

PCIE_PRBS_ERRCNT_6 - R - 32 bits - PCIEIND:0xD6			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_6	31:0	0x0	Number of errors detected on lane 6.

PCIE_PRBS_ERRCNT_7 - R - 32 bits - PCIEIND:0xD7			
Field Name	**Bits**	**Default**	**Description**

PRBS_ERRCNT_7	31:0	0x0	Number of errors detected on lane 7.

PCIE_PRBS_ERRCNT_8 - R - 32 bits - PCIEIND:0xD8			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_8	31:0	0x0	Number of errors detected on lane 8.

PCIE_PRBS_ERRCNT_9 - R - 32 bits - PCIEIND:0xD9			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_9	31:0	0x0	Number of errors detected on lane 9.

PCIE_PRBS_ERRCNT_10 - R - 32 bits - PCIEIND:0xDA			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_10	31:0	0x0	Number of errors detected on lane 10.

PCIE_PRBS_ERRCNT_11 - R - 32 bits - PCIEIND:0xDB			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_11	31:0	0x0	Number of errors detected on lane 11.

PCIE_PRBS_ERRCNT_12 - R - 32 bits - PCIEIND:0xDC			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_12	31:0	0x0	Number of errors detected on lane 12.

PCIE_PRBS_ERRCNT_13 - R - 32 bits - PCIEIND:0xDD			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_13	31:0	0x0	Number of errors detected on lane 13.

PCIE_PRBS_ERRCNT_14 - R - 32 bits - PCIEIND:0xDE			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_14	31:0	0x0	Number of errors detected on lane 14.

PCIE_PRBS_ERRCNT_15 - R - 32 bits - PCIEIND:0xDF			
Field Name	**Bits**	**Default**	**Description**

PRBS_ERRCNT_15	31:0	0x0	Number of errors detected on lane 15.

2.5.4 PCIEIND_P Registers

PCIEP_RESERVED - R - 32 bits - PCIEIND_P:0x0			
Field Name	**Bits**	**Default**	**Description**
PCIEP_RESERVED	31:0	0xffffffff	Reserved
Reserved			

PCIEP_SCRATCH - RW - 32 bits - PCIEIND_P:0x1			
Field Name	**Bits**	**Default**	**Description**
PCIEP_SCRATCH	31:0	0x0	Scratch Register
Scratch Register			

PCIEP_HW_DEBUG - RW - 32 bits - PCIEIND_P:0x2			
Field Name	**Bits**	**Default**	**Description**
HW_00_DEBUG	0	0x0	Bit [0]
HW_01_DEBUG	1	0x0	Bit [1]
HW_02_DEBUG	2	0x0	Bit [2]
HW_03_DEBUG	3	0x0	Bit [3]
HW_04_DEBUG	4	0x0	Bit [4]
HW_05_DEBUG	5	0x0	Bit [5]
HW_06_DEBUG	6	0x0	Bit [6]
HW_07_DEBUG	7	0x0	Bit [7]
HW_08_DEBUG	8	0x0	Bit [8]
HW_09_DEBUG	9	0x0	Bit [9]
HW_10_DEBUG	10	0x0	Bit [10]
HW_11_DEBUG	11	0x0	Bit [11]
HW_12_DEBUG	12	0x0	Bit [12]
HW_13_DEBUG	13	0x0	Bit [13]
HW_14_DEBUG	14	0x0	REGS_LC_NO_TSx_PAD_RCVD_DIS: Training sets can contain link and lane numbers set to PAD when transitioning from Polling.Active to Detect.Idle.
HW_15_DEBUG	15	0x0	REGS_LC_ALLOW_TX_L1_CONTROL: Allow TX to prevent LC from going to L1 when there are outstanding completions.
Hardware Debug Register			

PCIEP_PORT_CNTL - RW - 32 bits - PCIEIND_P:0x10			
Field Name	**Bits**	**Default**	**Description**
SLV_PORT_REQ_EN	0	0x1	Suspends all slave requests to client 0=Allow slave to be suspended 1=Ignore slave suspend signal
CI_SNOOP_OVERRIDE	1	0x0	Forces all slave requests to be snoop requests 0=Do not force all slave requests to be snoop requests 1=Force all slave requests to be snoop requests
HOTPLUG_MSG_EN	2	0x0	Enables hot-plug messages 0=Disable hot-plug messages 1=Enable hot-plug messages
NATIVE_PME_EN	3	0x1	Enables native PME 0=Disable native PME 1=Enable native PME
PWR_FAULT_EN	4	0x0	Enables power fault detection 0=Disable 1=Enable

PMI_BM_DIS	5	0x0	Disables bus master for power saving state 0=Normal 1=Disable
SEQNUM_DEBUG_MODE	6	0x0	Enables debug sequence number 0=Normal operation 1=Enable debug sequence number test mode
CI_SLV_CPL_STATIC_ALLOC_LIMIT_S	14:8	0x0	Limit for outstanding Slave Snooped Non-Posted request to Slave 0=128
CI_SLV_CPL_STATIC_ALLOC_LIMIT_NS	22:16	0x0	Limit for outstanding Slave Non-Snooped Non-Posted request to Slave 0=128
Port Control Register			

PCIE_TX_CNTL - RW - 32 bits - PCIEIND_P:0x20			
Field Name	**Bits**	**Default**	**Description**
TX_REPLAY_NUM_COUNT (R)	9:0	0x0	TX Replay Number Counter. Counter to keep track of the number of replays that have occured
TX_SNR_OVERRIDE	11:10	0x0	Snoop Not Required Override. Control of the Snoop bit for master requests 0=Generate bit as normal 1=Override equation, and always set bit 2=Override equation, and always clear bit 3=Invalid
TX_RO_OVERRIDE	13:12	0x0	Relaxed Ordering Override. Control relaxed ordering bit for master requests 0=Generate bit as normal 1=Override equation, and always set bit 2=Override equation, and always clear bit 3=Invalid
TX_PACK_PACKET_DIS	14	0x0	Packet Packing Disable. Back-to-back packing of TLP and DLLP 0=Place packets as close as allowable 1=Place STP/SDP in lane 0 only
TX_GAP_BTW_PKTS	18:16	0x0	Number of idle cycles between DLLP and TLP
TX_FLUSH_TLP_DIS	19	0x1	Disables flushing TLPs when Data Link is down 0=Normal 1=Disable
TX_CPL_PASS_P	20	0x1	Ordering rule: Let Completion Pass Posted 0=no pass 1=CPL pass
TX_NP_PASS_P	21	0x0	Ordering rule: Let Non-Posted Pass Posted 0=no pass 1=NP pass
TX_CLEAR_EXTRA_PM_REQS	22	0x1	Clears excess PM DLLPs from pipe 00=Traditional PM request behaviour 01=Clear PM DLLPs from pipe when link transactions from L1_Entry or L23_Entry to Rcv_L0
TX_FC_UPDATE_TIMEOUT_SEL	25:24	0x2	Adjusts the length of the timeout interval before sending out flow control update 0=Disable flow control 1=4x clock cycle 2=1024x clock cycle 3=4096x clock cycle
TX_FC_UPDATE_TIMEOUT	31:26	0x7	Interval length to send flow control update
TX Control Register			

PCIE_TX_REQUESTER_ID - RW - 32 bits - PCIEIND_P:0x21			
Field Name	**Bits**	**Default**	**Description**
TX_REQUESTER_ID_FUNCTION (R)	2:0	0x0	Function ID of Requester for Master transactions or Completer for Slave Completions
TX_REQUESTER_ID_DEVICE	7:3	0x0	Device ID of Requester for Master transactions or Completer for Slave Completions
TX_REQUESTER_ID_BUS	15:8	0x0	Bus ID of Requester for Master transactions or Completer for Slave Completions
TX Requester ID Register			

PCIE_TX_VENDOR_SPECIFIC - RW - 32 bits - PCIEIND_P:0x22			
Field Name	**Bits**	**Default**	**Description**
TX_VENDOR_DATA	23:0	0x0	Writing to this register generates a Vendor Specific DLLP using Vendor Data for the payload
TX Vendor Specific DLLP			

PCIE_TX_REQUEST_NUM_CNTL - RW - 32 bits - PCIEIND_P:0x23			
Field Name	**Bits**	**Default**	**Description**
TX_NUM_OUTSTANDING_NP	29:24	0x2	Number of Non-posted (VC0 and VC1) requests sent out before completion
TX_NUM_OUTSTANDING_NP_VC1_EN	30	0x0	Enable for number of Non-posted VC1 requests sent out before completion
TX_NUM_OUTSTANDING_NP_EN	31	0x0	Enable for number of Non-posted requests sent out before completion
TX Request Num Control Register			

PCIE_TX_SEQ - R - 32 bits - PCIEIND_P:0x24			
Field Name	**Bits**	**Default**	**Description**
TX_NEXT_TRANSMIT_SEQ	11:0	0x0	Next Transmit Sequence Number to send out
TX_ACKD_SEQ	27:16	0x0	Last Acknowledged Sequence Number
TX Sequence Register			

PCIE_TX_REPLAY - RW - 32 bits - PCIEIND_P:0x25			
Field Name	**Bits**	**Default**	**Description**
TX_REPLAY_NUM	9:0	0x3	Register to control Replay Number before Link goes to Retrain
TX_REPLAY_TIMER_OVERWRITE	15	0x0	Trigger for Replay Timer
TX_REPLAY_TIMER	31:16	0x90	Replay Timer. When expired do Replay
TX Replay Register			

PCIE_TX_ACK_LATENCY_LIMIT - RW - 32 bits - PCIEIND_P:0x26			
Field Name	**Bits**	**Default**	**Description**
TX_ACK_LATENCY_LIMIT	7:0	0x0	ACK Latency Limit for scheduling ACK DLLP transmission
TX_ACK_LATENCY_LIMIT_OVERWRITE	8	0x0	Use register value instead of hardware value from link width
TX ACK Latency Limit			

PCIE_TX_CREDITS_ADVT_P - R - 32 bits - PCIEIND_P:0x30			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_ADVT_PD	11:0	0x0	Posted data credits
TX_CREDITS_ADVT_PH	23:16	0x0	Posted header credits
Posted advertised credits			

PCIE_TX_CREDITS_ADVT_NP - R - 32 bits - PCIEIND_P:0x31			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_ADVT_NPD	11:0	0x0	Non-posted data credits
TX_CREDITS_ADVT_NPH	23:16	0x0	Non-posted header credits
Non-posted advertised credits			

PCIE_TX_CREDITS_ADVT_CPL - R - 32 bits - PCIEIND_P:0x32			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_ADVT_CPLD	11:0	0x0	Completion data credits
TX_CREDITS_ADVT_CPLH	23:16	0x0	Completion header credits
Completion advertised credits			

PCIE_TX_CREDITS_INIT_P - R - 32 bits - PCIEIND_P:0x33			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_INIT_PD	11:0	0x0	Posted data credits
TX_CREDITS_INIT_PH	23:16	0x0	Posted header credits
Posted initial credits			

PCIE_TX_CREDITS_INIT_NP - R - 32 bits - PCIEIND_P:0x34			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_INIT_NPD	11:0	0x0	Non-posted data credits
TX_CREDITS_INIT_NPH	23:16	0x0	Non-posted header credits
Non-posted initial credits			

PCIE_TX_CREDITS_INIT_CPL - R - 32 bits - PCIEIND_P:0x35			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_INIT_CPLD	11:0	0x0	Completion data credits
TX_CREDITS_INIT_CPLH	23:16	0x0	Completion header credits
Completion initial credits			

PCIE_TX_CREDITS_STATUS - RW - 32 bits - PCIEIND_P:0x36			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_ERR_PD	0	0x0	RW1C - Posted Data Credits Error
TX_CREDITS_ERR_PH	1	0x0	RW1C - Posted Header Credits Error
TX_CREDITS_ERR_NPD	2	0x0	RW1C - Non-posted Data Credits Error
TX_CREDITS_ERR_NPH	3	0x0	RW1C - Non-posted Header Credits Error
TX_CREDITS_ERR_CPLD	4	0x0	RW1C - Cpl Data Credits Error
TX_CREDITS_ERR_CPLH	5	0x0	RW1C - Cpl Header Credits Error
TX_CREDITS_CUR_STATUS_PD (R)	16	0x0	The current status of the posted data credits

TX_CREDITS_CUR_STATUS_PH (R)	17	0x0	The current status of the posted header credits
TX_CREDITS_CUR_STATUS_NPD (R)	18	0x0	The current status of the non-posted data credits
TX_CREDITS_CUR_STATUS_NPH (R)	19	0x0	The current status of the non-posted header credits
TX_CREDITS_CUR_STATUS_CPLD (R)	20	0x0	The current status of the cpl data credits
TX_CREDITS_CUR_STATUS_CPLH (R)	21	0x0	The current status of the cpl header credits
TX Credits status. When set to 1, remaining credits > init credits. Status bit will remain 1 until a 1 is written to it.			

PCIE_TX_CREDITS_FCU_THRESHOLD - RW - 32 bits - PCIEIND_P:0x37			
Field Name	**Bits**	**Default**	**Description**
TX_FCU_THRESHOLD_P_VC0	2:0	0x3	For VC0 posted header/data credits, fraction of (pending flow control updates / total flow control credits) before urgent DLLP flag is set. 0=0 1=1/16 2=1/8 3=1/4 4=1/2 5=3/4 6=7/8 7=1
TX_FCU_THRESHOLD_NP_VC0	6:4	0x3	For VC0 non-posted header/data credits, fraction of (pending flow control updates / total flow control credits) before urgent DLLP flag is set. 0=0 1=1/16 2=1/8 3=1/4 4=1/2 5=3/4 6=7/8 7=1
TX_FCU_THRESHOLD_CPL_VC0	10:8	0x3	For VC0 completion header/data credits, fraction of (pending flow control updates / total flow control credits) before urgent DLLP flag is set. 0=0 1=1/16 2=1/8 3=1/4 4=1/2 5=3/4 6=7/8 7=1
TX_FCU_THRESHOLD_P_VC1	18:16	0x3	For VC1 posted header/data credits, fraction of (pending flow control updates / total flow control credits) before urgent DLLP flag is set. 0=0 1=1/16 2=1/8 3=1/4 4=1/2 5=3/4 6=7/8 7=1

TX_FCU_THRESHOLD_NP_VC1	22:20	0x3	For VC1 non-posted header/data credits, fraction of (pending flow control updates / total flow control credits) before urgent DLLP flag is set. 0=0 1=1/16 2=1/8 3=1/4 4=1/2 5=3/4 6=7/8 7=1
TX_FCU_THRESHOLD_CPL_VC1	26:24	0x3	For VC1 completion header/data credits, fraction of (pending flow control updates / total flow control credits) before urgent DLLP flag is set. 0=0 1=1/16 2=1/8 3=1/4 4=1/2 5=3/4 6=7/8 7=1
TX Credits Flow Control Update Threshold			

PCIE_P_PORT_LANE_STATUS - RW - 32 bits - PCIEIND_P:0x50			
Field Name	**Bits**	**Default**	**Description**
PORT_LANE_REVERSAL (R)	0	0x0	Reverse lanes and control signals associated with a port 0=Port Lane order is normal 1=Port Lane order is reversed
PHY_LINK_WIDTH (R)	6:1	0x0	Link Width 0=6'b00_0000 disabled 1=6'b00_0001 x1 2=6'b00_0010 x2 3=6'b00_0100 x4 4=6'b00_1000 x8 5=6'b01_0000 x12 6=6'b10_0000 x16
Port-Lane Status Register			

PCIE_FC_P - RW - 32 bits - PCIEIND_P:0x60			
Field Name	**Bits**	**Default**	**Description**
PD_CREDITS	7:0	0x8	Posted Data Flow Control Advertised Credits
PH_CREDITS	15:8	0x2	Posted Header Flow Control Advertised Credits
Posted Flow Control Registers			

PCIE_FC_NP - RW - 32 bits - PCIEIND_P:0x61			
Field Name	**Bits**	**Default**	**Description**
NPD_CREDITS	7:0	0x2	Non-Posted Data Flow Control Advertised Credits
NPH_CREDITS	15:8	0x2	Non-Posted Header Flow Control Advertised Credits
Non-Posted Flow Control Registers			

PCIE_FC_CPL - RW - 32 bits - PCIEIND_P:0x62			
Field Name	**Bits**	**Default**	**Description**
CPLD_CREDITS	7:0	0x0	Completion Data Flow Control Credits
CPLH_CREDITS	15:8	0x0	Completion Header Flow Control Credits
Completion Flow Control Registers			

PCIE_ERR_CNTL - RW - 32 bits - PCIEIND_P:0x6A			
Field Name	**Bits**	**Default**	**Description**
ERR_REPORTING_DIS	0	0x0	Disables PCI Express Advanced Error Reporting
TX_GENERATE_LCRC_ERR (W)	4	0x0	Generates LCRC error for the next transmitted TLP.
RX_GENERATE_LCRC_ERR (W)	5	0x0	Generates LCRC error for the next received TLP.
TX_GENERATE_ECRC_ERR (W)	6	0x0	Generates ECRC error for the next transmitted TLP.
RX_GENERATE_ECRC_ERR (W)	7	0x0	Generates ECRC error for the next received TLP.
Error Control Registers			

PCIE_RX_CNTL - RW - 32 bits - PCIEIND_P:0x70			
Field Name	**Bits**	**Default**	**Description**
RX_IGNORE_IO_ERR	0	0x1	Ignore Malformed I/O TLP Errors
RX_IGNORE_BE_ERR	1	0x1	Ignore Malformed Byte Enable TLP Errors
RX_IGNORE_MSG_ERR	2	0x1	Ignore Malformed Message Error
RX_IGNORE_CRC_ERR	3	0x0	Ignore CRC Errors
RX_IGNORE_CFG_ERR	4	0x1	Ignore Malformed Configuration Errors
RX_IGNORE_CPL_ERR	5	0x1	Ignore Malformed Completion Errors
RX_IGNORE_EP_ERR	6	0x1	Ignore EP Errors
RX_IGNORE_LEN_MISMATCH_ERR	7	0x1	Ignore Malformed Length Mismatch Errors
RX_IGNORE_MAX_PAYLOAD_ERR	8	0x1	Ignore Malformed Maximum Payload Errors
RX_IGNORE_TC_ERR	9	0x1	Ignore Malformed Traffic Class Errors
RX_IGNORE_CFG_UR	10	0x1	Reserved
RX_IGNORE_IO_UR	11	0x0	Reserved
RX_IGNORE_VEND0_UR	12	0x0	Ignore ATS translation request Malformed Format Error
RX_NAK_IF_FIFO_FULL	13	0x0	Send NAK if RX internal FIFO is full
RX_GEN_ONE_NAK	14	0x1	Generate NAK only for the first bad packet until replayed
RX_FC_INIT_FROM_REG	15	0x0	Flow Control Initialization from registers 0=Init FC from FIFO sizes 1=Init FC from registers
RX_RCB_CPL_TIMEOUT	18:16	0x0	RCB cpl timeout 0=Disable 1=50us 2=10ms 3=25ms 4=50ms 5=100ms 6=500ms 7=1ms
RX_RCB_CPL_TIMEOUT_MODE	19	0x0	RCB cpl timeout on link down
RX_PCIE_CPL_TIMEOUT_DIS	20	0x0	
Reserved	31:21		Reserved
RX Control Register			

PCIE_RX_EXPECTED_SEQNUM - R - 32 bits - PCIEIND_P:0x71			
Field Name	**Bits**	**Default**	**Description**
RX_EXPECTED_SEQNUM	11:0	0x0	Next Expected sequence number
RX Next Expected Sequence Number Register			

PCIE_RX_VENDOR_SPECIFIC - R - 32 bits - PCIEIND_P:0x72			
Field Name	**Bits**	**Default**	**Description**
RX_VENDOR_DATA	23:0	0x0	Writing to this register will re-arm to capture the next Vendor Specific DLLP
RX_VENDOR_STATUS	24	0x0	Indicates that a Vendor Specific DLLP was decoded, and Vendor Data was captured
RX Vendor Specific DLLP			

PCIE_RX_CREDITS_ALLOCATED_P - R - 32 bits - PCIEIND_P:0x80			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_ALLOCATED_PD	11:0	0x0	For posted TLP data, the number of FC units granted to transmitter since initialization, modulo 4096
RX_CREDITS_ALLOCATED_PH	23:16	0x0	For posted TLP header, the number of FC units granted to transmitter since initialization, modulo 256
RX Credits Allocated Register (Posted)			

PCIE_RX_CREDITS_ALLOCATED_NP - R - 32 bits - PCIEIND_P:0x81			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_ALLOCATED_NPD	11:0	0x0	For non-posted TLP data, the number of FC units granted to transmitter since initialization, modulo 4096
RX_CREDITS_ALLOCATED_NPH	23:16	0x0	For non-posted TLP header, the number of FC units granted to transmitter since initialization, modulo 256
RX Credits Allocated Register (Non-Posted)			

PCIE_RX_CREDITS_ALLOCATED_CPL - R - 32 bits - PCIEIND_P:0x82			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_ALLOCATED_CPLD	11:0	0x0	For completion TLP data, the number of FC units granted to transmitter since initialization, modulo 4096
RX_CREDITS_ALLOCATED_CPLH	23:16	0x0	For completion TLP header, the number of FC units granted to transmitter since initialization, modulo 256
RX Credits Allocated Register (Completion)			

PCIE_RX_CREDITS_RECEIVED_P - R - 32 bits - PCIEIND_P:0x83			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_RECEIVED_PD	11:0	0x0	For posted TLP data, the number of FC units consumed by valid TLP received since initialization, modulo 4096
RX_CREDITS_RECEIVED_PH	23:16	0x0	For posted TLP header, the number of FC units consumed by valid TLP received since initialization, modulo 256
RX Credits Received Register (Posted)			

PCIE_RX_CREDITS_RECEIVED_NP - R - 32 bits - PCIEIND_P:0x84			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_RECEIVED_NPD	11:0	0x0	For non-posted TLP data, the number of FC units consumed by valid TLP received since initialization, modulo 4096
RX_CREDITS_RECEIVED_NPH	23:16	0x0	For non-posted TLP header, the number of FC units consumed by valid TLP received since initialization, modulo 256
RX Credits Received Register (Non-Posted)			

PCIE_RX_CREDITS_RECEIVED_CPL - R - 32 bits - PCIEIND_P:0x85			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_RECEIVED_CPLD	11:0	0x0	For completion TLP data, the number of FC units consumed by valid TLP received since initialization, module 4096
RX_CREDITS_RECEIVED_CPLH	23:16	0x0	For completion TLP header, the number of FC units consumed by valid TLP received since initialization, module 256
RX Credits Received Register (Completion)			

PCIE_LC_CNTL - RW - 32 bits - PCIEIND_P:0xA0			
Field Name	**Bits**	**Default**	**Description**
LC_CM_HI_ENABLE_COUNT	0	0x0	Enables count for CM_HIGH. When transmitter is to be turned on stop when the counter reaches CM_HI_COUNT_LIMIT_ON. If the number of lanes = 1 or 2: CM_HI_COUNT_LIMIT_ON = 12 or 10. If number of lanes = 3 or 4: CM_HI_COUNT_LIMIT_ON = 10 or 12. If number of lanes > 4: CM_HI_COUNT_LIMIT_ON = 10 or 15.
LC_DONT_ENTER_L23_IN_D0	1	0x0	Do not enter L23 in D0 state.
LC_RESET_L_IDLE_COUNT_EN	2	0x0	Enables reset of electrical idle counter.
LC_RESET_LINK	3	0x0	Resets an individual link without resetting the other ports.
LC_16X_CLEAR_TX_PIPE	7:4	0x5	Adjusts the time that the LC waits for the pipe to be idle. Setting this field to 0 results in the maximum time. Otherwise, the delay increases as this field is incremented.
LC_L0S_INACTIVITY	11:8	0x0	L0s inactivity timer setting 0=L0s is disabled 1=40ns 2=80ns 3=120ns 4=200ns 5=400ns 6=1us 7=2us 8=4us 9=10us 10=40us 11=100us 12=400us 13=1ms 14=4ms
LC_L1_INACTIVITY	15:12	0x0	L1 inactivity timer setting 0=L1 is disabled 1=1us 2=2us 3=4us 4=10us 5=20us 6=40us 7=100us 8=400us 9=1ms 10=4ms 11=10ms 12=40ms 13=100ms 14=400ms

LC_PMI_TO_L1_DIS	16	0x0	Disables the transition to L1 caused by programming PMI_STATE to non-D0
LC_INC_N_FTS_EN	17	0x0	Enables incrementing N_FTS for each transition to recovery
LC_LOOK_FOR_IDLE_IN_L1L23	19:18	0x0	Controls the number of clocks to wait for Electrical Idle set in L1, L23 0=250 1=100 2=10000 3=3000000
LC_FACTOR_IN_EXT_SYNC	20	0x0	Factors in the extended sync bit in the calculation for the replay timer adjustment
LC_WAIT_FOR_PM_ACK_DIS	21	0x0	Disables waiting for PM_ACK in L23 ready entry handshake
LC_WAKE_FROM_L23	22	0x0	For upstream component, wake the link from L23 ready
LC_L1_IMMEDIATE_ACK	23	0x0	Always ACK an ASPM L1 entry DLLP (ie. never generate PM_NAK)
LC_ASPM_TO_L1_DIS	24	0x0	Disables ASPM L1
LC_DELAY_COUNT	26:25	0x0	Controls minimum amount of time to stay in L0s or L1 0=255/ 4095 (Power-down) 1=1250 / 16383 (Power-down) 2=5000/ 65535 (Power-down) 3=25000 / 262143 (Power-down)
LC_DELAY_L0S_EXIT	27	0x0	Enables staying in L0s for a minimum time
LC_DELAY_L1_EXIT	28	0x0	Enables staying in L1 for a minimum time
LC_EXTEND_WAIT_FOR_EL_IDLE	29	0x1	Waits for Electrical idle in L1/L23 ready value
LC_ESCAPE_L1L23_EN	30	0x1	Enables L1/L23 entry escape arcs
LC_GATE_RCVR_IDLE	31	0x0	Ignores PHY Electrical idle detector 0=LC will look for PE_LC_IdleDetected 1=To gate off PE_LC_IdleDetected to LC, so that LC never sees receivers enter EIDLE
Link Control Register			

PCIE_LC_TRAINING_CNTL - RW - 32 bits - PCIEIND_P:0xA1			
Field Name	**Bits**	**Default**	**Description**
LC_TRAINING_CNTL	3:0	0x0	Training control bits in training sets 0=Reserved 1=Disable Link 2=Loopback 3=Disable Scrambling. The training control signal will be asserted in the TS when the associated bit is set to 1.
LC_COMPLIANCE_RECEIVE	4	0x0	Control for the Compliance Receive bit in Training Sequence 1 Ordered Sets.
LC_LOOK_FOR_MORE_NON_MATCHING_TS1	5	0x0	Looks for more non-mataching TS1 ordered sets.
LC_L0S_L1_TRAINING_CNTL_EN	6	0x0	Enables the transition from L0s & L1 to Recovery if a Hot Reset or Link Disable is initiated.
LC_L1_LONG_WAKE_FIX_EN	7	0x1	Enables fix for FTS going to L1 problem
LC_POWER_STATE (R)	10:8	0x0	Link Power state
LC_DONT_GO_TO_L0S_IF_L1_ARMED	11	0x0	Prevents the LTSSM from going to Rcv_L0s if it has already acknowledged a request to go to L1 but it hasn't transitioned there yet.
LC_INIT_SPD_CHG_WITH_CSR_EN	12	0x1	Controls PCIe® 2.0 clause that states that directed_speed_change should be set if the Retrain Link bit is set to 1 and the Target Link Speed is not equal to the current link speed. 0=Speed negotiation will not be initiated by RETRAIN_LINK Configuration bit. 1=Speed Negotiation can be initiated if RETRAIN_LINK is set and Target Link Speed does not equal the current link speed.

LC_EXTEND_WAIT_FOR_SKP	16	0x1	Extends the timer when in Rcv_L0s_Skp state. Bit is inverted before being used.
LC_AUTONOMOUS_CHANGE_OFF	17	0x0	'Autonomous Change' Data Rate Identifier Control 0='Autonomous Change' is reported as defined in the PCIe 2.0 specification. 1=Do not report 'Autonomous Change'.
LC_UPCONFIGURE_CAP_OFF	18	0x0	'Upconfigurat Capability' Data Rate Identifier Control 0='Upconfigure Capability' is reported as defined in the PCIe 2.0 specification. 1=Do not report 'Upconfigure Capability'.
LC_HW_LINK_DIS_EN	19	0x0	Control for the HW or Chip-induced Link Disable feature. Applies to RC only. 0=Turn off chip-induced Link Disable. 1=Allow chip to force link to Link Disable.
LC_LINK_DIS_BY_HW	20	0x0	HW or Chip-induced Link Disable status. Note that this bit is Sticky & RW1C. 0=Chip forced Link to the Link Disable state. 1=Chip-induced Link Disable cleared or never happened.
LC_STATIC_TX_PIPE_COUNT_EN	21	0x0	Use the same WAIT_FOR_EMPTY_PIPE values for all link widths when going to L1 or L23.
LC_ASPM_L1_NAK_TIMER_SEL	23:22	0x0	Select timer value to be used when a request to go to L1 is declined i.e. NAK is sent. 0=9.5us 1=3.2us 2=1.6us 3=0.8us
LC_DONT_DEASSERT_RX_EN_IN_R_SPEED	24	0x0	Prevents the deassertion of RX_EN during Recovery.Speed.
LC_DONT_DEASSERT_RX_EN_IN_TEST	25	0x0	Prevents the deassertion of RX_EN during Polling.Compliance and Loopback.
LC_RESET_ASPM_L1_NAK_TIMER	26	0x1	Prevent L1 Nak Counter from being continuously reset before it has expired (i.e. reached 9.5us) if additional ASPM L1 requests received. 0=Don't reset the 9.5us L1 Nak Counter if additional ASPM L1 requests received. 1=Reset the 9.5us L1 Nak Counter if additional ASPM L1 requests received before counter finishes.
LC_DEBUG_1	27	0x0	Added this bit in case fields needed after registers are frozen.
LC_DEBUG_2	28	0x0	Added this bit in case fields needed after registers are frozen.
LC_DEBUG_3	29	0x0	Added this bit in case fields needed after registers are frozen.
LC_DEBUG_4	30	0x0	Added this bit in case fields needed after registers are frozen.
LC_DEBUG_5	31	0x0	Enable Skip common mode detection ECO
LC Training Control Register			

PCIE_LC_LINK_WIDTH_CNTL - RW - 32 bits - PCIEIND_P:0xA2			
Field Name	**Bits**	**Default**	**Description**
LC_LINK_WIDTH	2:0	0x6	Link width required.
LC_LINK_WIDTH_RD (R)	6:4	0x0	Read back link width
LC_RECONFIG_ARC_MISSING_ESCAPE	7	0x0	Expedites the transition from Recovery.Idle to Detect during a long reconfiguration.
LC_RECONFIG_NOW	8	0x0	Initiates link width change.
LC_RENEGOTIATION_SUPPORT (R)	9	0x0	Advertises link width renegotiation support. 0=Other end does not support link width renegotiation. 1=Other end does support link width renegotiation.
LC_RENEGOTIATE_EN	10	0x0	Enables re-negotiation.
LC_SHORT_RECONFIG_EN	11	0x0	Enables short reconfiguration.
LC_UPCONFIGURE_SUPPORT	12	0x0	Control for the PCIe® 2.0 defined link width change.
LC_UPCONFIGURE_DIS	13	0x0	Overrides all other control signals of the PCIe 2.0 defined link width change feature.

LC_UPCFG_WAIT_FOR_RCVR_DIS	14	0x0	Disables waiting for all receivers during a link width upconfigure. 0=Enable 1=Disable
LC_UPCFG_TIMER_SEL	15	0x0	Time that state machine waits to receive TS on all receivers during a link width upconfigure. 0=1 msec 1=use LC_WAIT_FOR_LANES_IN_LW_NEG values
LC_DEASSERT_TX_PDNB	16	0x0	TX_PDNB Control for unused lanes 0=Keep TX_PDNB asserts for unused lanes. 1=Deassert TX_PDNB for unused lanes
LC_L1_RECONFIG_EN	17	0x0	Control for link width change in L1 state. 0=Link width reconfiguration can not be initiated from L1. 1=Link width reconfiguration can be initiated from L1.
LC_DYNLINK_MST_EN	18	0x0	HW initiated link width change feature. 0=Disable 1=Enable HW initiated link width change interface
LC_DUAL_END_RECONFIG_EN	19	0x0	Control Link Width Reconfiguration so that either end is allowed to initiate a link width change to the maximum supported width when the other end has initiated a change to a smaller link width. 0=Allow single end link reconfiguration 1=Allow link width reconfiguration to be simultaneously initiated by either end of the Link
LC_UPCONFIGURE_CAPABLE (R)	20	0x0	Represents upconfigure_capable variable defined in the PCIe 2.0 specification. 0=PCIe 2.0 Upconfigure feature NOT supported by both ends. 1=PCIe 2.0 Upconfigure feature IS supported by both ends of the Link.
Link Width Control			

PCIE_LC_N_FTS_CNTL - RW - 32 bits - PCIEIND_P:0xA3			
Field Name	**Bits**	**Default**	**Description**
LC_XMIT_N_FTS	7:0	0xc	Number of FTS to override the strap value
LC_XMIT_N_FTS_OVERRIDE_EN	8	0x0	Enables the previous field to override the strap value.
LC_XMIT_FTS_BEFORE_RECOVERY	9	0x1	Transmits FTS before Recovery.
LC_XMIT_N_FTS_LIMIT	23:16	0xff	The limit that the number of FTS can increment to when incrementing is enabled.
LC_N_FTS (R)	31:24	0x0	Number of FTS captured from the other end of the link.
LC Number of FTS Control			

PCIE_LC_SPEED_CNTL - RW - 32 bits - PCIEIND_P:0xA4			
Field Name	**Bits**	**Default**	**Description**
LC_GEN2_EN_STRAP	0	0x0	PCIe® Generation 2 enable bit. Strap Loadable. 0=Gen1 only support. 1=Gen2 supported.
LC_TARGET_LINK_SPEED_OVERRIDE_EN	1	0x0	Enables the overriding of the Target Link Speed configuration register. 0=Disable override. 1=Override Target Link Speed with LC_TARGET_LINK_SPEED_OVERRIDE.
LC_TARGET_LINK_SPEED_OVERRIDE	2	0x0	Value used instead of Target Link Speed when override enable is set. 0=Gen2 not supported when override is enabled. 1=Gen2 supported when override is enabled.

LC_FORCE_EN_SW_SPEED_CHANGE	3	0x0	Forces the bif_core to allow speed changes initiated by private registers.
LC_FORCE_DIS_SW_SPEED_CHANGE	4	0x0	Disables speed changes initiated by the bif_core private registers.
LC_FORCE_EN_HW_SPEED_CHANGE	5	0x0	Forces the bif_core to allow speed changes initiated by the chip interface (based on voltage levels).
LC_FORCE_DIS_HW_SPEED_CHANGE	6	0x1	Disables speed changes initiated by the chip interface (based on voltage levels).
LC_INITIATE_LINK_SPEED_CHANGE	7	0x0	Initiates speed negotiation when allowed by the register settings.
LC_SPEED_CHANGE_ATTEMPTS_ALLOWED	9:8	0x0	Determines the number of speed change attempts that are allowed.
LC_SPEED_CHANGE_ATTEMPT_FAILED (R)	10	0x0	Number of speed change attempts allowed has been reached. This bit and the related counter can be cleared using the LC_CLR_FAILED_SPD_CHANGE_CNT bit.
LC_CURRENT_DATA_RATE (R)	11	0x0	Current data rate of the Link. 0=Gen1 1=Gen2
LC_HW_VOLTAGE_IF_CONTROL	13:12	0x0	Controls the chip/bif_core speed control interface. 0=Ignore CHIP/BIF voltage interface. Voltage level is always assumed to be high. 1=CHIP/BIF voltage interface is enabled. 2=CHIP only allowed to lower or raise the voltage when the BIF is running at Gen1 data rate. CHIP must be running at high voltage if BIF is running at Gen2 data rate.
LC_VOLTAGE_TIMER_SEL	17:14	0xa	Controls the circuit that filters noise out of the chip/bif_core voltage interface. 0=No Delay. 1=10ns 2=100ns 3=1us 4=10us 5=100us 6=1ms 7=10ms 8=100ms 9=500ms 10=1sec 11=2sec 12=5sec 13=10sec 14=15sec 15=20sec
LC_GO_TO_RECOVERY	18	0x0	Forces the Link to Recovery. Only applicable when link in L0 state.
LC_N_EIE_SEL	19	0x0	Selects the number of EIE (K28.7) symbols that are going to be sent when running at Gen2 speed and the link is exiting L0s. 0=Send 4 EIE (K28.7) symbols before transmitting FTS when exiting L0s at Gen2 speed. 1=Send 8 EIE (K28.7) symbols before transmitting FTS when exiting L0s at Gen2 speed.
LC_DONT_CLR_TARGET_SPD_CHANGE_STATUS	20	0x0	Autonomous speed change control after a speed change attempt has failed. 0=Clear speed negotiation failure initiated by Target Link Speed in Detect. 1=Speed negotiation failure initiated by Target Link Speed is only allowed to fail once.

LC_CLR_FAILED_SPD_CHANGE_CNT	21	0x0	Clears the LC_SPEED_CHANGE_ATTEMPT_FAILED field when a '1' is written to it. 0=No Change 1=Clear LC_SPEED_CHANGE_ATTEMPT_FAILED register bit so that more SW or HW(Voltage) initiated speed negotiations can be initiated.
LC_1_OR_MORE_TS2_SPEED_ARC_EN	22	0x0	Enables the transition from Recovery.RcvrCfg to Recovery.Speed when more than 1, but not all, 8 TS2s (with required parameters for a speed change) are received. 0=Don't allow transition from Recovery.RcvrCfg to Recovery.Speed if 1 to 7 TS2s are received. 1=Allow the the transition from Recovery.RcvrCfg to Recovery.Speed if 1 to 7 TS2s with speed_change are received.
LC_OTHER_SIDE_EVER_SENT_GEN2 (R)	23	0x0	Cumulative 5.0GT/s capability of the other end of the Link. 0=Other side of link has never advertised that it supports Gen2. 1=Other side of the link has ever advertised that it supports Gen2 - although it may not currently support Gen2.
LC_OTHER_SIDE_SUPPORTS_GEN2 (R)	24	0x0	Current 5.0GT/s capability of the other end of the Link. 0=Other side of the link does not currently advertise that it supports Gen2. 1=Other side of the link currently supports Gen2.
LC_AUTO_RECOVERY_DIS	25	0x1	Autonomous control of the speed advertised after a voltage change. 0=Automatically go to Recovery in order to advertise that a change in Gen2 support has occured due to a voltage increase. 1=Do not automatically go to Recovery.
LC_SPEED_CHANGE_STATUS	26	0x0	This will gate a HW (i.e. voltage) initiated change to Gen2 when set to 1. 0=No status. 1=Tried to change to Gen2 speed and other end refused. Asserted when the other side no longer supports Gen2.
LC_DATA_RATE_ADVERTISED (R)	27	0x0	Data rate advertised by the port. 0=Only Gen1 support advertised. 1=Gen2 support advertised.
LC_CHECK_DATA_RATE	28	0x1	Determines if the LC is going to check the DATA RATE symbol if the LC_GEN2_EN_STRAP bit is not set. 0=Only check the DATA RATE identifiers when Gen2 is supported. 1=Always check the DATA RATE identifiers regardless of Gen2.
LC_MULT_UPSTREAM_AUTO_SPD_CHNG_EN	29	0x0	Allows the upstream component to initiate speed changes to the highest link speed supported by both ends of the link. Note that multiple speed changes are only allowed if there aren't any failures in previous speed change attempts. Note: STRAP_BIF_AUTO_RC_SPEED_NEGOTIATION_DIS must be 0. 0=The upstream component will only try to automatically change the link to the highest link speed supported by both ends once - regardless of whether the change is successful or not. 1=The upstream component can automatically initiate multiple speed changes.
LC_INIT_SPEED_NEG_IN_L0s_EN	30	0x0	Speed negotiation during L0s control. 0=Do not allow a speed change to be initialized when in the L0s state. 1=Allow speed change negotiations to be initialized from L0s.

LC_INIT_SPEED_NEG_IN_L1_EN	31	0x0	Speed negotiation during L1 control. 0=Do not allow a speed change to be initialized when in the L1 state. 1=Allow speed change negotiations to be initialized from L1.
Data Rate Control			

PCIE_LC_STATE0 - R - 32 bits - PCIEIND_P:0xA5			
Field Name	**Bits**	**Default**	**Description**
LC_CURRENT_STATE	5:0	0x0	Current LC State
LC_PREV_STATE1	13:8	0x0	1st Previous LC State
LC_PREV_STATE2	21:16	0x0	2nd Previous LC State
LC_PREV_STATE3	29:24	0x0	3rd Previous LC State
Link Control State Register			

PCIE_LC_STATE1 - R - 32 bits - PCIEIND_P:0xA6			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE4	5:0	0x0	4th Previous LC State
LC_PREV_STATE5	13:8	0x0	5th Previous LC State
LC_PREV_STATE6	21:16	0x0	6th Previous LC State
LC_PREV_STATE7	29:24	0x0	7th Previous LC State
Link Control State Register			

PCIE_LC_STATE2 - R - 32 bits - PCIEIND_P:0xA7			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE8	5:0	0x0	8th Previous LC State
LC_PREV_STATE9	13:8	0x0	9th Previous LC State
LC_PREV_STATE10	21:16	0x0	10th Previous LC State
LC_PREV_STATE11	29:24	0x0	11th Previous LC State
Link Control State Register			

PCIE_LC_STATE3 - R - 32 bits - PCIEIND_P:0xA8			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE12	5:0	0x0	12th Previous LC State
LC_PREV_STATE13	13:8	0x0	13th Previous LC State
LC_PREV_STATE14	21:16	0x0	14th Previous LC State
LC_PREV_STATE15	29:24	0x0	15th Previous LC State
Link Control State Register			

PCIE_LC_STATE4 - R - 32 bits - PCIEIND_P:0xA9			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE16	5:0	0x0	16th Previous LC State
LC_PREV_STATE17	13:8	0x0	17th Previous LC State
LC_PREV_STATE18	21:16	0x0	18th Previous LC State
LC_PREV_STATE19	29:24	0x0	19th Previous LC State
Link Control State Register			

PCIE_LC_STATE5 - R - 32 bits - PCIEIND_P:0xAA			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE20	5:0	0x0	20th Previous LC State
LC_PREV_STATE21	13:8	0x0	21st Previous LC State
LC_PREV_STATE22	21:16	0x0	22nd Previous LC State
LC_PREV_STATE23	29:24	0x0	23rd Previous LC State
Link Control State Register			

PCIE_LC_CNTL2 - RW - 32 bits - PCIEIND_P:0xB1			
Field Name	**Bits**	**Default**	**Description**
LC_TIMED_OUT_STATE (R)	5:0	0x0	States that the LC was in when the deadman timer expired.
LC_STATE_TIMED_OUT	6	0x0	Deadman timer expired.
LC_LOOK_FOR_BW_REDUCTION	7	0x1	Enables check for bandwidth change when reporting Link Bandwidth Notification Status. 0=Do not check if bandwidth was reduced. 1=Check if bandwidth was reduced.
LC_MORE_TS2_EN	8	0x0	Sends out 128 sets instead of 16.
LC_X12_NEGOTIATION_DIS	9	0x1	Disables x12 negotiation.
LC_LINK_UP_REVERSAL_EN	10	0x0	Allows reversal for a wider width in link up.
LC_ILLEGAL_STATE	11	0x0	The LC is in an illegal state.
LC_ILLEGAL_STATE_RESTART_EN	12	0x0	Enables the LC to be restarted when it is in an illegal state.
LC_WAIT_FOR_OTHER_LANES_MODE	13	0x0	Eliminates delay introduced by waiting for other lanes. 0=Timer based 1=Identical Training Set based
LC_ELEC_IDLE_MODE	15:14	0x0	Electrical Idle Mode for LC. 0=GEN1 - entry:PHY, exit:PHY; GEN2 - entry:infer, exit:PHY 1=GEN1 - entry:infer, exit:PHY; GEN2 - entry:infer, exit PHY 2=GEN1 - entry:PHY, exit:PHY; GEN2 - entry:PHY, exit:PHY 3=Reserved
LC_DISABLE_INFERRED_ELEC_IDLE_DET	16	0x0	Disables Inferred Electrical Idle detection. 0=Inferred Electrical Idle Detection is enabled 1=Inferred Electrical Idle Detection is disabled
LC_ALLOW_PDWN_IN_L1	17	0x0	Sets the BIF_CHIP_CLK_PDWN output to 1 when the LC is in the L1 state.
LC_ALLOW_PDWN_IN_L23	18	0x0	Sets the BIF_CHIP_CLK_PDWN output to 1 when the LC is in the L23_Ready state.
LC_DEASSERT_RX_EN_IN_L0S	19	0x0	Turns off transmitters when the link is in L0s.
LC_BLOCK_EL_IDLE_IN_L0	20	0x0	Prevents the Electrical Idle from causing a transition from Rcv_L0 to Rcv_L0s.
LC_RCV_L0_TO_RCV_L0S_DIS	21	0x0	Disables transition from Rcv_L0 to Rcv_L0s
LC_ASSERT_INACTIVE_DURING_HOLD	22	0x0	Asserts the INACTIVE_LANES signals when CHIP_BIF_hold_training is high.
LC_WAIT_FOR_LANES_IN_LW_NEG	24:23	0x0	Mode used to wait for TS on all lanes in link width negotiation.
LC_PWR_DOWN_NEG_OFF_LANES	25	0x1	Powers down unused lanes
LC_DISABLE_LOST_SYM_LOCK_ARCS	26	0x1	Control transition to Recovery.RcvrLock from Configuration.Idle or Recovery.Idle when a training set is received. It is similar to the ‘idle_to_rlock_transitioned’ variable.
LC_LINK_BW_NOTIFICATION_DIS	27	0x0	Control for the Link Bandwidth Notification Feature.
LC_ENABLE_RX_CR_EN_DEASSERTION	28	0x0	Enables the deassertion of PG2RX_CR_EN to lock clock recovery parameter when lane is in electrical idle 0=CR_EN is always asserted 1=CR_EN is deasserted when RX_EN is deasserted during L0s/L1 and inactive lanes

LC_TEST_TIMER_SEL	30:29	0x0	State timeout select 0=LTSSM uses spec compliant timeout values. 1=LTSSM uses simulation timeout values. 2=LTSSM uses decreased timeout values for lab testing. 3=Reserved
LC_ENABLE_INFERRED_ELEC_IDLE_FOR_PI	31	0x1	Enables Inferred Electrical Idle Detection for PI (Physical Layer blocks) 0=Inferred Electrical Idle Detection is disabled for PI (Physical Layer block) 1=Inferred Electrical Idle Detection is enabled for PI (Physical Layer block)
Link Control Register 2			

PCIE_LC_BW_CHANGE_CNTL - RW - 32 bits - PCIEIND_P:0xB2			
Field Name	**Bits**	**Default**	**Description**
LC_BW_CHANGE_INT_EN	0	0x0	Enables Interrupt when the link bandwidth changes.
LC_HW_INIT_SPEED_CHANGE (R)	1	0x0	Link speed changed due to a hardware initiated speed negotiation.
LC_SW_INIT_SPEED_CHANGE (R)	2	0x0	Link speed changed due to a software initiated speed negotiation.
LC_OTHER_INIT_SPEED_CHANGE (R)	3	0x0	Link speed changed due to a speed negotiation initiated by the other end of the link.
LC_RELIABILITY_SPEED_CHANGE (R)	4	0x0	Link speed changed due to a reliability issue at the current speed.
LC_FAILED_SPEED_NEG (R)	5	0x0	Link speed change failed and link speed was reverted to initial speed.
LC_LONG_LW_CHANGE (R)	6	0x0	Link width was changed due to a long dynamic link width reconfiguration.
LC_SHORT_LW_CHANGE (R)	7	0x0	Link width was changed due to a short dynamic link width reconfiguration.
LC_LW_CHANGE_OTHER (R)	8	0x0	Link width changed and the change was initiated by the other end of the link.
LC_LW_CHANGE_FAILED (R)	9	0x0	Link width change was initiated by the width was not changed.
LC_LINK_BW_NOTIFICATION_DETECT_MODE	10	0x0	Control Link Bandwidth Management for speed changes in Detect. 0=Disable Link Bandwidth Management Capabilities in Detect. 1=Update LINK_BW_MANAGEMENT_STATUS when speed changes in Detect.
LC Bandwidth Change Notification Control Register			

PCIE_LC_CDR_CNTL - RW - 32 bits - PCIEIND_P:0xB3			
Field Name	**Bits**	**Default**	**Description**
LC_CDR_TEST_OFF	11:0	0x60	Enables CDR Test Mode
LC_CDR_TEST_SETS	23:12	0x18	Selects the number of sets that are transmitted during CDR test mode.
LC_CDR_SET_TYPE	25:24	0x1	Selects the type of set that is transmitted during CDR test mode
CDR Control Register			

PCIE_LC_LANE_CNTL - RW - 32 bits - PCIEIND_P:0xB4			
Field Name	**Bits**	**Default**	**Description**
LC_CORRUPTED_LANES (R)	15:0	0x0	Each bit indicates if that associated lane had trouble during training.

LC_LANE_DIS	31:16	0x0	Permanently disable associated lane.
Lane Status and Control Register			

PCIE_LC_CNTL3 - RW - 32 bits - PCIEIND_P:0xB5			
Field Name	**Bits**	**Default**	**Description**
LC_SELECT_DEEMPHASIS	0	0x0	Downstream De-Emphasis 0 = -6dB De-emphasis required. 1 = -3.5dB De-emphasis required.
LC_SELECT_DEEMPHASIS_CNTL	2:1	0x0	Upstream De-Emphasis control 0=Use De-emphasis from CSR. 1=Use De-emphasis from downstream component. 2=Use -6dB De-emphasis. 3=Use -3.5dB De-emphasis.
LC_RCVD_DEEMPHASIS (R)	3	0x0	De-emphasis setting advertised by other end.
LC_COMP_TO_DETECT	4	0x0	Modified Compliance Pattern control 0=No action taken. 1=Transition LTSSM from Polling.Compliance to Detect if sending out Modified Compliance Pattern due to receipt of TS1s.
LC_RESET_TSX_CNT_IN_RLOCK_EN	5	0x1	TS Ordered Set Counter Control in Recovery.RcvrLock 0=No change in Training Sequence counter when DIRECTED_SPEED_CHANGE asserted in Recovery.RcvrLock. 1=Reset Training Sequence counter when DIRECTED_SPEED_CHANGE is asserted in Recovery.RcvrLock.
LC_AUTO_SPEED_CHANGE_ATTEMPTS_ALLOWED	7:6	0x0	Number of unsuccessful Autonomous Speed Changes that are allowed. N/A for downstream components. 0=1 1=2 2=3 3=4
LC_AUTO_SPEED_CHANGE_ATTEMPT_FAILED (R)	8	0x0	Number of maximum unsuccessful Autonomous Speed Change attempts reached. N/A for downstream components. 0=Autonomous changes by RC allowed. 1=Maximum allowable number of autonomous speed changes reached.
LC_CLR_FAILED_AUTO_SPD_CHANGE_CNT	9	0x0	Clear Autonomous Speed Change counter. N/A for downstream components. 0=No action taken. 1=Clear LC_AUTO_SPEED_CHANGE_ATTEMPT_FAILED register bit so that the RC can autonomously initiate more speed negotiations.
Link Control Register 3			

PCIEP_STRAP_LC - RW - 32 bits - PCIEIND_P:0xC0			
Field Name	**Bits**	**Default**	**Description**
STRAP_FTS_yTSx_COUNT	1:0	0x0	Provides an override for STRAP_FTS_yTSx_COUNT
STRAP_LONG_yTSx_COUNT	3:2	0x0	Provides an override for STRAP_LONG_yTSx_COUNT
STRAP_MED_yTSx_COUNT	5:4	0x0	Provides an override for STRAP_MED_yTSx_COUNT
STRAP_SHORT_yTSx_COUNT	7:6	0x0	Provides an override for STRAP_SHORT_yTSx_COUNT
STRAP_SKIP_INTERVAL	10:8	0x0	Provides an override for STRAP_SKIP_INTERVAL
STRAP_BYPASS_RCVR_DET	11	0x0	Provides an override for STRAP_BYPASS_RCVR_DET
STRAP_COMPLIANCE_DIS	12	0x0	Provides an override for STRAP_COMPLIANCE_DIS
STRAP_FORCE_COMPLIANCE	13	0x0	Provides an override for STRAP_FORCE_COMPLIANCE
STRAP_REVERSE_LC_LANES	14	0x0	Provides an override for STRAP_REVERSE_LC_LANES

STRAP_AUTO_RC_SPEED_NEGOTIATION_DIS	15	0x0	Provides an override for STRAP_AUTO_RC_SPEED_NEGOTIATION_DIS
STRAP_LANE_NEGOTIATION	18:16	0x0	Provides an override for STRAP_LANE_NEGOTIATION 0=Compliant mode, widest possible link 1=Compliant mode, fix missing lane 0 2=Compliant mode, reverse only 3=Compliant mode, reverse only, don't require the sets to be contiguous 4=Old mode, revrese only 5=Easy training mode, reverse only 6=Reliable mode, reverse only - means to reliably train, in a reliable system 7=Reserved
Misc LC strap loadable register value			

PCIEP_STRAP_MISC - RW - 32 bits - PCIEIND_P:0xC1			
Field Name	**Bits**	**Default**	**Description**
STRAP_EXIT_LATENCY	3:0	0x0	Provides an override for STRAP_EXIT_LATENCY
STRAP_REVERSE_LANES	4	0x0	Provides an override for STRAP_REVERSE_LANES
Misc port strap loadable register values			

2.5.5 NBMISCIND Registers

NB_CNTL - RW - 32 bits - NBMISCIND:0x0			
Field Name	**Bits**	**Default**	**Description**
HIDE_NB_MSI_CAP	0	0x0	Hides the MSI capabilities in Host Bridge (NBCFG) 0=Visible (Enable) 1=Hide (Disable)
HIDE_P2P_AGP_CAP	1	0x1	Hides AGP Capabilities in the legacy AGP bridge (device 1) 0=Visible (Enable) 1=Hide (Disable)
HIDE_NB_GART_BAR	2	0x0	Hides BAR1, the legacy AGP GART BAR register 0=Visible (Enable) 1=Hide (Disable)
HIDE_MMCFG_BAR	3	0x0	Hides BAR3, the PCI Express MMCFG BAR register 0=Visible (Enable) 1=Hide (Disable)
AGPMODE30	4	0x0	Reserved for future use. This register controls no hardware 0=Disable 1=Enable AGP3.0 REGISTER MODE
AGP30ENHANCED	5	0x0	Reserved for future use. This register controls no hardware 0=Disable 1=Enable ENHANCED AGP3.0 MODE
NB_SB_CFG_EN	6	0x0	Enables configuration space access to Device 8 which is the A-Link bridge to the southbridge 0=Disable 1=Enable
HWINIT_WR_LOCK	7	0x0	Locks HWINIT register values 0=Disable 1=Enable
HIDE_CLKCFG_HEADER	8	0x0	Hides the PCI configuration space header (registers 0x0-> 0x3F) in Device 0 Function 1
STRAP_MSI_ENABLE	10	0x1	Reserved for future use. This register controls no hardware 0=Disable 1=Enable
TESTMODE_ENABLE (R)	13	0x0	From Test Controller
COM_PORT_MODE (R)	14	0x0	From Test Controller
ROM_CTRL_POST	31:16	0x0	Reserved for future use. This register controls no hardware
North Bridge Control			

NB_IOC_DEBUG - RW - 32 bits - NBMISCIND:0x1			
Field Name	**Bits**	**Default**	**Description**
SLI_OVERWRITE_EN	0	0x0	1=Overwrite SLI strap inputs (enables dev3 p2p bridge access). 0=Takes SLI inputs to control dev3 bridge access. Note: dev3 access is also controlled by IOC_P2P_CNTL:Dev3BridgeDis(nbmiscind0x0C). If only IOC_P2P_CNTL:Dev3BridgeDis is 0, access to dev3 bridge is possilbe.
NB_IOC_DEBUG_RW	15:1	0x0	Spare Read/Write Control Bits
IOC_MultiReqVldErr (R)	16	0x0	Detects Multiple CPU Downstream Request Valid Error
IOC_MemMapCfgErr (R)	17	0x0	Detects Memory Map Cfg Access Format Error
NB_IOC_DEBUG_RO (R)	31:18	0x0	Spare Read Only Status Bits
IOC Debugging purpose registers			

NB_SPARE1 - RW - 32 bits - NBMISCIND:0x2			
Field Name	**Bits**	**Default**	**Description**
NB_SPARE1_RW	15:0	0x0	Spare Read/Write Control Bits
NB_SPARE1_RO (R)	31:16	0x0	Spare Read Only Status Bits
Spare Register			

NB_STRAPS_READBACK_MUX - RW - 32 bits - NBMISCIND:0x3			
Field Name	**Bits**	**Default**	**Description**
SELECT	7:0	0x0	This register selects which 32 bits of Power-on STRAPS are read via NB_STRAPS_READBACK_DATA.
Strap Readback Mux Select Register			

NB_STRAPS_READBACK_DATA - R - 32 bits - NBMISCIND:0x4			
Field Name	**Bits**	**Default**	**Description**
READ	31:0	0x0	Values of STRAPS as selected by the mux selector, NB_STRAPS_READBACK_MUX.
Strap Readback Register			

DFT_CNTL0 - RW - 32 bits - NBMISCIND:0x5			
Field Name	**Bits**	**Default**	**Description**
TEST_DEBUG_EN	0	0x0	Enables debug bus
TEST_DEBUG_OUT_EN	6:1	0x0	Debug bus output mode select
Reserved	9:7	0x0	Reserved for future use. This register controls no hardware
TEST_DEBUG_MUX	15:10	0x0	Debug bus mux select for blk 1
GPIO_DEBUG_BUS_MUX_SEL0	19:16	0x0	Selects which bit of the internal 16-bit debug bus to route to DFT_GPIO1
GPIO_DEBUG_BUS_MUX_SEL1	23:20	0x1	Selects which bit of the internal 16-bit debug bus to route to DFT_GPIO2
GPIO_DEBUG_BUS_MUX_SEL2	27:24	0x2	Selects which bit of the internal 16-bit debug bus to route to DFT_GPIO3
GPIO_DEBUG_BUS_MUX_SEL3	31:28	0x3	Selects which bit of the internal 16-bit debug bus to route to DFT_GPIO4
DFT control 0 register			

DFT_CNTL1 - RW - 32 bits - NBMISCIND:0x6			
Field Name	**Bits**	**Default**	**Description**
TEST_DEBUG_COUNTER_EN	0	0x0	Enables debug bus counter mode
TEST_DEBUG_IN_EN	1	0x0	Reserved for future use. This register controls no hardware
DEBUG_TESTCLKIN	2	0x0	Selects the test clock output
TEST_CLK0_INV	3	0x0	Invert test output clock
DFT_MISC	15:4	0x0	Reserved
COM_PORT_OE	17:16	0x0	Reserved
COM_PORT_OUT	19:18	0x0	Reserved
COM_PORT_IN (R)	20	0x0	Reserved
DFT control 1 register			

PCIE_PDNB_CNTL - RW - 32 bits - NBMISCIND:0x7			
Field Name	**Bits**	**Default**	**Description**
TXCLK_OFF_GPP1	0	0x0	Turns off TXCLK completely for GPP1
TXCLK_OFF_GPP2	1	0x0	Turns off TXCLK completely for GPP2
TXCLK_OFF_GPP3a	2	0x0	Turns off TXCLK completely for GPP3a
TXCLK_OFF_GPP3b	3	0x0	Turns off TXCLK completely for GPP3b
TXCLK_DYN_CLKGATE_EN_GPP1	4	0x0	Enables TXCLK Dynamic clock gating for GPP1
TXCLK_DYN_CLKGATE_EN_GPP2	5	0x0	Enables TXCLK Dynamic clock gating for GPP2
TXCLK_DYN_CLKGATE_EN_GPP3a	6	0x0	Enables TXCLK Dynamic clock gating for GPP3a
TXCLK_DYN_CLKGATE_EN_SB	7	0x0	Enables TXCLK Dynamic clock gating for SB
TXCLK_SNDRCV_CLKGATE_EN_GPP1	8	0x0	Enables TXCLK SND and RCV clock gating for GPP1
TXCLK_SNDRCV_CLKGATE_EN_GPP2	9	0x0	Enables TXCLK SND and RCV clock gating for GPP2
TXCLK_SNDRCV_CLKGATE_EN_GPP3a	10	0x0	Enables TXCLK SND and RCV clock gating for GPP3a
TXCLK_SNDRCV_CLKGATE_EN_SB	11	0x0	Enables TXCLK SND and RCV clock gating for SB
TXCLK_SND_SEL_GPP1	13:12	0x0	Mux control for TXCLK SND for upper or lower PLL for GPP1
TXCLK_IO_SEL_GPP1	15:14	0x0	Mux control for TXCLK IO for upper or lower PLL for GPP1
TXCLK_SEL_GPP1	16	0x0	Mux control for TXCLK PERM, DYN, RCV for upper or lower PLL for GPP1
TXCLK_SEL_GPP2	17	0x0	Mux control for TXCLK PERM, DYN, RCV for upper or lower PLL for GPP2
BIT18	18	0x0	Reserved
BIT19	19	0x0	Reserved
TXCLK_SND_SEL_GPP2	21:20	0x0	Mux control for TXCLK SND for upper or lower PLL for GPP2
TXCLK_IO_SEL_GPP2	23:22	0x0	Mux control for TXCLK IO for upper or lower PLL for GPP2
TXCLK_DYN_CLKGATE_EN_GPP3b	24	0x0	Enables TXCLK Dynamic clock gating for GPP3b
TXCLK_SNDRCV_CLKGATE_EN_GPP3b	25	0x0	Enables TXCLK SND and RCV clock gating for GPP3b
BIT26	26	0x0	Reserved
BIT27	27	0x0	Reserved
BIT28	28	0x0	Reserved
BIT29	29	0x0	Reserved
BIT30	30	0x0	Reserved
BIT31	31	0x0	Reserved
PCIe control register			

PCIE_LINK_CFG - RW - 32 bits - NBMISCIND:0x8			
Field Name	**Bits**	**Default**	**Description**
SW_RESET_DURATION_GPP1	1:0	0x0	Sets the duration of PCIE GPP1 atomic reset 0=16 CCLK's 1=370 CCLK's 2=37000 CCLK's 3=370000 CCLK's
ATOMIC_SW_RESET_GPP1	2	0x0	Triggers Atomic Reset for PCIE GPP1 Core
ATOMIC_SW_RESET_GPP2	3	0x0	Triggers Atomic Reset for PCIE GPP2 Core
HOLD_TRAIN0_GPP1	4	0x1	Holds PCIE GPP1 Port 0 from Link Training 0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN1_GPP1	5	0x1	Holds PCIE GPP1 Port 1 from Link Training 0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN0_GPP2	6	0x1	Holds PCIE GPP2 Port 0 from Link Training 0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN1_GPP2	7	0x1	Holds PCIE GPP2 Port 1 from Link Training 0=Allow Link Training 1=Hold (Prevent) Link Training
MULTIPORT_CONFIG_GPP1	8	0x0	Multiport Configuration for PCIE GPP1 Core 0=Port 0 only 1=Port 0 and Port 1

MULTIPORT_CONFIG_GPP2	9	0x0	Multiport Configuration for PCIE GPP2 Core 0=Port 0 only 1=Port 0 and Port 1
SW_RESET_DURATION_GPP2	11:10	0x0	Duration of PCIE GPP2 atomic reset 0=16 CCLK's 1=370 CCLK's 2=37000 CCLK's 3=370000 CCLK's
CALIB_RESET_GPP2	12	0x0	Software Reset of PCIE GPP2 calibration logic 0=Disable 1=Enable
GLOBAL_RESET_GPP2	13	0x1	Software Reset of PCIE GPP2 core logic 0=Disable 1=Enable
CALIB_RESET_GPP1	14	0x0	Software Reset of PCIE GPP1 calibration logic 0=Disable 1=Enable
GLOBAL_RESET_GPP1	15	0x1	Software Reset of PCIE GPP1 core logic 0=Disable 1=Enable
SW_RESET_DURATION_GPP3a_SB	17:16	0x0	Duration of PCIE GPP3a and SB atomic reset 0=16 CCLK's 1=370 CCLK's 2=37000 CCLK's 3=370000 CCLK's
ATOMIC_SW_RESET_GPP3a	18	0x0	Atomic Reset for PCIE GPP3a Core
ATOMIC_SW_RESET_SB	19	0x0	Atomic Reset for PCIE SB Core
HOLD_TRAIN0_SB	20	0x0	Holds PCIE SB Port 0 from Link Training 0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN1_GPP3a	21	0x1	Holds PCIE GPP3a Port 0 from Link Training 0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN2_GPP3a	22	0x1	Holds PCIE GPP3a Port 1 from Link Training 0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN3_GPP3a	23	0x1	Holds PCIE GPP3a Port 2 from Link Training 0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN4_GPP3a	24	0x1	Holds PCIE GPP3a Port 3 from Link Training 0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN5_GPP3a	25	0x1	Holds PCIE GPP3a Port 4 from Link Training 0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN6_GPP3a	26	0x1	Holds PCIE GPP3a Port 5 from Link Training 0=Allow Link Training 1=Hold (Prevent) Link Training
CALIB_RESET_SB	28	0x0	Software Reset of PCIe SB calibration logic 0=Disable 1=Enable
GLOBAL_RESET_SB	29	0x0	Software Reset of PCIe SB core logic 0=Disable 1=Enable
CALIB_RESET_GPP3a	30	0x0	Software Reset of PCIE GPP3a calibration logic 0=Disable 1=Enable
GLOBAL_RESET_GPP3a	31	0x1	Software Reset of PCIE GPP3a core logic 0=Disable 1=Enable
PCIe Link Configuration Register			

IOC_DMA_ARBITER - RW - 32 bits - NBMISCIND:0x9			
Field Name	**Bits**	**Default**	**Description**
DMA_ARBITER	31:0	0x0	Arbitration algorithm implementation
IOC dma arbiter			

IOC_PCIE_CSR_Count - RW - 32 bits - NBMISCIND:0xA			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	Sets the delay in core clocks between re-issuing configuration space requests through the SB port that previously returned CRS completion status when IOC_PCIE_CNTL[CsrEnable] is set
CsrLimitCount	31:24	0x0	Sets the number of times configuration space requests through the SB port are retried when IOC_PCIE_CNTL[CsrEnable] is set before returning CRS back to the HTIU. HTIU converts CRS status to Master Abort when returning the response to the processor
IOC CSR counter			

IOC_PCIE_CNTL - RW - 32 bits - NBMISCIND:0xB			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	Forces DMA requests coming through the SB port to have the relaxed ordering attribute set when IOC_PCIE_CNTL[DmaFixAttrEn] is set
DmaForceSnoop	1	0x0	Forces DMA requests coming through the SB port to have the snoop attribute set when IOC_PCIE_CNTL[DmaFixAttrEn] is set
DmaFixAttrEn	2	0x0	Fix dma request snoop attribute
P2pDis	3	0x0	Reserved for future use. This register controls no hardware
BMSetDis	7	0x0	Disables BMSTS from being set by DMA requests coming from the SB
XactOrder	8	0x1	Enables mst read order rule
BlockNonSp	9	0x0	Blocks non-snoop dma request if PMArbDis is set
BlockSnoop	10	0x0	Blocks snoop dma request if PMArbDis is set
MstRelaxOrder	11	0x0	Master Relaxed Ordering override value. If MstRelaxOrderEn is set, the value in this register is used to override the relaxed ordering attribute for host requests targetting the southbridge
MstRelaxOrderEn	12	0x0	Enables the override for the relaxed ordering attribute for downstream host requests targetting the southbridge
MstNSoopEn	13	0x0	0=Host requests targetting the southbridge are issued with the no-snoop attribute 1=Host requests targetting the southbridge are issued with the snoop attribute
ExtDevPlug	16	0x0	Forces logical detection of an external device on the southbridge port
ExtDevCsrEn	17	0x0	When set, the CSR retry limit is ignored for the SB port when a device is detected on the far side of the PCI Express link and the link is up
CsrEnable	18	0x0	When set, configuration requests to the SB port that return CRS completion status are retried automatically
IntSelMod	19	0x0	Interrupt ABCD(0) or EFGH(1) mode
SetPowEn	20	0x0	Enables set_slot_power message to SB
IOC_SB_SetPowEn	21	0x0	Enables Set_Slot_Power_limit/Scale message to SB
IOC_SetDMAInValidEn	22	0x1	Enables DMA InValid Request handling

IOC_SB_SetPMETurnOffEn	23	0x0	Enables PME_Turn_Off/PME_To_Ack protocol between NB and SB
LockOrderingByPassDisable	24	0x0	Reserved for future use. This register controls no hardware
DMAInvalidMode	26	0x0	Control DMA InValid request handling mode: mode0=Return UR for non_posted request mode1=Drop all requests
CfgDat_Enable_NS_Ordering	27	0x0	Reserved for future use. This register controls no hardware
CrsIDRdEn	28	0x0	Enables CRS software visibility for configuration requests to the SB port. Response data equal to 0x0001 is returned for DeviceID and VendorID if CRS is returned as the completion status 0=Enable 1=Disable
IOC PCIE control counter			

IOC_P2P_CNTL - RW - 32 bits - NBMISCIND:0xC			
Field Name	**Bits**	**Default**	**Description**
Dev2BridgeDis	2	0x0	When set to 1, hides the device 2 function 0 PCIe bridge
Dev3BridgeDis	3	0x0	When set to 1, hides the device 3 function 0 PCIe bridge
Dev4BridgeDis	4	0x0	When set to 1, hides the device 4 function 0 PCIe bridge
Dev5BridgeDis	5	0x0	When set to 1, hides the device 5 function 0 PCIe bridge
Dev6BridgeDis	6	0x0	When set to 1, hides the device 6 function 0 PCIe bridge
Dev7BridgeDis	7	0x0	When set to 1, hides the device 7 function 0 PCIe bridge
GfxMetaCtl	8	0x1	When set to 1, enables multi-flopping to counteract metastability
SBMetaCtl	9	0x1	When set to 1, enables multi-flopping to counteract metastability
MsgMetaCtl	10	0x1	When set to 1, enables multi-flopping to counteract metastability
DLDownResetEn	11	0x0	When set to 1, enables DLDown to reset all ioc shadowed PCI Express registers
NonDev0ToSBEn	12	0x1	Enabling this bit will put All Type0NonDev0 external cfg request to SB
GSMEnable	13	0x0	When set to 1, enables AMD generalized stutter mode support during C1e state
BMREQPinEnable	14	0x0	Reserved for future use. This register controls no hardware
Dev9BridgeDis	16	0x0	When set to 1, hides the device 9 function 0 PCIe bridge
Dev10BridgeDis	17	0x0	When set to 1, hides the device 10 function 0 PCIe bridge
Dev11BridgeDis	18	0x0	When set to 1, hides the device 11 function 0 PCIe bridge
Dev12BridgeDis	19	0x0	When set to 1, hides the device 12 function 0 PCIe bridge
Dev13BridgeDis	20	0x0	
IOC p2p bridge control			

PCIE_LINK_DISABLE_CONTROL1 - RW - 32 bits - NBMISCIND:0xD			
Field Name	**Bits**	**Default**	**Description**
FATAL_SB_A_mask	0	0x0	When set to 1, fatal errors detected by the SB link result in the SB link being disabled
NON_FATAL_SB_A_mask	1	0x0	When set to 1, non-fatal errors detected by the SB link result in the SB link being disabled
CORR_SB_A_mask	2	0x0	When set to 1, correctable errors detected by the SB link result in the SB link being disabled
SYNCFLD_SB_A_mask	3	0x0	When set to 1, HyperTransport™ syncfloods result in the SB link being disabled

FATAL_GPP3b_A_mask	4	0x0	When set to 1, fatal errors detected by the bridge 13 link result in the bridge 13 link being disabled
NON_FATAL_GPP3bmask	5	0x0	When set to 1, non-fatal errors detected by the bridge 13 link result in the bridge 13 link being disabled
CORR_GPP3b_A_mask	6	0x0	When set to 1, correctable errors detected by the bridge 13 link result in the bridge 13 link being disabled
SYNCFLD_GPP3b_A_mask	7	0x0	When set to 1, HyperTransport syncfloods result in the bridge 13 link being disabled
FATAL_GPP1_A_mask	8	0x0	When set to 1, fatal errors detected by the bridge 2 link result in the bridge 2 link being disabled
NON_FATAL_GPP1_A_mask	9	0x0	When set to 1, non-fatal errors detected by the bridge 2 link result in the bridge 2 link being disabled
CORR_GPP1_A_mask	10	0x0	When set to 1, correctable errors detected by the bridge 2 link result in the bridge 2 link being disabled
SYNCFLD_GPP1_A_mask	11	0x0	When set to 1, HyperTransport syncfloods result in the bridge 2 link being disabled
FATAL_GPP1_B_mask	12	0x0	When set to 1, fatal errors detected by the bridge 3 link result in the bridge 3 link being disabled
NON_FATAL_GPP1_B_mask	13	0x0	When set to 1, non-fatal errors detected by the bridge 3 link result in the bridge 3 link being disabled
CORR_GPP1_B_mask	14	0x0	When set to 1, correctable errors detected by the bridge 3 link result in the bridge 3 link being disabled
SYNCFLD_GPP1_B_mask	15	0x0	When set to 1, HyperTransport syncfloods result in the bridge 3 link being disabled
FATAL_GPP2_A_mask	16	0x0	When set to 1, fatal errors detected by the bridge 11 link result in the bridge 11 link being disabled
NON_FATAL_GPP2_A_mask	17	0x0	When set to 1, non-fatal errors detected by the bridge 11 link result in the bridge 11 link being disabled
CORR_GPP2_A_mask	18	0x0	When set to 1, correctable errors detected by the bridge 11 link result in the bridge 11 link being disabled
SYNCFLD_GPP2_A_mask	19	0x0	When set to 1, HyperTransport syncfloods result in the bridge 11 link being disabled
FATAL_GPP2_B_mask	20	0x0	When set to 1, fatal errors detected by the bridge 12 link result in the bridge 12 link being disabled
NON_FATAL_GPP2_B_mask	21	0x0	When set to 1, non-fatal errors detected by the bridge 12 link result in the bridge 12 link being disabled
CORR_GPP2_B_mask	22	0x0	When set to 1, correctable errors detected by the bridge 12 link result in the bridge 12 link being disabled
SYNCFLD_GPP2_B_mask	23	0x0	When set to 1, HyperTransport syncfloods result in the bridge 12 link being disabled
FATAL_GPP3a_A_mask	24	0x0	When set to 1, fatal errors detected by the bridge 4 link result in the bridge 4 link being disabled
NON_FATAL_GPP3a_A_mask	25	0x0	When set to 1, non-fatal errors detected by the bridge 4 link result in the bridge 4 link being disabled
CORR_GPP3a_A_mask	26	0x0	When set to 1, correctable errors detected by the bridge 4 link result in the bridge 4 link being disabled
SYNCFLD_GPP3a_A_mask	27	0x0	When set to 1, HyperTransport syncfloods result in the bridge 4 link being disabled
FATAL_GPP3a_B_mask	28	0x0	When set to 1, fatal errors detected by the bridge 5 link result in the bridge 5 link being disabled
NON_FATAL_GPP3a_B_mask	29	0x0	When set to 1, non-fatal errors detected by the bridge 5 link result in the bridge 5 link being disabled
CORR_GPP3a_B_mask	30	0x0	When set to 1, correctable errors detected by the bridge 5 link result in the bridge 5 link being disabled
SYNCFLD_GPP3a_B_mask	31	0x0	When set to 1, HyperTransport syncfloods result in the bridge 5 link being disabled

IOCIsocMapAddr_LO - RW - 32 bits - NBMISCIND:0xE			
Field Name	**Bits**	**Default**	**Description**
IsocMapAdd_LO	31:6	0x0	Reserved for future use. This register controls no hardware
N/A			

IOCIsocMapAddr_HI - RW - 32 bits - NBMISCIND:0xF			
Field Name	**Bits**	**Default**	**Description**
IsocMapAdd_HI	7:0	0x0	Reserved for future use. This register controls no hardware
N/A			

DFT_CNTL2 - RW - 32 bits - NBMISCIND:0x10			
Field Name	**Bits**	**Default**	**Description**
TEST_DEBUG_READBACK (R)	15:0	0x0	Register readback port for debug bus
TEST_DEBUG_IDSEL	22:16	0x0	Debug bus block ID select
TEST_DEBUG_IDSEL_BLK2	29:23	0x0	Debug bus block 2 ID select for dual-debug bus
DFT control 2 register			

NB_BUS_NUM_CNTL - RW - 32 bits - NBMISCIND:0x11			
Field Name	**Bits**	**Default**	**Description**
NB_BUS_NUM	7:0	0x0	Sets the bus number of the northbridge when NB_BUS_LAT_Mode is 1
NB_BUS_LAT_Mode	8	0x0	Sets the mode for setting the NB bus number, if 1 the NB bus number is set by NB_BUS_NUM
CURRENT_NB_BUS_NUM	16:9	0x0	

PCIE_CORE_ARB - RW - 32 bits - NBMISCIND:0x12			
Field Name	**Bits**	**Default**	**Description**
PCIE_GPP_ARB	15:0	0x5555	Sets the arbitration priority between GPP1 and GPP2
IOC_CONTROL_2	31:16	0x0	[16] - 1: Enable forwarding of RequesterID for P2P cycles to GPP1 and GPP2 PCIE cores. [17] - 1: Enable forwarding of RequesterID for P2P cycles to SB, GPP1GPP3a, and GPP2GPP3b PCIe® cores. [18] - 1: Always use the legacy ReqID intended for messages to SB, 16`b0 for non-msg, to drive the Requester ID field. [19] - 1: Enable Interrupt Accumulator in IOC for INTx msg going to SB. [20] - 1: Enable the forwarding of the completion status for non-posted host writes; 0: Disable. [21] - 1: Enable downstream PCIe messages to pass downstream traffic; 0: Disable. [22] - 1: Enable the AER interface to UR unsupported message codes; 0: Disable. [23] - 1: Enable NMI upstream interrupt to use bits [31:24] as part of the address 0: Use hardcoded 0xFF. [31:24] - Sets bits [15:8] of the NMI interrupt address when bit 23 is set to 1

NB_TOM_PCI - RW - 32 bits - NBMISCIND:0x16			
Field Name	**Bits**	**Default**	**Description**
SAME_AS_TOM_BIU	0	0x1	When set, makes TOM_FOR_PCI the same as TOP_OF_DRAM. This is a legacy register that should always be set to 1.
TOM_FOR_PCI	31:16	0x0	Reserved
TOM for PCI			

NB_MMIOBASE - RW - 32 bits - NBMISCIND:0x17			
Field Name	**Bits**	**Default**	**Description**
MMIOBASE	31:8	0x0	Register bits [31:8] define MMIOBASE [39:16], which is the lower part of the MMIO base address
Lower MMIO base			

NB_MMIOLIMIT - RW - 32 bits - NBMISCIND:0x18			
Field Name	**Bits**	**Default**	**Description**
MMIOLIMIT	31:8	0x0	Register bits [31:8] define MMIOLIMIT [39:16], which is the lower part of the MMIO LIMIT address
High MMIO base			

PCIE_NBCFG_REG17 - RW - 32 bits - NBMISCIND:0x19			
Field Name	**Bits**	**Default**	**Description**
STRAP_BIF_CPL_ABORT_ERR_EN_GPP1	0	0x0	Enable the CPL_ABORT_ERR_STATUS, CPL_ABORT_ERR_MASK, CPL_ABORT_ERR_SEVERITY
STRAP_BIF_CPL_ABORT_ERR_EN_GPP2	1	0x0	Enable the CPL_ABORT_ERR_STATUS, CPL_ABORT_ERR_MASK, CPL_ABORT_ERR_SEVERITY
STRAP_BIF_CPL_ABORT_ERR_EN_GPP3a	2	0x0	Enable the CPL_ABORT_ERR_STATUS, CPL_ABORT_ERR_MASK, CPL_ABORT_ERR_SEVERITY
STRAP_BIF_CPL_ABORT_ERR_EN_sb	3	0x0	Enable the CPL_ABORT_ERR_STATUS, CPL_ABORT_ERR_MASK, CPL_ABORT_ERR_SEVERITY
STRAP_BIF_CPL_ABORT_ERR_EN_GPP3b	4	0x0	Enable the CPL_ABORT_ERR_STATUS, CPL_ABORT_ERR_MASK, CPL_ABORT_ERR_SEVERITY
non_fat_err_mask_A_sb	5	0x0	Non-fatal error mask
non_fat_err_rcvd_mask_A_sb	6	0x0	Mask of receiving non-fatal error message
corr_err_mask_A_sb	7	0x0	Correctable error mask
corr_err_rcvd_mask_A_sb	8	0x0	Mask of receiving correctable error message
fat_err_mask_A_sb	9	0x0	Fatal error mask
fat_err_rcvd_mask_A_sb	10	0x0	Mask of receiving fatal error message
non_fat_err_mask_A_GPP3b	11	0x0	Non-fatal error mask
non_fat_err_rcvd_mask_A_GPP3b	12	0x0	Mask of receiving non-fatal error message
corr_err_mask_A_GPP3b	13	0x0	Correctable error mask
corr_err_rcvd_mask_A_GPP3b	14	0x0	Mask of receiving correctable error message
fat_err_mask_A_GPP3b	15	0x0	Fatal error mask
fat_err_rcvd_mask_A_GPP3b	16	0x0	Mask of receiving fatal error message
non_fat_err_mask_A_GPP2	17	0x0	Non-fatal error mask
non_fat_err_rcvd_mask_A_GPP2	18	0x0	Mask of receiving non-fatal error message
corr_err_mask_A_GPP2	19	0x0	Correctable error mask
corr_err_rcvd_mask_A_GPP2	20	0x0	Mask of receiving correctable error message
fat_err_mask_A_GPP2	21	0x0	Fatal error mask

fat_err_rcvd_mask_A_GPP2	22	0x0	Mask of receiving fatal error message
non_fat_err_mask_B_GPP2	23	0x0	Non-fatal error mask
non_fat_err_rcvd_mask_B_GPP2	24	0x0	Mask of receiving non-fatal error message
corr_err_mask_B_GPP2	25	0x0	Correctable error mask
corr_err_rcvd_mask_B_GPP2	26	0x0	Mask of receiving correctable error message
fat_err_mask_B_GPP2	27	0x0	Fatal error mask
fat_err_rcvd_mask_B_GPP2	28	0x0	Mask of receiving fatal error message
non_fat_err_mask_A_GPP3a	29	0x0	Non-fatal error mask
non_fat_err_rcvd_mask_A_GPP3a	30	0x0	Mask of receiving non-fatal error message
corr_err_mask_A_GPP3a	31	0x0	Correctable error mask

PCIE_NBCFG register 17, bits 703 to 672

PCIE_NBCFG_REG18 - RW - 32 bits - NBMISCIND:0x1A			
Field Name	**Bits**	**Default**	**Description**
corr_err_rcvd_mask_A_GPP3a	0	0x0	Correctable error mask
fat_err_mask_A_GPP3a	1	0x0	Fatal error mask
fat_err_rcvd_mask_A_GPP3a	2	0x0	Mask of receiving fatal error message
non_fat_err_mask_B_GPP3a	3	0x0	Non-fatal error mask
non_fat_err_rcvd_mask_B_GPP3a	4	0x0	Mask of receiving non-fatal error message
corr_err_mask_B_GPP3a	5	0x0	Correctable error mask
corr_err_rcvd_mask_B_GPP3a	6	0x0	Mask of receiving correctable error message
fat_err_mask_B_GPP3a	7	0x0	Fatal error mask
fat_err_rcvd_mask_B_GPP3a	8	0x0	Mask of receiving fatal error message
non_fat_err_mask_C_GPP3a	9	0x0	Non-fatal error mask
non_fat_err_rcvd_mask_C_GPP3a	10	0x0	Mask of receiving non-fatal error message
corr_err_mask_C_GPP3a	11	0x0	Correctable error mask
corr_err_rcvd_mask_C_GPP3a	12	0x0	Mask of receiving correctable error message
fat_err_mask_C_GPP3a	13	0x0	Fatal error mask
fat_err_rcvd_mask_C_GPP3a	14	0x0	Mask of receiving fatal error message
non_fat_err_mask_D_GPP3a	15	0x0	Non-fatal error mask
non_fat_err_rcvd_mask_D_GPP3a	16	0x0	Mask of receiving non-fatal error message
corr_err_mask_D_GPP3a	17	0x0	Correctable error mask
corr_err_rcvd_mask_D_GPP3a	18	0x0	Mask of receiving correctable error message
fat_err_mask_D_GPP3a	19	0x0	Fatal error mask
fat_err_rcvd_mask_D_GPP3a	20	0x0	Mask of receiving fatal error message
non_fat_err_mask_E_GPP3a	21	0x0	Non-fatal error mask
non_fat_err_rcvd_mask_E_GPP3a	22	0x0	Mask of receiving non-fatal error message
corr_err_mask_E_GPP3a	23	0x0	Correctable error mask
corr_err_rcvd_mask_E_GPP3a	24	0x0	Mask of receiving correctable error message
fat_err_mask_E_GPP3a	25	0x0	Fatal error mask
fat_err_rcvd_mask_E_GPP3a	26	0x0	Mask of receiving fatal error message
non_fat_err_mask_F_GPP3a	27	0x0	Non-fatal error mask
non_fat_err_rcvd_mask_F_GPP3a	28	0x0	Mask of receiving non-fatal error message
corr_err_mask_F_GPP3a	29	0x0	Correctable error mask
corr_err_rcvd_mask_F_GPP3a	30	0x0	Mask of receiving correctable error message
fat_err_mask_F_GPP3a	31	0x0	Fatal error mask

PCIE_NBCFG register 18, bits 735 to 704

PCIE_NBCFG_REG19 - RW - 32 bits - NBMISCIND:0x1B			
Field Name	**Bits**	**Default**	**Description**
fat_err_rcvd_mask_F_GPP3a	0	0x0	Mask of receiving fatal error message
non_fat_err_mask_A_GPP1	1	0x0	Non-fatal error mask
non_fat_err_rcvd_mask_A_GPP1	2	0x0	Mask of receiving non-fatal error message
corr_err_mask_A_GPP1	3	0x0	Correctable error mask
corr_err_rcvd_mask_A_GPP1	4	0x0	Mask of receiving correctable error message
fat_err_mask_A_GPP1	5	0x0	Fatal error mask
fat_err_rcvd_mask_A_GPP1	6	0x0	Mask of receiving fatal error message
non_fat_err_mask_B_GPP1	7	0x0	Non-fatal error mask
non_fat_err_rcvd_mask_B_GPP1	8	0x0	Mask of receiving non-fatal error message
corr_err_mask_B_GPP1	9	0x0	Correctable error mask

corr_err_rcvd_mask_B_GPP1	10	0x0	Mask of receiving correctable error message
fat_err_mask_B_GPP1	11	0x0	Fatal error mask
fat_err_rcvd_mask_B_GPP1	12	0x0	Mask of receiving fatal error message
spare_14_13	14:13	0x0	
run_parity_eco	15		
enable_RAS_Parity_link_down_for_GPP1	16	0x0	Enable PCIe link down for PCIe memory parity error
enable_RAS_Parity_link_down_for_GPP2	17	0x0	Enable PCIe link down for PCIe memory parity error
enable_RAS_Parity_link_down_for_GPP3a	18	0x0	Enable PCIe link down for PCIe memory parity error
enable_RAS_Parity_link_down_for_SB	19	0x0	Enable PCIe link down for PCIe memory parity error
enable_RAS_Parity_link_down_for_GPP3b	20	0x0	Enable PCIe link down for PCIe memory parity error
external_write_enable	21		
external_address	29:22		
IOAPIC_polarity_eco_disable	30		
spare_31	31	0x0	

PCIE_NBCFG register 19, bits 767 to 736

DFT_CNTL4 - RW - 32 bits - NBMISCIND:0x1C			
Field Name	**Bits**	**Default**	**Description**
GPP3a_DEBUG_BUS_MUX_SEL0	3:0	0x0	Selects which bit of the internal 16-bit debug bus to route to GPP3a bit [0]
GPP3a_DEBUG_BUS_MUX_SEL1	7:4	0x0	Selects which bit of the internal 16-bit debug bus to route to GPP3a bit [1]
GPP3a_DEBUG_BUS_MUX_SEL2	11:8	0x0	Selects which bit of the internal 16-bit debug bus to route to GPP3a bit [2]
GPP3a_DEBUG_BUS_MUX_SEL3	15:12	0x0	Selects which bit of the internal 16-bit debug bus to route to GPP3a bit [3]
GPP3a_DEBUG_BUS_MUX_SEL4	19:16	0x0	Selects which bit of the internal 16-bit debug bus to route to GPP3a bit [4]
GPP3a_DEBUG_BUS_MUX_SEL5	23:20	0x0	Selects which bit of the internal 16-bit debug bus to route to GPP3a bit [5]

DFT_CNTL5 - RW - 32 bits - NBMISCIND:0x1D			
Field Name	**Bits**	**Default**	**Description**
GPP3b_DEBUG_BUS_MUX_SEL0	3:0	0x0	Selects which bit of the internal 16-bit debug bus to route to GPP3b bit [0]
GPP3b_DEBUG_BUS_MUX_SEL1	7:4	0x0	Selects which bit of the internal 16-bit debug bus to route to GPP3b bit [1]
GPP3b_DEBUG_BUS_MUX_SEL2	11:8	0x0	Selects which bit of the internal 16-bit debug bus to route to GPP3b bit [2]
GPP3b2_DEBUG_BUS_MUX_SEL3	15:12	0x0	Selects which bit of the internal 16-bit debug bus to route to GPP3b bit [3]
Reserved	31:16	0x0	

IOC_PCIE_D13_CSR_Count - RW - 32 bits - NBMISCIND:0x1E			
Field Name	**Bits**	**Default**	**Description**

CsrDelayCount	23:0	0x0	Sets the delay in core clocks between re-issuing configuration space requests through PCI Express bridge 13 that previously returned CRS completion status when IOC_PCIE_D13_CNTL[CsrEnable] is set
CsrLimitCount	31:24	0x0	Sets the number of times configuration space requests through PCI Express bridge 13 are retried when IOC_PCIE_D13_CNTL[CsrEnable] is set before returning CRS back to the HTIU. HTIU converts CRS status to Master Abort when returning the response to the processor
CSR Register			

IOC_PCIE_D13_CNTL - RW - 32 bits - NBMISCIND:0x1F			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	Forces DMA requests coming through PCI Express bridge 13 to have the relaxed ordering attribute set when IOC_PCIE_D13_CNTL[DmaFixAttrEn] is set
DmaForceSnoop	1	0x0	Forces DMA requests coming through PCI Express bridge 13 to have the snoop attribute set when IOC_PCIE_D13_CNTL[DmaFixAttrEn] is set
DmaFixAttrEn	2	0x0	Allows forcing of DMA attributes
P2pDis	3	0x0	Prevents peer to peer transactions from targetting devices behind this bridge
BMSetDis	7	0x0	Disables BMSTS from being set by DMA requests coming through this bridge
XactOrder	8	0x1	Forces ordering between DMA writes and cpu completions
BlockNonSp	9	0x0	Blocks Nonsnoop DMA
BlockSnoop	10	0x0	Blocks Snoop DMA
MstRelaxOrder	11	0x0	Forces relax ordering on cpu requests to this deivce
MstRelaxOrderEn	12	0x0	Allows forcing of relax ordering on cpu requests to this device
MstNSoopEn	13	0x0	0=Host requests routed through PCI Express bridge 13 are issued with the no-snoop attribute 1=Host requests routed through PCI Express bridge 13 are issued with the snoop attribute
ExtDevPlug	16	0x0	Forces logical detection of an external device on the PCI Express bridge 13 port
ExtDevCsrEn	17	0x0	When set, the CSR retry limit is ignored for PCI Express bridge 13 when a device is detected on the far side of the PCI Express link and the link is up
CsrEnable	18	0x0	When set, configuration requests through PCI Express bridge 13 that return CRS completion status are retried automatically
IntSelMod	19	0x0	Interrupt select between ABCD or EFGH
SetPowEn	20	0x0	Allows set slot power messages to this device
Device Specific controls			

NB_PROG_DEVICE_REMAP_0 - RW - 32 bits - NBMISCIND:0x20			
Field Name	**Bits**	**Default**	**Description**
NB_PROG_DEVMAP_EN	0	0x0	Enables mode to allow allocation of device numbers through registers
IOC_PCIE_Dev_Remap_Dis	1	0x1	Disables automatic remapping according to GPP PCIe configuration
GPP_PORT2_DEVMAP	7:4	0x0	Device number of GPP1 port 0
GPP_PORT3_DEVMAP	11:8	0x0	Device number of GPP1 port 1
GPP_PORT4_DEVMAP	15:12	0x0	Device number of GPP3a port 0
GPP_PORT5_DEVMAP	19:16	0x0	Device number of GPP3a port 1
GPP_PORT6_DEVMAP	23:20	0x0	Device number of GPP3a port 2
GPP_PORT7_DEVMAP	27:24	0x0	Device number of GPP3a port 3
GPP_PORT9_DEVMAP	31:28	0x0	Device number of GPP3a port 4

Register for controlling the device mapping

NB_PROG_DEVICE_REMAP_1 - RW - 32 bits - NBMISCIND:0x21			
Field Name	**Bits**	**Default**	**Description**
GPP_PORT10_DEVMAP	3:0	0x0	Device number of GPP3a port 5
GPP_PORT11_DEVMAP	7:4	0x0	Device number of GPP2 port 0
GPP_PORT12_DEVMAP	11:8	0x0	Device number of GPP2 port 1
GPP_PORT13_DEVMAP	15:12	0x0	

PCIE_NBCFG_REGA - RW - 32 bits - NBMISCIND:0x22			
Field Name	**Bits**	**Default**	**Description**
B_P90PLL_IBIAS_GPP2	9:0	0xC6	Bankwdith control of PLL
spare_11_10	11:10	0x0	
B_PG2RX_EQ_GPP1	15:12	0x0	Higher two bits for GEN2, lower two bits for GEN1, Rx Equalization setting, 00 is minimum equalization; 11 is maximum equalization
B_PG2RX_EQ_GPP2	19:16	0x0	Higher two bits for GEN2, lower two bits for GEN1, Rx Equalization setting, 00 is minimum equalization; 11 is maximum equalization
B_PG2RX_EQ_GPP3a	23:20	0x0	Higher two bits for GEN2, lower two bits for GEN1, Rx Equalization setting, 00 is minimum equalization; 11 is maximum equalization
prbs23_en_GPP1	24	0x0	PRBS23 mode enable
prbs23_en_GPP2	25	0x0	PRBS23 mode enable
prbs23_en_GPP3a	26	0x0	PRBS23 mode enable
CMGOOD_OVERRIDE_all_valid	27	0x0	Force CMGOOD high for lanes that are powered off by PCIE_P_PAD_FORCE_DIS:B_PTX_PDNB_FDIS
B_PRX_EN_FEN_sb	28	0x0	Force B_PRX_EN to enable PHY RX
B_PRX_EN_FEN_GPP1	29	0x0	Force B_PRX_EN to enable PHY RX
B_PRX_EN_FEN_GPP2	30	0x0	Force B_PRX_EN to enable PHY RX
B_PRX_EN_FEN_GPP3a	31	0x0	Force B_PRX_EN to enable PHY RX

PCIE_NBCFG register A, bits 287 to 256

PCIE_NBCFG_REGB - RW - 32 bits - NBMISCIND:0x23			
Field Name	**Bits**	**Default**	**Description**
B_PPLL_PDNB_FDIS_GPP1	1:0	0x0	Force B_PPLL_PDNB to disable PLL, the same register in PCIE_INDEX is useless
B_PPLL_BUF_PDNB_FDIS_GPP1	3:2	0x0	Force B_PPLL_BUF_PDNB to disable 10x driver in PLL, the same register in PCIE_INDEX is useless
B_PPLL_PDNB_FEN_GPP1	5:4	0x0	Force B_PPLL_PDNB to enable PLL, the same register in PCIE_INDEX is useless
B_PPLL_BUF_PDNB_FEN_GPP1	7:6	0x0	Force B_PPLL_BUF_PDNB to enable 10x driver in PLL, the same register in PCIE_INDEX is useless
B_PPLL_PDNB_FDIS_GPP2	9:8	0x0	Force B_PPLL_PDNB to disable PLL, the same register in PCIE_INDEX is useless
B_PPLL_BUF_PDNB_FDIS_GPP2	11:10	0x0	Force B_PPLL_BUF_PDNB to disable 10x driver in PLL, the same register in PCIE_INDEX is useless
B_PPLL_PDNB_FEN_GPP2	13:12	0x0	Force B_PPLL_PDNB to enable PLL, the same register in PCIE_INDEX is useless
B_PPLL_BUF_PDNB_FEN_GPP2	15:14	0x0	Force B_PPLL_BUF_PDNB to enable 10x driver in PLL, the same register in PCIE_INDEX is useless
B_PPLL_BUF_PDNB_FDIS_GPP3a	16	0x0	Force B_PPLL_BUF_PDNB to disable 10x driver in PLL, the same register in PCIE_INDEX is useless
B_PPLL_BUF_PDNB_FEN_GPP3a	17	0x0	Force B_PPLL_BUF_PDNB to enable 10x driver in PLL, the same register in PCIE_INDEX is useless
B_PPLL_PDNB_FDIS_GPP3a	18	0x0	Force B_PPLL_PDNB to disable PLL, the same register in PCIE_INDEX is useless

B_PPLL_PDNB_FEN_GPP3a	19	0x0	Force B_PPLL_PDNB to enable PLL, the same register in PCIE_INDEX is useless
prbs32_en_sb	20	0x0	PRBS32 mode enable
PHY_DEBUG_EN_GPP1	21	0x0	PHY debug mode enable
PHY_DEBUG_EN_GPP2	22	0x0	PHY debug mode enable
PHY_DEBUG_EN_GPP3a	23	0x0	PHY debug mode enable
PHY_DEBUG_MODE_all_valid	25:24	0x0	PHY debug model select 00 16 lane; 01 1 lane; 10 8 lane; output P_BRX_DATA_CLK 11 8 lane; output P90_BRX_ELEC_IDLE_ASYNC
prbs23_clr_all_valid	26	0x0	PRBS23 mode reset: clear all count, status ..
spare_31_27	31:27	0x14	

PCIE_NBCFG register B, bits 319 to 288

PCIE_NBCFG_REGC - RW - 32 bits - NBMISCIND:0x24			
Field Name	**Bits**	**Default**	**Description**
spare_9_0	9:0	0x0	
reconfig_gppsb_en_sb	10	0x0	PCIE_SB SW reset module: trigger PCIE_sb core reconfig
reconfig_gppsb_reg_idle_force_en_sb	11	0x0	PCIE_SB SW reset module: force the reg_req_idle and reg_cpl_idle to 1
reconfig_gppsb_sb	12	0x0	PCIE_SB SW reset module: reconfig_gppsb_en is low then this feature is not enabled
reconfig_gppsb_link_config_xfer_mode_sb	13	0x0	PCIE_SB SW reset module: if mode is 1, then give bif_core the value of LINK_CONFIG directly (existing implementation) if mode is 0, then only give bif_core the value after reset has been asserted
reconfig_gppsb_use_link_up_en_sb	14	0x0	PCIE_SB SW reset module: reconfig is finished when 1: reset is done and link is up 0: reset is done
reconfig_gppsb_atomic_reset_dis_sb	15	0x0	PCIE_SB SW reset module: if atomic reset is disabled, then use the rising edge of reconfig_gppsb_in_progress to trigger the reset to trigger atomic_sw_reset, the bios should read this register bit, then write the inverted value to it note that internal_reset_trigger is asserted for only 1 clock in both cases
STRAP_BIF_2VC_EN_sb	16	0x0	Enable 2nd VC functionality
ENABLE_NonD0MA_sb	17	0x0	For IOC to know when we are not in D0 state, so IOC will forward all transactions (except config cycles) to SouthBrid 1: IOC check device state and decide if forward to SB 0: IOC always forward cycle to PCIe
ENABLE_NonD0MA_GPP1	18	0x0	For IOC to know when we are not in D0 state, so IOC will forward all transactions (except config cycles) to SouthBrid 1: IOC check device state and decide if forward to SB 0: IOC always forward cycle to PCIe
ENABLE_NonD0MA_GPP2	19	0x0	For IOC to know when we are not in D0 state, so IOC will forward all transactions (except config cycles) to SouthBrid 1: IOC check device state and decide if forward to SB 0: IOC always forward cycle to PCIe
ENABLE_NonD0MA_GPP3a_GPP3b	20	0x0	For IOC to know when we are not in D0 state, so IOC will forward all transactions (except config cycles) to SouthBrid 1: IOC check device state and decide if forward to SB 0: IOC always forward cycle to PCIe
STRAP_BIF_GEN2_COMPLIANCE_GPP1_GPP2	21	0x1	Enable PCIe GEN 2 config features
STRAP_BIF_GEN2_COMPLIANCE_GPP3a	22	0x1	Enable PCIe GEN 2 config features
STRAP_BIF_ECN1P1_EN_GPP1_GPP2	23	0x1	Enable PCIe Spec1.1 ECN support
STRAP_BIF_ECN1P1_EN_GPP3a	24	0x1	Enable PCIe Spec1.1 ECN support
STRAP_BIF_ERR_REPORTING_DIS_GPP3a	25	0x1	Disable error reporting.

STRAP_BIF_ERR_REPORTING_DIS_GPP2	26	0x1	Disable error reporting.
STRAP_BIF_ERR_REPORTING_DIS_GPP1	27	0x1	Disable error reporting.
STRAP_BIF_AER_EN_sb	28	0x0	Advanced Error Reporting Enable
STRAP_BIF_AER_EN_GPP1	29	0x0	Advanced Error Reporting Enable
STRAP_BIF_AER_EN_GPP2	30	0x0	Advanced Error Reporting Enable
STRAP_BIF_AER_EN_GPP3a	31	0x0	Advanced Error Reporting Enable

PCIE_NBCFG register C, bits 351 to 320

PCIE_NBCFG_REGD - RW - 32 bits - NBMISCIND:0x25			
Field Name	**Bits**	**Default**	**Description**
STRAP_BIF_FORCE_GEN2_MODE_GPP1	0	0x0	To force PHY to operate at GEN2 speed without LC to go through GEN2 speed negotiation. This mode is intended to be used in ATE only.
STRAP_BIF_FORCE_GEN2_MODE_GPP2	1	0x0	To force PHY to operate at GEN2 speed without LC to go through GEN2 speed negotiation. This mode is intended to be used in ATE only.
STRAP_BIF_FORCE_GEN2_MODE_GPP3a	2	0x0	To force PHY to operate at GEN2 speed without LC to go through GEN2 speed negotiation. This mode is intended to be used in ATE only.
STRAP_BIF_FORCE_CDR_MODE_GPP1	3	0x0	Enable CDR test mode.
STRAP_BIF_FORCE_CDR_MODE_GPP2	4	0x0	Enable CDR test mode.
STRAP_BIF_FORCE_CDR_MODE_GPP3a	5	0x0	Enable CDR test mode.
iDbgCntrMode_all_valid	6	0x0	PCIE_PHY debug module rotation mode enable
DEBUG_BUS_CLK_EN_all_valid	7	0x0	Output enable of all debug clocks
STRAP_BIF_TEST_TOGGLE_MODE_GPP1	8	0x0	Debug mode to send 1010 pattern through the transmitter. On the receive side, the pattern is checked to make sure that the 1010 pattern is received correctly.
STRAP_BIF_TEST_TOGGLE_MODE_GPP2	9	0x0	Debug mode to send 1010 pattern through the transmitter. On the receive side, the pattern is checked to make sure that the 1010 pattern is received correctly.
STRAP_BIF_TEST_TOGGLE_MODE_GPP3a	10	0x0	Debug mode to send 1010 pattern through the transmitter. On the receive side, the pattern is checked to make sure that the 1010 pattern is received correctly.
spare_11	11	0x0	
STRAP_BIF_ALWAYS_USE_FAST_TXCLK_GPP2	12	0x0	To bypass the txclk_switch and use the 500MHz PLL clk directly for TXCLK for the bif_core, regardless of the port speed
STRAP_BIF_ALWAYS_USE_FAST_TXCLK_GPP3a	13	0x0	To bypass the txclk_switch and use the 500MHz PLL clk directly for TXCLK for the bif_core, regardless of the port speed
STRAP_BIF_ALWAYS_USE_FAST_TXCLK_GPP1	14	0x0	To bypass the txclk_switch and use the 500MHz PLL clk directly for TXCLK for the bif_core, regardless of the port speed
spare_15	15	0x0	
MarginEnable_d_GPP1	16	0x0	RX Margin Adjustment Enable
MarginEnable_d_GPP2	17	0x0	RX Margin Adjustment Enable
MarginEnable_d_GPP3a	18	0x0	RX Margin Adjustment Enable
MarginEnable_d_sb	19	0x0	RX Margin Adjustment Enable
margin_index_all_valid	23:20	0x0	RX Margin Index
STRAP_BIF_LINK_BW_NOTIFICATION_CAP_EN_GPP1	24	0x0	Selects the default value of the Link Bandwidth Notification Capability feature.
STRAP_BIF_LINK_BW_NOTIFICATION_CAP_EN_GPP2	25	0x0	Selects the default value of the Link Bandwidth Notification Capability feature.
STRAP_BIF_LINK_BW_NOTIFICATION_CAP_EN_GPP3a	26	0x0	Selects the default value of the Link Bandwidth Notification Capability feature.

CHIP_BIF_mode_GPP1	27	0x0	Identifies to the hardware whether it is the upstream or downstream component. 0: BIF is the downstream component 1: BIF is the updstream component
CHIP_BIF_mode_GPP2	28	0x0	Identifies to the hardware whether it is the upstream or downstream component. 0: BIF is the downstream component 1: BIF is the updstream component
CHIP_BIF_mode_GPP3a	29	0x0	Identifies to the hardware whether it is the upstream or downstream component. 0: BIF is the downstream component 1: BIF is the updstream component
spare_31_30	31:30	0x0	

PCIE_NBCFG register D, bits 383 to 352

PCIE_NBCFG_REGE - RW - 32 bits - NBMISCIND:0x26			
Field Name	**Bits**	**Default**	**Description**
MUX_SEL0_DownShift1_GPP3a	0	0x0	For GPP3a, TX, 6 lanes' PHY map to 8 lanes' logic design shift value, shift 1
MUX_SEL0_DownShift2_GPP3a	1	0x0	For GPP3a, TX, 6 lanes' PHY map to 8 lanes' logic design shift value, shift 2
MUX_SEL1_DownShift1_GPP3a	2	0x1	For GPP3a, TX, 6 lanes' PHY map to 8 lanes' logic design shift value, shift 1
MUX_SEL1_DownShift2_GPP3a	3	0x0	For GPP3a, TX, 6 lanes' PHY map to 8 lanes' logic design shift value, shift 2
MUX_SEL2_DownShift1_GPP3a	4	0x1	For GPP3a, TX, 6 lanes' PHY map to 8 lanes' logic design shift value, shift 1
MUX_SEL2_DownShift2_GPP3a	5	0x0	For GPP3a, TX, 6 lanes' PHY map to 8 lanes' logic design shift value, shift 2
MUX_SEL3_DownShift1_GPP3a	6	0x1	For GPP3a, TX, 6 lanes' PHY map to 8 lanes' logic design shift value, shift 1
MUX_SEL3_DownShift2_GPP3a	7	0x0	For GPP3a, TX, 6 lanes' PHY map to 8 lanes' logic design shift value, shift 2
MUX_SEL4_DownShift1_GPP3a	8	0x1	For GPP3a, TX, 6 lanes' PHY map to 8 lanes' logic design shift value, shift 1
MUX_SEL4_DownShift2_GPP3a	9	0x0	For GPP3a, TX, 6 lanes' PHY map to 8 lanes' logic design shift value, shift 2
MUX_SEL5_DownShift1_GPP3a	10	0x1	For GPP3a, TX, 6 lanes' PHY map to 8 lanes' logic design shift value, shift 1
MUX_SEL5_DownShift2_GPP3a	11	0x0	For GPP3a, TX, 6 lanes' PHY map to 8 lanes' logic design shift value, shift 2
MUX_SEL0_GPP3a	13:12	0x3	For GPP3a, RX, 8 lanes' logic design map to 6 lanes' PHY, select register
MUX_SEL1_GPP3a	15:14	0x0	For GPP3a, RX, 8 lanes' logic design map to 6 lanes' PHY, select register
MUX_SEL2_GPP3a	17:16	0x2	For GPP3a, RX, 8 lanes' logic design map to 6 lanes' PHY, select register
MUX_SEL3_GPP3a	19:18	0x2	For GPP3a, RX, 8 lanes' logic design map to 6 lanes' PHY, select register
MUX_SEL4_GPP3a	21:20	0x2	For GPP3a, RX, 8 lanes' logic design map to 6 lanes' PHY, select register
MUX_SEL5_GPP3a	23:22	0x2	For GPP3a, RX, 8 lanes' logic design map to 6 lanes' PHY, select register
MUX_SEL6_GPP3a	25:24	0x2	For GPP3a, RX, 8 lanes' logic design map to 6 lanes' PHY, select register
MUX_SEL7_GPP3a	27:26	0x0	For GPP3a, RX, 8 lanes' logic design map to 6 lanes' PHY, select register
STRAP_BIF_all_valid_GPP1	28	0x0	When asserted (low), allows strap values to be loaded into the PCIe core.
STRAP_BIF_all_valid_GPP2	29	0x0	When asserted (low), allows strap values to be loaded into the PCIe core.
STRAP_BIF_all_valid_GPP3a	30	0x0	When asserted (low), allows strap values to be loaded into the PCIe core.

STRAP_BIF_all_valid_sb	31	0x0	When asserted (low), allows strap values to be loaded into the PCIe core.

PCIE_NBCFG register E, bits 415 to 384

PCIE_NBCFG_REGF - RW - 32 bits - NBMISCIND:0x27			
Field Name	**Bits**	**Default**	**Description**
STRAP_BIF_REVERSE_ALL_GPP1	0	0x0	Reverse all lanes (lane 0->15, lane 15->0). This is independent of port reversal
STRAP_BIF_REVERSE_ALL_GPP2	1	0x0	Reverse all lanes (lane 0->15, lane 15->0). This is independent of port reversal
STRAP_BIF_REVERSE_ALL_GPP3a	2	0x0	Reverse all lanes (lane 0->5, lane 5->0). This is independent of port reversal
STRAP_BIF_REVERSE_LANES_A_GPP 1	3	0x0	Reverse lanes per port in the PHY (1 bit per port)
STRAP_BIF_REVERSE_LANES_B_GPP 1	4	0x0	Reverse lanes per port in the PHY (1 bit per port)
STRAP_BIF_REVERSE_LANES_A_GPP 2	5	0x0	Reverse lanes per port in the PHY (1 bit per port)
STRAP_BIF_REVERSE_LANES_B_GPP 2	6	0x0	Reverse lanes per port in the PHY (1 bit per port)
STRAP_BIF_REVERSE_LANES_A_GPP 3a	7	0x0	Reverse lanes per port in the PHY (1 bit per port)
STRAP_BIF_REVERSE_LANES_B_GPP 3a	8	0x0	Reverse lanes per port in the PHY (1 bit per port)
STRAP_BIF_REVERSE_LANES_C_GPP 3a	9	0x0	Reverse lanes per port in the PHY (1 bit per port)
STRAP_BIF_REVERSE_LANES_D_GPP 3a	10	0x0	Reverse lanes per port in the PHY (1 bit per port)
STRAP_BIF_REVERSE_LANES_E_GPP 3a	11	0x0	Reverse lanes per port in the PHY (1 bit per port)
STRAP_BIF_REVERSE_LANES_F_GPP 3a	12	0x0	Reverse lanes per port in the PHY (1 bit per port)
STRAP_BIF_REVERSE_LC_LANES_A_ GPP1	13	0x0	Reverse lanes per port in the LC (1 bit per port), this is for EP
STRAP_BIF_REVERSE_LC_LANES_B_ GPP1	14	0x0	Reverse lanes per port in the LC (1 bit per port), this is for EP
STRAP_BIF_REVERSE_LC_LANES_A_ GPP2	15	0x0	Reverse lanes per port in the LC (1 bit per port), this is for EP
STRAP_BIF_REVERSE_LC_LANES_B_ GPP2	16	0x0	Reverse lanes per port in the LC (1 bit per port), this is for EP
STRAP_BIF_REVERSE_LC_LANES_A_ GPP3a	17	0x0	Reverse lanes per port in the LC (1 bit per port), this is for EP
STRAP_BIF_REVERSE_LC_LANES_B_ GPP3a	18	0x0	Reverse lanes per port in the LC (1 bit per port), this is for EP
STRAP_BIF_REVERSE_LC_LANES_C_ GPP3a	19	0x0	Reverse lanes per port in the LC (1 bit per port), this is for EP
STRAP_BIF_REVERSE_LC_LANES_D_ GPP3a	20	0x0	Reverse lanes per port in the LC (1 bit per port), this is for EP
STRAP_BIF_REVERSE_LC_LANES_E_ GPP3a	21	0x0	Reverse lanes per port in the LC (1 bit per port), this is for EP
STRAP_BIF_REVERSE_LC_LANES_F_ GPP3a	22	0x0	Reverse lanes per port in the LC (1 bit per port), this is for EP
Force_off_LCLK_PCIE_GPP1	23	0x0	Set to 1 to turn off LCLK for one core
Force_off_LCLK_PCIE_GPP2	24	0x0	Set to 1 to turn off LCLK for one core
Force_off_LCLK_PCIE_GPP3a	25	0x0	Set to 1 to turn off LCLK for one core
Force_off_LCLK_PCIE_GPP3b	26	0x0	Set to 1 to turn off LCLK for one core
STRAP_DEEMPH_STR_SEL_gpp_GPP1 _GPP2	29:27	0x0	Using B_P90TX_DEEMPH_STR to control De-emphasis settings for the PHY, this function has a higher priority than STRAP_BIF_TX_DEEMPH_STR

STRAP_BIF_DE_EMPHASIS_SEL_A_GPP2	30	0x1	This controls the default value of the Selectable De-emphasis field (bit 6) of the Link Control 2 configuration register. 1 = RC advertises -3.5dB de-emphasis 0 = the RC advertises -6dB de-emphasis.
STRAP_BIF_DE_EMPHASIS_SEL_B_GPP2	31	0x1	This controls the default value of the Selectable De-emphasis field (bit 6) of the Link Control 2 configuration register. 1 = RC advertises -3.5dB de-emphasis 0 = the RC advertises -6dB de-emphasis.

PCIE_NBCFG register F, bits 447 to 416

PCIE_NBCFG_REG10 - RW - 32 bits - NBMISCIND:0x28			
Field Name	**Bits**	**Default**	**Description**
STRAP_BIF_DE_EMPHASIS_SEL_A_GPP1	0	0x1	This controls the default value of the Selectable De-emphasis field (bit 6) of the Link Control 2 configuration register. 1 = RC advertises -3.5dB de-emphasis 0 = the RC advertises -6dB de-emphasis.
STRAP_BIF_DE_EMPHASIS_SEL_B_GPP1	1	0x1	This controls the default value of the Selectable De-emphasis field (bit 6) of the Link Control 2 configuration register. 1 = RC advertises -3.5dB de-emphasis 0 = the RC advertises -6dB de-emphasis.
STRAP_BIF_DE_EMPHASIS_SEL_A_GPP3a	2	0x1	This controls the default value of the Selectable De-emphasis field (bit 6) of the Link Control 2 configuration register. 1 = RC advertises -3.5dB de-emphasis 0 = the RC advertises -6dB de-emphasis.
STRAP_BIF_DE_EMPHASIS_SEL_B_GPP3a	3	0x1	This controls the default value of the Selectable De-emphasis field (bit 6) of the Link Control 2 configuration register. 1 = RC advertises -3.5dB de-emphasis 0 = the RC advertises -6dB de-emphasis.
STRAP_BIF_DE_EMPHASIS_SEL_C_GPP3a	4	0x1	This controls the default value of the Selectable De-emphasis field (bit 6) of the Link Control 2 configuration register. 1 = RC advertises -3.5dB de-emphasis 0 = the RC advertises -6dB de-emphasis.
STRAP_BIF_DE_EMPHASIS_SEL_D_GPP3a	5	0x1	This controls the default value of the Selectable De-emphasis field (bit 6) of the Link Control 2 configuration register. 1 = RC advertises -3.5dB de-emphasis 0 = the RC advertises -6dB de-emphasis.
STRAP_BIF_DE_EMPHASIS_SEL_E_GPP3a	6	0x1	This controls the default value of the Selectable De-emphasis field (bit 6) of the Link Control 2 configuration register. 1 = RC advertises -3.5dB de-emphasis 0 = the RC advertises -6dB de-emphasis.
STRAP_BIF_DE_EMPHASIS_SEL_F_GPP3a	7	0x0	This controls the default value of the Selectable De-emphasis field (bit 6) of the Link Control 2 configuration register. 1 = RC advertises -3.5dB de-emphasis 0 = the RC advertises -6dB de-emphasis.
STRAP_BIF_DEEMPH_BIF_SEL_A_GPP2	8	0x1	Allow the bif_core to select the LTSSM Deemphasis value that goes to the PHY (based on PCIe® 2.0, rev 0.9 specification). When set to '0', the value comes from the STRAP_BIF_TX_DEEMPH_STR straps.
STRAP_BIF_DEEMPH_BIF_SEL_B_GPP2	9	0x1	Allow the bif_core to select the LTSSM Deemphasis value that goes to the PHY (based on PCIe 2.0, rev 0.9 specification). When set to '0', the value comes from the STRAP_BIF_TX_DEEMPH_STR straps.

STRAP_BIF_DEEMPH_BIF_SEL_A_GPP1	10	0x1	Allow the bif_core to select the LTSSM Deemphasis value that goes to the PHY (based on PCIe 2.0, rev 0.9 specification). When set to '0', the value comes from the STRAP_BIF_TX_DEEMPH_STR straps.
STRAP_BIF_DEEMPH_BIF_SEL_B_GPP1	11	0x1	Allow the bif_core to select the LTSSM Deemphasis value that goes to the PHY (based on PCIe 2.0, rev 0.9 specification). When set to '0', the value comes from the STRAP_BIF_TX_DEEMPH_STR straps.
STRAP_BIF_DEEMPH_BIF_SEL_A_GPP3a	12	0x1	Allow the bif_core to select the LTSSM Deemphasis value that goes to the PHY (based on PCIe 2.0, rev 0.9 specification). When set to '0', the value comes from the STRAP_BIF_TX_DEEMPH_STR straps.
STRAP_BIF_DEEMPH_BIF_SEL_B_GPP3a	13	0x1	Allow the bif_core to select the LTSSM Deemphasis value that goes to the PHY (based on PCIe 2.0, rev 0.9 specification). When set to '0', the value comes from the STRAP_BIF_TX_DEEMPH_STR straps.
STRAP_BIF_DEEMPH_BIF_SEL_C_GPP3a	14	0x1	Allow the bif_core to select the LTSSM Deemphasis value that goes to the PHY (based on PCIe 2.0, rev 0.9 specification). When set to '0', the value comes from the STRAP_BIF_TX_DEEMPH_STR straps.
STRAP_BIF_DEEMPH_BIF_SEL_D_GPP3a	15	0x1	Allow the bif_core to select the LTSSM Deemphasis value that goes to the PHY (based on PCIe 2.0, rev 0.9 specification). When set to '0', the value comes from the STRAP_BIF_TX_DEEMPH_STR straps.
STRAP_BIF_DEEMPH_BIF_SEL_E_GPP3a	16	0x1	Allow the bif_core to select the LTSSM Deemphasis value that goes to the PHY (based on PCIe 2.0, rev 0.9 specification). When set to '0', the value comes from the STRAP_BIF_TX_DEEMPH_STR straps.
STRAP_BIF_DEEMPH_BIF_SEL_F_GPP3a	17	0x1	Allow the bif_core to select the LTSSM Deemphasis value that goes to the PHY (based on PCIe 2.0, rev 0.9 specification). When set to '0', the value comes from the STRAP_BIF_TX_DEEMPH_STR straps.
STRAP_BIF_EN_DEC_TO_HIDDEN_REG_GPP2	18	0x1	Hide register if the cfg cap is disabled
STRAP_BIF_EN_DEC_TO_HIDDEN_REG_GPP1	19	0x1	Hide register if the cfg cap is disabled
STRAP_BIF_EN_DEC_TO_HIDDEN_REG_GPP3a	20	0x1	Hide register if the cfg cap is disabled
STRAP_BIF_EN_DEC_TO_HIDDEN_REG_sb	21	0x1	Hide register if the cfg cap is disabled
STRAP_BIF_LC_SELECT_DEEMPHASIS_GPP2	22	0x0	Default value of the LC_SELECT_DEEMPHASIS private register.
STRAP_BIF_LC_SELECT_DEEMPHASIS_GPP1	23	0x0	Default value of the LC_SELECT_DEEMPHASIS private register.
STRAP_BIF_LC_SELECT_DEEMPHASIS_GPP3a	24	0x0	Default value of the LC_SELECT_DEEMPHASIS private register.
STRAP_BIF_SYMALIGN_HW_DEBUG_GPP2	25	0x0	This strap is for debug purpose. 0: debug off 1: debug on
STRAP_BIF_SYMALIGN_HW_DEBUG_GPP1	26	0x0	This strap is for debug purpose. 0: debug off 1: debug on
STRAP_BIF_SYMALIGN_HW_DEBUG_GPP3a	27	0x0	This strap is for debug purpose. 0: debug off 1: debug on
STRAP_BIF_SYMALIGN_HW_DEBUG_GPP3b	28	0x0	This strap is for debug purpose. 0: debug off 1: debug on
spare_30_29	30:29	0x0	
STRAP_BIF_LC_DONT_DEASSERT_RX_EN_IN_TEST_GPP2	31	0x0	Control LC_PI_RcvrEn in s_Poll_Compliance_Idle and s_Rcvd_Loopback_Speed. 0: De-assert RcvrEn in s_Poll_Compliance_Idle and s_Rcvd_Loopback_Speed after the EIOS have been transmitted. 1: Don't de-assert RcvrEn in s_Poll_Compliance_Idle or s_Rcvd_Loopback_Speed.

PCIE_NBCFG register 10, bits 479 to 448

PCIE_NBCFG_REG11 - RW - 32 bits - NBMISCIND:0x29			
Field Name	**Bits**	**Default**	**Description**
STRAP_BIF_LC_DONT_DEASSERT_RX_EN_IN_TEST_GPP1	0	0x0	Control LC_PI_RcvrEn in s_Poll_Compliance_Idle and s_Rcvd_Loopback_Speed. 0: De-assert RcvrEn in s_Poll_Compliance_Idle and s_Rcvd_Loopback_Speed after the EIOS have been transmitted. 1: Don't de-assert RcvrEn in s_Poll_Compliance_Idle or s_Rcvd_Loopback_Speed.
STRAP_BIF_LC_DONT_DEASSERT_RX_EN_IN_TEST_GPP3a	1	0x0	Control LC_PI_RcvrEn in s_Poll_Compliance_Idle and s_Rcvd_Loopback_Speed. 0: De-assert RcvrEn in s_Poll_Compliance_Idle and s_Rcvd_Loopback_Speed after the EIOS have been transmitted. 1: Don't de-assert RcvrEn in s_Poll_Compliance_Idle or s_Rcvd_Loopback_Speed.
STRAP_BIF_DSN_EN_GPP2	2	0x0	Enable device serial number cap.
STRAP_BIF_DSN_EN_GPP1	3	0x0	Enable device serial number cap.
STRAP_BIF_DSN_EN_GPP3a	4	0x0	Enable device serial number cap.
STRAP_BIF_DSN_EN_sb	5	0x0	Enable device serial number cap.
spare_7_6	7:6	0x0	
STRAP_BIF_TX_DEEMPH_STR_GPP2	15:8	0x1	De-emphasis and Transmit Margin settings for the PHY
STRAP_BIF_TX_DEEMPH_STR_GPP1	23:16	0x1	De-emphasis and Transmit Margin settings for the PHY
STRAP_BIF_TX_DEEMPH_STR_GPP3a	31:24	0x1	De-emphasis and Transmit Margin settings for the PHY

PCIE_NBCFG register 11, bits 511 to 480

PCIE_NBCFG_REG12 - RW - 32 bits - NBMISCIND:0x2A			
Field Name	**Bits**	**Default**	**Description**
sw_reset_duration_GPP3b	1:0	0x0	Sets the duration of PCIE GPP3b atomic reset POSSIBLE VALUES: 00 - 16 CCLK`s 01 - 370 CCLK`s 02 - 37000 CCLK`s 03 - 370000 CCLK`s
atomic_sw_reset_GPP3b	2	0x0	Atomic Reset for PCIE GPP3b Core
spare_3	3	0x0	
CHIP_BIF_hold_training_GPP3b	4	0x1	Hold PCIE GPP3b from Link Training POSSIBLE VALUES: 00 - Allow Link Training 01 - Hold (Prevent) Link Training
spare_13_5	13:5	0x0	
LINK_CONFIG_CALIB_RESET_GPP3b	14	0x0	Software Reset of PCIE GPP3b calibration logic POSSIBLE VALUES: 00 - Disable 01 - Enable
LINK_CONFIG_GLOBAL_RESET_GPP3b	15	0x1	Software Reset of PCIE GPP3b calibration logic POSSIBLE VALUES: 00 - Disable 01 - Enable
B_PG2PLL_IDLEDET_TH_GPP3b	17:16	0x0	Idle detector threshold control. 00: VDD/22 01: VDD/34 10: VDD/18 11: VDD/14

B_PG2PLL_CREN_MODE_GPP3b	18	0x0	Clock Recovery Enable mode. 0: Clock recovery is enabled when B_PG2RX_CR_EN=1 and disabled when B_PG2RX_CR_EN=0 when P90_BRX_ELEC_IDLE_ASYNC=1 1: Clock recovery enable is independent of B_PG2RX_CR_EN
B_P90PLL_TEST_GPP3b	19	0x0	Test mode control for the PLL counters. When asserted, the reference divider and the feedback divider are cascaded and the output is observed through P90_BPLL_TESTOUT. The REFCLK to P90_BPLL_TESTOUT divide ratio is given by NR NF. When either NR or NF is one, P90_BPLL_TESTOUT will not toggle.
B_P90PLL_IBIAS_GPP3b	29:20	0xC6	Bankwdith control of PLL
B_P90PLL_RESET_GPP3b	30	0x0	PLL reset (active high).
B_P90PLL_RESET_EN_GPP3b	31	0x0	PLL reset enable. 0: PLL reset comes from internal counter (triggered by B_PPLL_PDNB). 1: PLL reset comes from B_P90PLL_RESET

PCIE_NBCFG register 12, bits 543 to 512

PCIE_NBCFG_REG13 - RW - 32 bits - NBMISCIND:0x2B			
Field Name	**Bits**	**Default**	**Description**
B_P90PLL_CLKF_GPP3b	6:0	0x32	Feedback clock divider setting (NF). NF = B_P90PLL_CLKF[6:0] + 1 0: divide by 2 1: divide by 3 2: divide by 2 3: divide by 3 4: divide by 4
spare_7	7	0x0	
B_P90PLL_CLKR_GPP3b	9:8	0x0	Reference clock divider setting (NR). NR = B_P90PLL_CLKR[1:0] + 1 Bit 1 not used. 0: divide by 1 1: divide by 2
B_PTX_DEEMPH_EN_GPP3b	11:10	0x3	PCI Express transmitter de-emphasis enable , higher bit for GEN2, lower bit for GEN1 0: de-emphasis disabled for mobile 1: de-emphasis enabled
B_PG2RX_EQ_GPP3b	15:12	0x0	higher two bits for GEN2, lower two bits for GEN1, Rx Equalization setting, 00 is minimum equalization; 11 is maximum equalization
B_P90TX_DEEMPH_STR_GPP3b	23:16	0x1	De-emphasis settings for the PHY, this value is used when STRAP_DEEMPH_STR_SEL=1
B_P90RX_CRPHSIZE_GPP3b	27:24	0x5	Receiver Clock Recovery Phase Filter size, higher two bits for GEN2, lower two bits for GEN1 00: N=2, effective % ratio = 8 01: N=4, effective % ratio = 16 10: N=8, effective % ratio = 32 11: N=16, effective % ratio = 64
B_P90RX_CRFRSIZE_GPP3b	31:28	0x5	Clock recovery Freq Filter size, higher two bits for GEN2, lower two bits for GEN1.

PCIE_NBCFG register 13, bits 575 to 544

PCIE_NBCFG_REG14 - RW - 32 bits - NBMISCIND:0x2C			
Field Name	**Bits**	**Default**	**Description**
B_P90RX_CRFR_ON_GPP3b	1:0	0x0	Higher bit for GEN2, lower bit for GEN1. 0: Clock recovery frequency loop disabled 1: Clock recovery frequency loop enabled

B_PTX_PWRS_ENB_GPP3b	2	0x1	PCI Express transmitter power-saving enable bar 0: 50% Tx output swing for mobile applications 1: Full output swing
B_P90TX_CLKG_EN_GPP3b	3	0x1	Transmitter Clock Gating Enable 0: Disable clock gating 1: Enable clock gating for power savings
B_P90TX_DRV_STR_GPP3b	5:4	0x1	Output driver strength control. 00: 26mA nominal 01: 20mA nominal 10: 22mA nominal 11: 24mA nominal
B_PG2TX_TAPINV_GPP3b	6	0x1	When asserted, inverts the third de-emphasis filter tap
B_PG2RX_IDLEDET_EN_GPP3b	7	0x1	0: Idle detector is disabled. P90_BRX_ELEC_IDLE_ASYNC is forced low. 1: Idle detector is enabled.
B_PRX_LBACK_EN_GPP3b	8	0x0	When asserted, the Rx receives its input from txrx_lback_d_p and txrx_lback_d_n. See rxtx_lback_en in Tx.
B_PRX_DET_BLOCK_GPP3b	9	0x0	When asserted, sets P_BRX_ELEC_IDLE low.
B_P90RX_CLKG_EN_GPP3b	10	0x1	When de-asserted, disables clock gating in power saving modes.
B_P90RX_CRFR_BPASS_GPP3b	11	0x0	When asserted, bypasses the clock recovery Freq Estimator output with B_PRX_CRFR[5:0].
B_P90RX_CRFR_GPP3b	17:12	0x0	Bypass value for the clock recovery Freq Estimator output. Selected by asserting B_PRX_CRFR_BPASS.
B_P90RX_CRCTRL_BPASS_GPP3b	18	0x0	When asserted, bypasses the clock recovery Phase Counter output with B_PRX_CRCTRL[6:0].
B_P90PLL_BACKUP_2_GPP3b	19	0x0	
B_P90RX_CRCTRL_GPP3b	26:20	0x0	Bypass value for the clock recovery Phase Counter output. Selected by asserting B_PRX_CRCTRL_BPASS
B_PG2REFCLK_TERM_EN_GPP3b	27	0x0	PCIe® reference clock termination enable
B_P90PLL_BACKUP_1_0_GPP3b	29:28	0x0	B_P90PLL_BACKUP[0] (distributed to Rx as pllrxg2_bypass_sel): 0: select rxcr_data_clk for rxtxg2_bypass_data from Rx to high speed Tx bypass path 1: select rxcr90_elec_idle_async for rxtxg2_bypass_data from Rx to high speed Tx bypass path B_P90PLL_BACKUP[1] (distributed to Tx as plltxg2_bypass_sel): 0: select B_P90TX_TEST_DATA[0] for high speed Tx bypass path 1: select for rxtxg2_bypass_data for high Tx bypass path
B_PG2REFCLK_TERM_VAL_GPP3b	31:30	0x0	PCIe reference clock termination value: 00: 100 Ohms differential 01: 100 - x Ohms differential 10: 100 + x Ohms differential 11: 100 + 2x Ohms differential

PCIE_NBCFG register 14, bits 607 to 576

PCIE_NBCFG_REG15 - RW - 32 bits - NBMISCIND:0x2D			
Field Name	**Bits**	**Default**	**Description**
prbs23_en_GPP3b	0	0x0	PRBS23 mode enable
PHY_DEBUG_EN_GPP3b	1	0x0	PHY debug mode enable
MarginEnable_d_GPP3b	2	0x0	RX Margin Adjustment Enable
spare_3	3	0x0	
STRAP_DEEMPH_STR_SEL_GPP3b	4	0x0	Using B_P90TX_DEEMPH_STR to control De-emphasis settings for the PHY, this function has a higher priority than STRAP_BIF_TX_DEEMPH_STR

STRAP_BIF_DE_EMPHASIS_SEL_A_GPP3b	5	0x1	This controls the default value of the Selectable De-emphasis field (bit 6) of the Link Control 2 configuration register. 1 = RC advertises -3.5dB de-emphasis 0 = the RC advertises -6dB de-emphasis.
STRAP_BIF_DEEMPH_BIF_SEL_A_GPP3b	6	0x1	Allow the bif_core to select the LTSSM Deemphasis value that goes to the PHY (based on PCIe 2.0, rev 0.9 specification). When set to '0', the value comes from the STRAP_BIF_TX_DEEMPH_STR straps.
STRAP_BIF_EN_DEC_TO_HIDDEN_REG_GPP3b	7	0x1	Hide register if the cfg cap is disabled
STRAP_BIF_TX_DEEMPH_STR_GPP3b	15:8	0x1	De-emphasis and Transmit Margin settings for the PHY
STRAP_BIF_LC_SELECT_DEEMPHASIS_GPP3b	16	0x0	Default value of the LC_SELECT_DEEMPHASIS private register.
spare_18_17	18:17	0x0	
STRAP_BIF_DSN_EN_GPP3b	19	0x0	Enable device serial number cap.
STRAP_BIF_LC_DONT_DEASSERT_RX_EN_IN_TEST_GPP3b	20	0x0	Control LC_PI_RcvrEn in s_Poll_Compliance_Idle and s_Rcvd_Loopback_Speed. 0: De-assert RcvrEn in s_Poll_Compliance_Idle and s_Rcvd_Loopback_Speed after the EIOS have been transmitted. 1: Don't de-assert RcvrEn in s_Poll_Compliance_Idle or s_Rcvd_Loopback_Speed.
STRAP_BIF_all_valid_GPP3b	21	0x0	When asserted (low), allows strap values to be loaded into the PCIe core.
STRAP_BIF_FORCE_CDR_MODE_GPP3b	22	0x0	Enable CDR test mode.
STRAP_BIF_TEST_TOGGLE_MODE_GPP3b	23	0x0	Debug mode to send 1010 pattern through the transmitter. On the receive side, the pattern is checked to make sure that the 1010 pattern is received correctly.
STRAP_BIF_REVERSE_LC_LANES_A_GPP3b	24	0x0	Reverse lanes per port in the LC (1 bit per port), this is for EP
STRAP_BIF_REVERSE_LANES_A_GPP3b	25	0x0	Reverse lanes per port in the PHY (1 bit per port)
spare_26	26	0x1	
STRAP_BIF_REVERSE_ALL_GPP3b	27	0x0	Reverse all lanes (lane 0->3, lane 3->0). This is independent of port reversal
STRAP_BIF_AER_EN_GPP3b	28	0x0	Advanced Error Reporting Enable
STRAP_BIF_ERR_REPORTING_DIS_GPP3b	29	0x1	Disable error reporting.
STRAP_BIF_ECN1P1_EN_GPP3b	30	0x1	Enable PCIe® Spec1.1 ECN support
STRAP_BIF_GEN2_COMPLIANCE_GPP3b	31	0x1	Enable PCIe GEN 2 config features

PCIE_NBCFG register 15, bits 639 to 608

PCIE_NBCFG_REG16 - RW - 32 bits - NBMISCIND:0x2E			
Field Name	**Bits**	**Default**	**Description**
STRAP_BIF_FORCE_GEN2_MODE_GPP3b	0	0x0	To force PHY to operate at GEN2 speed without LC to go through GEN2 speed negotiation. This mode is intended to be used in ATE only.
STRAP_BIF_LINK_BW_NOTIFICATION_CAP_EN_GPP3b	1	0x0	Selects the default value of the Link Bandwidth Notification Capability feature.
STRAP_BIF_ALWAYS_USE_FAST_TXCLK_GPP3b	2	0x0	To bypass the txclk_switch and use the 500MHz PLL clk directly for TXCLK for the bif_core, regardless of the port speed
CHIP_BIF_mode_GPP3b	3	0x0	Identifies to the hardware whether it is the upstream or downstream component. 0: BIF is the downstream component 1: BIF is the updstream component
B_PRX_EN_FEN_GPP3b	4	0x0	Force B_PRX_EN to enable PHY RX, the same register in PCIE_INDEX is useless

B_PPLL_PDNB_FEN_GPP3b	5	0x0	Force B_PPLL_PDNB to enable PLL, the same register in PCIE_INDEX is useless
B_PPLL_PDNB_FDIS_GPP3b	6	0x0	Force B_PPLL_PDNB to disable PLL, the same register in PCIE_INDEX is useless
B_PPLL_BUF_PDNB_FEN_GPP3b	7	0x0	Force B_PPLL_BUF_PDNB to enable 10x driver in PLL, the same register in PCIE_INDEX is useless
B_PPLL_BUF_PDNB_FDIS_GPP3b	8	0x0	Force B_PPLL_BUF_PDNB to disable 10x driver in PLL, the same register in PCIE_INDEX is useless
B_PPLL_PDNB_FEN_PHY_GPP3b	9	0x0	Directly force to PHY PLL_PDNB to enable PLL
spare_11_10	11:10	0x0	
STRAP_BIF_VC_EN_GPP2	12	0x0	Virtual Channel CFG register Enable
STRAP_BIF_VC_EN_GPP1	13	0x0	Virtual Channel CFG register Enable
STRAP_BIF_VC_EN_gpp	14	0x0	Virtual Channel CFG register Enable
STRAP_BIF_VC_EN_GPP3b	15	0x0	Virtual Channel CFG register Enable
STRAP_BIF_LC_TARGET_LINK_SPEED_OVERRIDE_EN_GPP2	16	0x0	Default value for the LC_TARGET_LINK_SPEED_OVERRIDE_EN private register bit. Set this strap to '1' in order to force the advertised Target Link Speed to 2.5GT/s during boot up.
STRAP_BIF_LC_TARGET_LINK_SPEED_OVERRIDE_EN_GPP1	17	0x0	Default value for the LC_TARGET_LINK_SPEED_OVERRIDE_EN private register bit. Set this strap to '1' in order to force the advertised Target Link Speed to 2.5GT/s during boot up.
STRAP_BIF_LC_TARGET_LINK_SPEED_OVERRIDE_EN_GPP3a	18	0x0	Default value for the LC_TARGET_LINK_SPEED_OVERRIDE_EN private register bit. Set this strap to '1' in order to force the advertised Target Link Speed to 2.5GT/s during boot up.
STRAP_BIF_LC_TARGET_LINK_SPEED_OVERRIDE_EN_GPP3b	19	0x0	Default value for the LC_TARGET_LINK_SPEED_OVERRIDE_EN private register bit. Set this strap to '1' in order to force the advertised Target Link Speed to 2.5GT/s during boot up.
STRAP_BIF_ECRC_GEN_EN_GPP1	20	0x0	Generate ECRC in TX
STRAP_BIF_ECRC_GEN_EN_GPP2	21	0x0	Generate ECRC in TX
STRAP_BIF_ECRC_GEN_EN_GPP3a	22	0x0	Generate ECRC in TX
STRAP_BIF_ECRC_GEN_EN_sb	23	0x0	Generate ECRC in TX
STRAP_BIF_ECRC_GEN_EN_GPP3b	24	0x0	Generate ECRC in TX
STRAP_BIF_ECRC_CHECK_EN_GPP1	25	0x0	enable ECRC check in RX and ECRC error report
STRAP_BIF_ECRC_CHECK_EN_GPP2	26	0x0	enable ECRC check in RX and ECRC error report
STRAP_BIF_ECRC_CHECK_EN_GPP3a	27	0x0	enable ECRC check in RX and ECRC error report
STRAP_BIF_ECRC_CHECK_EN_sb	28	0x0	enable ECRC check in RX and ECRC error report
STRAP_BIF_ECRC_CHECK_EN_GPP3b	29	0x0	enable ECRC check in RX and ECRC error report
spare_31_30	31:30	0x0	

PCIE_NBCFG register 16, bits 671 to 640

PCIE_GPP2_P2P_ARBITRER_CONTROL - RW - 32 bits - NBMISCIND:0x2F			
Field Name	**Bits**	**Default**	**Description**
Eff_size_a_GPP2	7:0	0x4	Number of times we select a client a on GPP2 before we are forced to switch
Eff_size_b_GPP2	15:8	0x4	Number of times we select a client b on GPP2 before we are forced to switch
Eff_mask_GPP2	31:16	0xffff	Programmable address mask to determine what is a match on GPP2

PCIE_NBCFG_REG2 - RW - 32 bits - NBMISCIND:0x32			
Field Name	**Bits**	**Default**	**Description**
B_PG2REFCLK_TERM_VAL_GPP1	1:0	0x0	PCIe® reference clock termination value: 00: 100 Ohms differential 01: 100 - x Ohms differential 10: 100 + x Ohms differential 11: 100 + 2x Ohms differential

B_PG2REFCLK_TERM_VAL_GPP2	3:2	0x0	PCIe reference clock termination value: 00: 100 Ohms differential 01: 100 - x Ohms differential 10: 100 + x Ohms differential 11: 100 + 2x Ohms differential
B_PG2REFCLK_TERM_VAL_GPP3a	5:4	0x0	PCIe reference clock termination value: 00: 100 Ohms differential 01: 100 - x Ohms differential 10: 100 + x Ohms differential 11: 100 + 2x Ohms differential
B_PG2REFCLK_TERM_EN_GPP1_GPP2	6	0x0	PCIe reference clock termination enable
B_PG2REFCLK_TERM_EN_GPP3a	7	0x0	PCIe reference clock termination enable
B_P90PLL_IBIAS_GPP3a	17:8	0xC6	Bankwdith control of PLL
B_PPLL_PDNB_FEN_PHY_GPP1	19:18	0x0	Directly force to PHY PLL_PDNB to enable PLL
B_PG2PLL_IDLEDET_TH_GPP1	21:20	0x0	Idle detector threshold control. 00: VDD/22 01: VDD/34 10: VDD/18 11: VDD/14
B_PG2PLL_IDLEDET_TH_GPP2	23:22	0x0	Idle detector threshold control. 00: VDD/22 01: VDD/34 10: VDD/18 11: VDD/14
B_PG2PLL_IDLEDET_TH_GPP3a	25:24	0x0	Idle detector threshold control. 00: VDD/22 01: VDD/34 10: VDD/18 11: VDD/14
REG2_spare_28_26	28:26	0x7	
B_PG2PLL_VCTRLADC_EN_all_valid	29	0x0	PLL control voltage a2d converter enable
B_PPLL_PDNB_FEN_PHY_GPP2	31:30	0x0	Directly force to PHY PLL_PDNB to enable PLL

PCIE_NBCFG register 2, bits 31 to 0

PCIE_NBCFG_REG3 - RW - 32 bits - NBMISCIND:0x33			
Field Name	**Bits**	**Default**	**Description**
B_P90PLL_IBIAS_1_0_GPP1	9:0	0xC6	
B_P90PLL_BACKUP_1_0_GPP1	11:10	0x0	B_P90PLL_BACKUP[0] (distributed to Rx as pllrxg2_bypass_sel): 0: select rxcr_data_clk for rxtxg2_bypass_data from Rx to high speed Tx bypass path 1: select rxcr90_elec_idle_async for rxtxg2_bypass_data from Rx to high speed Tx bypass path B_P90PLL_BACKUP[1] (distributed to Tx as plltxg2_bypass_sel): 0: select B_P90TX_TEST_DATA[0] for high speed Tx bypass path 1: select for rxtxg2_bypass_data for high Tx bypass path
B_P90PLL_BACKUP_1_0_GPP2	13:12	0x0	B_P90PLL_BACKUP[0] (distributed to Rx as pllrxg2_bypass_sel): 0: select rxcr_data_clk for rxtxg2_bypass_data from Rx to high speed Tx bypass path 1: select rxcr90_elec_idle_async for rxtxg2_bypass_data from Rx to high speed Tx bypass path B_P90PLL_BACKUP[1] (distributed to Tx as plltxg2_bypass_sel): 0: select B_P90TX_TEST_DATA[0] for high speed Tx bypass path 1: select for rxtxg2_bypass_data for high Tx bypass path

B_P90PLL_BACKUP_1_0_GPP3a	15:14	0x0	B_P90PLL_BACKUP[0] (distributed to Rx as pllrxg2_bypass_sel): 0: select rxcr_data_clk for rxtxg2_bypass_data from Rx to high speed Tx bypass path 1: select rxcr90_elec_idle_async for rxtxg2_bypass_data from Rx to high speed Tx bypass path B_P90PLL_BACKUP[1] (distributed to Tx as plltxg2_bypass_sel): 0: select B_P90TX_TEST_DATA[0] for high speed Tx bypass path 1: select for rxtxg2_bypass_data for high Tx bypass path
STRAP_INC_PLLCAL_PHASE_GPP1_GPP2	16	0x0	This register will increase the upper phase (15:13) for the PLL lock time timer (16 bit timer)
ARESET_STRAP_all_valid	17	0x0	Asynchronous reset. Asserted at the beginning of slow-speed functional test to align P_BRX_DATA_OUT[9:0] and P_BRX_DATA_CLK across all lanes.
B_PG2PLL_CREN_MODE_GPP2	18	0x0	Clock Recovery Enable mode. 0: Clock recovery is enabled when B_PG2RX_CR_EN=1 and disabled when B_PG2RX_CR_EN=0 when P90_BRX_ELEC_IDLE_ASYNC=1 1: Clock recovery enable is independent of B_PG2RX_CR_EN
B_PG2PLL_CREN_MODE_GPP1	19	0x0	Clock Recovery Enable mode. 0: Clock recovery is enabled when B_PG2RX_CR_EN=1 and disabled when B_PG2RX_CR_EN=0 when P90_BRX_ELEC_IDLE_ASYNC=1 1: Clock recovery enable is independent of B_PG2RX_CR_EN
B_PG2PLL_FREQ_LOCK_EN_FC_all_valid	20	0x0	
B_PG2PLL_CREN_MODE_GPP3a	21	0x0	Clock Recovery Enable mode. 0: Clock recovery is enabled when B_PG2RX_CR_EN=1 and disabled when B_PG2RX_CR_EN=0 when P90_BRX_ELEC_IDLE_ASYNC=1 1: Clock recovery enable is independent of B_PG2RX_CR_EN
B_P90PLL_TEST_GPP1	22	0x0	Test mode control for the PLL counters. When asserted, the reference divider and the feedback divider are cascaded and the output is observed through P90_BPLL_TESTOUT. The REFCLK to P90_BPLL_TESTOUT divide ratio is given by NR NF. When either NR or NF is one, P90_BPLL_TESTOUT will not toggle.
B_P90PLL_TEST_GPP2	23	0x0	Test mode control for the PLL counters. When asserted, the reference divider and the feedback divider are cascaded and the output is observed through P90_BPLL_TESTOUT. The REFCLK to P90_BPLL_TESTOUT divide ratio is given by NR NF. When either NR or NF is one, P90_BPLL_TESTOUT will not toggle.
B_P90PLL_TEST_GPP3a	24	0x0	Test mode control for the PLL counters. When asserted, the reference divider and the feedback divider are cascaded and the output is observed through P90_BPLL_TESTOUT. The REFCLK to P90_BPLL_TESTOUT divide ratio is given by NR NF. When either NR or NF is one, P90_BPLL_TESTOUT will not toggle.
B_P90PLL_RESET_GPP1	25	0x0	PLL reset (active high).
B_P90PLL_RESET_GPP2	26	0x0	PLL reset (active high).
B_P90PLL_RESET_GPP3a	27	0x0	PLL reset (active high).
B_P90PLL_RESET_EN_GPP1	28	0x0	PLL reset enable. 0: PLL reset comes from internal counter (triggered by B_PPLL_PDNB). 1: PLL reset comes from B_P90PLL_RESET

B_P90PLL_RESET_EN_GPP2	29	0x0	PLL reset enable. 0: PLL reset comes from internal counter (triggered by B_PPLL_PDNB). 1: PLL reset comes from B_P90PLL_RESET
B_P90PLL_RESET_EN_GPP3a	30	0x0	PLL reset enable. 0: PLL reset comes from internal counter (triggered by B_PPLL_PDNB). 1: PLL reset comes from B_P90PLL_RESET
spare_31	31	0x0	

PCIE_NBCFG register 3, bits 63 to 32

PCIE_NBCFG_REG4 - RW - 32 bits - NBMISCIND:0x34			
Field Name	**Bits**	**Default**	**Description**
B_P90PLL_CLKF_GPP1	6:0	0x32	Feedback clock divider setting (NF). NF = B_P90PLL_CLKF[6:0] + 1 0: divide by 2 1: divide by 3 2: divide by 2 3: divide by 3 4: divide by 4
B_P90PLL_BACKUP_2_GPP1	7	0x0	
B_P90PLL_CLKF_GPP2	14:8	0x32	Feedback clock divider setting (NF). NF = B_P90PLL_CLKF[6:0] + 1 0: divide by 2 1: divide by 3 2: divide by 2 3: divide by 3 4: divide by 4
B_P90PLL_BACKUP_2_GPP2	15	0x0	
B_P90PLL_CLKF_GPP3a	22:16	0x32	Feedback clock divider setting (NF). NF = B_P90PLL_CLKF[6:0] + 1 0: divide by 2 1: divide by 3 2: divide by 2 3: divide by 3 4: divide by 4
B_P90PLL_BACKUP_2_GPP3a	23	0x0	
B_P90PLL_CLKR_GPP1	25:24	0x0	Reference clock divider setting (NR). NR = B_P90PLL_CLKR[1:0] + 1 Bit 1 not used. 0: divide by 1 1: divide by 2
B_P90PLL_CLKR_GPP2	27:26	0x0	Reference clock divider setting (NR). NR = B_P90PLL_CLKR[1:0] + 1 Bit 1 not used. 0: divide by 1 1: divide by 2
B_P90PLL_CLKR_GPP3a	29:28	0x0	Reference clock divider setting (NR). NR = B_P90PLL_CLKR[1:0] + 1 Bit 1 not used. 0: divide by 1 1: divide by 2
B_PPLL_PDNB_FEN_PHY_GPP3a	30	0x0	Directly force to PHY PLL_PDNB to enable PLL
B_PPLL_PDNB_FEN_PHY_sb	31	0x0	Directly force to PHY PLL_PDNB to enable PLL

PCIE_NBCFG register 4, bits 95 to 64

PCIE_NBCFG_REG5 - RW - 32 bits - NBMISCIND:0x35			
Field Name	**Bits**	**Default**	**Description**
spare_0	0	0x1	
B_P90PLL_BACKUP_3_GPP1	1	0x0	
B_P90PLL_BACKUP_3_GPP2	2	0x0	

B_P90PLL_BACKUP_3_GPP3a	3	0x0	
B_P90PLL_BACKUP_3_GPP3b	4	0x0	
B_P90PLL_BACKUP_sb	5	0x0	
Reg_Turn_Off_Both_PLLs_GPP1_GPP2	7:6	0x1	PLL_CALIB_DONE select, in X16 mode, set to 2'b11, in X8 mode, set to 2'b00
spare_9_8	9:8	0x0	
Parity_manager_clk_switch	10	0x0	
spare_12_11	12:11	0x2	
Reg_Blocking_AT_sb	13	0x0	Blocking AT field non-zero value of EP
Reg_Blocking_AT_GPP3b	14	0x0	Blocking AT field non-zero value of EP
Reg_Blocking_AT_GPP3a	15	0x0	Blocking AT field non-zero value of EP
Reg_Blocking_AT_GPP2	16	0x0	Blocking AT field non-zero value of EP
Reg_Blocking_AT_GPP1	17	0x0	Blocking AT field non-zero value of EP
B_PTX_PWRS_ENB_GPP1	18	0x1	PCI Express transmitter power-saving enable bar 0: 50% Tx output swing for mobile applications 1: Full output swing
B_PTX_PWRS_ENB_GPP2	19	0x1	PCI Express transmitter power-saving enable bar 0: 50% Tx output swing for mobile applications 1: Full output swing
B_PTX_PWRS_ENB_GPP3a	20	0x1	PCI Express transmitter power-saving enable bar 0: 50% Tx output swing for mobile applications 1: Full output swing
B_P90TX_CLKG_EN_GPP1	21	0x1	Transmitter Clock Gating Enable 0: Disable clock gating 1: Enable clock gating for power savings
B_P90TX_CLKG_EN_GPP2	22	0x1	Transmitter Clock Gating Enable 0: Disable clock gating 1: Enable clock gating for power savings
B_P90TX_CLKG_EN_GPP3a	23	0x1	Transmitter Clock Gating Enable 0: Disable clock gating 1: Enable clock gating for power savings
B_PG2TX_TAPINV_GPP1_GPP2	24	0x1	When asserted, inverts the third de-emphasis filter tap
B_PG2TX_TAPINV_GPP3a	25	0x1	When asserted, inverts the third de-emphasis filter tap
B_P90TX_DRV_STR_GPP1	27:26	0x1	Output driver strength control. 00: 26mA nominal 01: 20mA nominal 10: 22mA nominal 11: 24mA nominal
B_P90TX_DRV_STR_GPP2	29:28	0x1	Output driver strength control. 00: 26mA nominal 01: 20mA nominal 10: 22mA nominal 11: 24mA nominal
B_P90TX_DRV_STR_GPP3a	31:30	0x1	Output driver strength control. 00: 26mA nominal 01: 20mA nominal 10: 22mA nominal 11: 24mA nominal

PCIE_NBCFG register 5, bits 127 to 96

PCIE_NBCFG_REG6 - RW - 32 bits - NBMISCIND:0x36			
Field Name	**Bits**	**Default**	**Description**
B_P90TX_DEEMPH_STR_GPP1	7:0	0x1	De-emphasis settings for the PHY, this value is used when STRAP_DEEMPH_STR_SEL=1
B_P90TX_DEEMPH_STR_GPP2	15:8	0x1	De-emphasis settings for the PHY, this value is used when STRAP_DEEMPH_STR_SEL=1
B_P90TX_DEEMPH_STR_GPP3a	23:16	0x1	De-emphasis settings for the PHY, this value is used when STRAP_DEEMPH_STR_SEL=1
B_PTX_DEEMPH_EN_GPP1	25:24	0x3	PCI Express transmitter de-emphasis enable , higher bit for GEN2, lower bit for GEN1 0: de-emphasis disabled for mobile 1: de-emphasis enabled

B_PTX_DEEMPH_EN_GPP2	27:26	0x3	PCI Express transmitter de-emphasis enable , higher bit for GEN2, lower bit for GEN1 0: de-emphasis disabled for mobile 1: de-emphasis enabled
B_PTX_DEEMPH_EN_GPP3a	29:28	0x3	PCI Express transmitter de-emphasis enable , higher bit for GEN2, lower bit for GEN1 0: de-emphasis disabled for mobile 1: de-emphasis enabled
spare_31_30	31:30	0x0	

PCIE_NBCFG register 6, bits 159 to 128

PCIE_NBCFG_REG7 - RW - 32 bits - NBMISCIND:0x37			
Field Name	**Bits**	**Default**	**Description**
B_PG2RX_IDLEDET_EN_GPP1	0	0x1	0: Idle detector is disabled. P90_BRX_ELEC_IDLE_ASYNC is forced low. 1: Idle detector is enabled.
B_PG2RX_IDLEDET_EN_GPP2	1	0x1	0: Idle detector is disabled. P90_BRX_ELEC_IDLE_ASYNC is forced low. 1: Idle detector is enabled.
B_PG2RX_IDLEDET_EN_GPP3a	2	0x1	0: Idle detector is disabled. P90_BRX_ELEC_IDLE_ASYNC is forced low. 1: Idle detector is enabled.
B_PRX_LBACK_EN_GPP1	3	0x0	When asserted, the Rx receives its input from txrx_lback_d_p and txrx_lback_d_n. See rxtx_lback_en in Tx.
B_PRX_LBACK_EN_GPP2	4	0x0	When asserted, the Rx receives its input from txrx_lback_d_p and txrx_lback_d_n. See rxtx_lback_en in Tx.
B_PRX_LBACK_EN_GPP3a	5	0x0	When asserted, the Rx receives its input from txrx_lback_d_p and txrx_lback_d_n. See rxtx_lback_en in Tx.
B_PRX_DET_BLOCK_GPP1_GPP2	6	0x0	When asserted, sets P_BRX_ELEC_IDLE low.
B_PRX_DET_BLOCK_GPP3a	7	0x0	When asserted, sets P_BRX_ELEC_IDLE low.
spare_10_8	10:8	0x7	
B_P90RX_CLKG_EN_GPP1	11	0x1	When de-asserted, disables clock gating in power saving modes.
B_P90RX_CLKG_EN_GPP2	12	0x1	When de-asserted, disables clock gating in power saving modes.
B_P90RX_CLKG_EN_GPP3a	13	0x1	When de-asserted, disables clock gating in power saving modes.
spare_16_14	16:14	0x7	
B_P90RX_CRFR_BPASS_GPP1	17	0x0	When asserted, bypasses the clock recovery Freq Estimator output with B_PRX_CRFR[5:0].
B_P90RX_CRFR_BPASS_GPP2	18	0x0	When asserted, bypasses the clock recovery Freq Estimator output with B_PRX_CRFR[5:0].
B_P90RX_CRFR_BPASS_GPP3a	19	0x0	When asserted, bypasses the clock recovery Freq Estimator output with B_PRX_CRFR[5:0].
B_P90RX_CRPHSIZE_GPP1	23:20	0x5	Receiver Clock Recovery Phase Filter size, higher two bits for GEN2, lower two bits for GEN1 00: N=2, effective % ratio = 8 01: N=4, effective % ratio = 16 10: N=8, effective % ratio = 32 11: N=16, effective % ratio = 64
B_P90RX_CRPHSIZE_GPP2	27:24	0x5	Receiver Clock Recovery Phase Filter size, higher two bits for GEN2, lower two bits for GEN1 00: N=2, effective % ratio = 8 01: N=4, effective % ratio = 16 10: N=8, effective % ratio = 32 11: N=16, effective % ratio = 64
B_P90RX_CRPHSIZE_GPP3a	31:28	0x5	Receiver Clock Recovery Phase Filter size, higher two bits for GEN2, lower two bits for GEN1 00: N=2, effective % ratio = 8 01: N=4, effective % ratio = 16 10: N=8, effective % ratio = 32 11: N=16, effective % ratio = 64

PCIE_NBCFG register 7, bits 191 to 160

PCIE_NBCFG_REG8 - RW - 32 bits - NBMISCIND:0x38			
Field Name	**Bits**	**Default**	**Description**
B_P90RX_CRFR_GPP1	5:0	0x0	Bypass value for the clock recovery Freq Estimator output. Selected by asserting B_PRX_CRFR_BPASS.
B_P90RX_CRFR_ON_GPP1	7:6	0x0	higher bit for GEN2, lower bit for GEN1, 0: Clock recovery frequency loop disabled 1: Clock recovery frequency loop enabled
B_P90RX_CRFR_GPP2	13:8	0x0	Bypass value for the clock recovery Freq Estimator output. Selected by asserting B_PRX_CRFR_BPASS.
B_P90RX_CRFR_ON_GPP2	15:14	0x0	higher bit for GEN2, lower bit for GEN1, 0: Clock recovery frequency loop disabled 1: Clock recovery frequency loop enabled
B_P90RX_CRFR_GPP3a	21:16	0x0	Bypass value for the clock recovery Freq Estimator output. Selected by asserting B_PRX_CRFR_BPASS.
B_P90RX_CRFR_ON_GPP3a	23:22	0x0	higher bit for GEN2, lower bit for GEN1, 0: Clock recovery frequency loop disabled 1: Clock recovery frequency loop enabled
B_P90RX_CRCTRL_GPP1	30:24	0x0	Bypass value for the clock recovery Phase Counter output. Selected by asserting B_PRX_CRCTRL_BPASS
B_P90RX_CRCTRL_BPASS_GPP1	31	0x0	When asserted, bypasses the clock recovery Phase Counter output with B_PRX_CRCTRL[6:0].

PCIE_NBCFG register 8, bits 223 to 192

PCIE_NBCFG_REG9 - RW - 32 bits - NBMISCIND:0x39			
Field Name	**Bits**	**Default**	**Description**
B_P90RX_CRCTRL_GPP2	6:0	0x0	Bypass value for the clock recovery Phase Counter output. Selected by asserting B_PRX_CRCTRL_BPASS
B_P90RX_CRCTRL_BPASS_GPP2	7	0x0	When asserted, bypasses the clock recovery Phase Counter output with B_PRX_CRCTRL[6:0].
B_P90RX_CRCTRL_GPP3a	14:8	0x0	Bypass value for the clock recovery Phase Counter output. Selected by asserting B_PRX_CRCTRL_BPASS
B_P90RX_CRCTRL_BPASS_GPP3a	15	0x0	When asserted, bypasses the clock recovery Phase Counter output with B_PRX_CRCTRL[6:0].
B_P90RX_CRFRSIZE_GPP1	19:16	0x5	Clock recovery Freq Filter size, higher two bits for GEN2, lower two bits for GEN1.
B_P90RX_CRFRSIZE_GPP2	23:20	0x5	Clock recovery Freq Filter size, higher two bits for GEN2, lower two bits for GEN1.
B_P90RX_CRFRSIZE_GPP3a	27:24	0x5	Clock recovery Freq Filter size, higher two bits for GEN2, lower two bits for GEN1.
spare_29_28	29:28	0x0	
CHIP_BIF_VOLTAGE_LEVEL_all_valid	30	0x0	The status of current voltage level for PCIe module, GEN2 needs high voltage, 1: For Gen2; 0: For Gen1
CHIP_BIF_VOLTAGE_LOW_REQ_B_all_valid	31	0x0	For power saving, require PCIe module changing to low speed (Gen1 mode)

PCIE_NBCFG register 9, bits 255 to 224

NB_BROADCAST_BASE_LO - RW - 32 bits - NBMISCIND:0x3A			
Field Name	**Bits**	**Default**	**Description**
GPU_FB_BROADCAST_SIZE	7:0	0x0	Broadcast range size, unit is 8MB. 0x01=8MBytes 0x02=16Mbytes
GPU_FB_BROADCAST_BASE_LO	31:20	0x0	Broadcast base address[31:20]
Broadcast bass low address			

NB_BROADCAST_BASE_HI - RW - 32 bits - NBMISCIND:0x3B			
Field Name	**Bits**	**Default**	**Description**
GPU_FB_BROADCAST_BASE_HI	31:0	0x0	Broadcast base address[63:32]
Broadcast base high address			

NB_BROADCAST_CNTL - RW - 32 bits - NBMISCIND:0x3C			
Field Name	**Bits**	**Default**	**Description**
GPU_FB_BROADCAST_PRIMARY	1:0	0x0	Defines primary graphics device 0=Dev2 1=Dev3 2=Dev11 3=Dev12
GPU_FB_BROADCAST_DEV_EN	5:2	0x0	Broadcast Enable for each device individually
GPU_FB_BROADCAST_EN	6	0x0	Enables broadcast range
GPU_FB_BROADCAST_P2PSELF_EN	7	0x0	Allows gfx device to broadcast to itself
GPU_FB_BROADCAST_OFFSET	31:12	0x0	Offset between prefetachable base address and translated broadcast base
Broadcast control registers			

NB_APIC_P2P_CNTL - RW - 32 bits - NBMISCIND:0x3D			
Field Name	**Bits**	**Default**	**Description**
APIC_D2_Enable	0	0x0	Enables Dev2 pci bridge APIC range decoding. Cpu memory request with address[39:12] = 0x00_FECx_x is decoded and issued to each p2p bridge depending on each bridge's APIC range setting in APIC_D2_Range. What is left in this range(0x00_FECx_x) that is not declared by any bridge is forwarded to SB
APIC_D3_Enable	1	0x0	Enables Dev3 pci bridge APIC range decoding. Cpu memory request with address[39:12] = 0x00_FECx_x is decoded and issued to each p2p bridge depending on each bridge's APIC range setting in APIC_D3_Range. What is left in this range(0x00_FECx_x) that is not declared by any bridge is forwarded to SB
APIC_D4_Enable	2	0x0	Enables Dev4 pci bridge APIC range decoding. Cpu memory request with address[39:12] = 0x00_FECx_x is decoded and issued to each p2p bridge depending on each bridge's APIC range setting in APIC_D4_Range. What is left in this range(0x00_FECx_x) that is not declared by any bridge is forwarded to SB
APIC_D5_Enable	3	0x0	Enables Dev5 pci bridge APIC range decoding. Cpu memory request with address[39:12] = 0x00_FECx_x is decoded and issued to each p2p bridge depending on each bridge's APIC range setting in APIC_D5_Range. What is left in this range(0x00_FECx_x) that is not declared by any bridge is forwarded to SB
APIC_D6_Enable	4	0x0	Enables Dev6 pci bridge APIC range decoding. Cpu memory request with address[39:12] = 0x00_FECx_x is decoded and issued to each p2p bridge depending on each bridge's APIC range setting in APIC_D6_Range. What is left in this range(0x00_FECx_x) that is not declared by any bridge is forwarded to SB

APIC_D7_Enable	5	0x0	Enables Dev7 pci bridge APIC range decoding. Cpu memory request with address[39:12] = 0x00_FECx_x is decoded and issued to each p2p bridge depending on each bridge's APIC range setting in APIC_D7_Range. What is left in this range(0x00_FECx_x) that is not declared by any bridge is forwarded to SB
APIC_D9_Enable	6	0x0	Enables Dev9 pci bridge APIC range decoding. Cpu memory request with address[39:12] = 0x00_FECx_x is decoded and issued to each p2p bridge depending on each bridge's APIC range setting in APIC_D9_Range. What is left in this range(0x00_FECx_x) that is not declared by any bridge is forwarded to SB
APIC_D10_Enable	7	0x0	Enables Dev10 pci bridge APIC range decoding. Cpu memory request with address[39:12] = 0x00_FECx_x is decoded and issued to each p2p bridge depending on each bridge's APIC range setting in APIC_D10_Range. What is left in this range(0x00_FECx_x) that is not declared by any bridge is forwarded to SB
APIC_D11_Enable	8	0x0	Enables Dev11 pci bridge APIC range decoding. Cpu memory request with address[39:12] = 0x00_FECx_x is decoded and issued to each p2p bridge depending on each bridge's APIC range setting in APIC_D11_Range. What is left in this range(0x00_FECx_x) that is not declared by any bridge is forwarded to SB
APIC_D12_Enable	9	0x0	Enables Dev12 pci bridge APIC range decoding. Cpu memory request with address[39:12] = 0x00_FECx_x is decoded and issued to each p2p bridge depending on each bridge's APIC range setting in APIC_D12_Range. What is left in this range(0x00_FECx_x) that is not declared by any bridge is forwarded to SB
APIC_D13_Enable	10	0x0	Enables Dev13 pci bridge APIC range decoding. Cpu memory request with address[39:12] = 0x00_FECx_x is decoded and issued to each p2p bridge depending on each bridge's APIC range setting in APIC_D13_Range. What is left in this range(0x00_FECx_x) that is not declared by any bridge is forwarded to SB
PCI bridge APIC control register			

NB_APIC_P2P_RANGE_0 - RW - 32 bits - NBMISCIND:0x3E			
Field Name	**Bits**	**Default**	**Description**
APIC_D2_Range	7:0	0x0	Defines bits [19:12] for Dev2 APIC range. Dev2 APIC range is Addr[39:12] = 20'h00_FEC, APIC_D2_Range[7:0]
APIC_D3_Range	15:8	0x0	Defines bits [19:12] for Dev3 APIC range. Dev3 APIC range is Addr[39:12] = 12'h00_FEC, APIC_D3_Range[7:0]
APIC_D4_Range	23:16	0x0	Defines bits [19:12] for Dev4 APIC range. Dev4 APIC range is Addr[39:12] = 12'h00_FEC, APIC_D4_Range[7:0]
APIC_D5_Range	31:24	0x0	Defines bits [19:12] for Dev5 APIC range. Dev5 APIC range is Addr[39:12] = 12'h00_FEC, APIC_D5_Range[7:0]
PCI bridge APIC range 0			

NB_APIC_P2P_RANGE_1 - RW - 32 bits - NBMISCIND:0x3F			
Field Name	**Bits**	**Default**	**Description**
APIC_D6_Range	7:0	0x0	Defines bits [19:12] for Dev6 APIC range. Dev6 APIC range is Addr[39:12] = 20'h00_FEC, APIC_D6_Range[7:0]
APIC_D7_Range	15:8	0x0	Defines bits [19:12] for Dev7 APIC range. Dev7 APIC range is Addr[39:12] = 20'h00_FEC, APIC_D7_Range[7:0]

APIC_D9_Range	23:16	0x0	Defines bits [19:12] for Dev9 APIC range. Dev9 APIC range is Addr[39:12] = 20'h00_FEC, APIC_D9_Range[7:0]
APIC_D10_Range	31:24	0x0	Defines bits [19:12] for Dev10 APIC range. Dev10 APIC range is Addr[39:12] = 20'h00_FEC, APIC_D10_Range[7:0]
PCI bridge APIC range 1			

NB_APIC_P2P_RANGE_2 - RW - 32 bits - NBMISCIND:0x40			
Field Name	**Bits**	**Default**	**Description**
APIC_D11_Range	7:0	0x0	Defines bits [19:12] for Dev11 APIC range. Dev11 APIC range is Addr[39:12] = 20'h00_FEC, APIC_D11_Range[7:0]
APIC_D12_Range	15:8	0x0	Defines bits [19:12] for Dev12 APIC range. Dev12 APIC range is Addr[39:12] = 20'h00_FEC, APIC_D12_Range[7:0]
APIC_D13_Range	23:16	0x0	Defines bits [19:12] for Dev13 APIC range. Dev13 APIC range is Addr[39:12] = 20'h00_FEC, APIC_D13_Range[7:0]
PCI bridge APIC range 2			

GPIO_PAD_CNTL_PU_PD - RW - 32 bits - NBMISCIND:0x41			
Field Name	**Bits**	**Default**	**Description**
GPIO_TMDS_HPD_PU	0	0x1	Reserved for future use. This register controls no hardware
GPIO_DDC_DATA_PU	1	0x1	Reserved for future use. This register controls no hardware
GPIO_I2C_CLK_PU	2	0x1	Weak pull up control for the I2C_CLK pad when GPIO_I2C_CLK_OR is set 1=Weak pull up disabled 0=Weak pull up enabled
GPIO_I2C_DATA_PU	3	0x1	Weak pull up control for the I2C_DATA pad when GPIO_I2C_DATA_OR is set 1=Weak pull up disabled 0=Weak pull up enabled
GPIO_STRP_DATA_PU	4	0x1	Weak pull up control for the STRP_DATA pad when GPIO_STRP_DATA_OR is set 1=Weak pull up disabled 0=Weak pull up enabled
GPIO_DAC_SDA_PU	5	0x1	Reserved for future use. This register controls no hardware
GPIO_DAC_HSYNC_PU	6	0x1	Reserved for future use. This register controls no hardware
GPIO_DAC_VSYNC_PU	7	0x1	Reserved for future use. This register controls no hardware
GPIO_LVDS_ENA_BL_PU	8	0x1	Reserved for future use. This register controls no hardware
GPIO_LVDS_DIGON_PU	9	0x1	Reserved for future use. This register controls no hardware
GPIO_LVDS_BLON_PU	10	0x1	Reserved for future use. This register controls no hardware
GPIO_CPU_SLPb_PU	11	0x1	Reserved for future use. This register controls no hardware
spare_15_12	15:12	0x0	Reserved for future use. This register controls no hardware
GPIO_TMDS_HPD_PD	16	0x0	Reserved for future use. This register controls no hardware
GPIO_DDC_DATA_PD	17	0x0	Reserved for future use. This register controls no hardware
GPIO_I2C_CLK_PD	18	0x0	Weak pull down control for the I2C_CLK pad when GPIO_I2C_CLK_OR is set 1=Weak pull down enabled 0=Weak pull down disabled
GPIO_I2C_DATA_PD	19	0x0	Weak pull down control for the I2C_DATA pad when GPIO_I2C_DATA_OR is set 1=Weak pull down enabled 0=Weak pull down disabled
GPIO_STRP_DATA_PD	20	0x0	Weak pull down control for the STRP_DATA pad when GPIO_STRP_DATA_OR is set 1=Weak pull down enabled 0=Weak pull down disabled
GPIO_DAC_SDA_PD	21	0x0	Reserved for future use. This register controls no hardware
GPIO_DAC_HSYNC_PD	22	0x0	Reserved for future use. This register controls no hardware
GPIO_DAC_VSYNC_PD	23	0x0	Reserved for future use. This register controls no hardware
GPIO_LVDS_ENA_BL_PD	24	0x0	Reserved for future use. This register controls no hardware
GPIO_LVDS_DIGON_PD	25	0x0	Reserved for future use. This register controls no hardware
GPIO_LVDS_BLON_PD	26	0x0	Reserved for future use. This register controls no hardware

GPIO_CPU_SLPb_PD	27	0x0	Reserved for future use. This register controls no hardware
spare_31_28	31:28	0x0	Reserved for future use. This register controls no hardware
GPIO_PAD_CNTL_PU_PD			

GPIO_PAD_SCHMEM_OE - RW - 32 bits - NBMISCIND:0x42			
Field Name	**Bits**	**Default**	**Description**
GPIO_TMDS_HPD_SCHMEN	0	0x1	Reserved for future use. This register controls no hardware
GPIO_DDC_DATA_SCHMEN	1	0x1	Reserved for future use. This register controls no hardware
GPIO_I2C_CLK_SCHMEN	2	0x1	Schmidt trigger enable control for the I2C_CLK pad receiver when GPIO_I2C_CLK_OR is set 1=Schmidt trigger input enabled 0=Schmidt trigger input disabled
GPIO_I2C_DATA_SCHMEN	3	0x1	Schmidt trigger enable control for the I2C_DATA pad receiver when GPIO_I2C_DATA_OR is set 1=Schmidt trigger input enabled 0=Schmidt trigger input disabled
GPIO_STRP_DATA_SCHMEN	4	0x1	Schmidt trigger enable control for the STRP_DATA pad receiver when GPIO_STRP_DATA_OR is set 1=Schmidt trigger input enabled 0=Schmidt trigger input disabled
GPIO_DAC_SDA_SCHMEN	5	0x1	Reserved for future use. This register controls no hardware
GPIO_DAC_HSYNC_SCHMEN	6	0x1	Reserved for future use. This register controls no hardware
GPIO_DAC_VSYNC_SCHMEN	7	0x1	Reserved for future use. This register controls no hardware
GPIO_LVDS_ENA_BL_SCHMEN	8	0x1	Reserved for future use. This register controls no hardware
GPIO_LVDS_DIGON_SCHMEN	9	0x1	Reserved for future use. This register controls no hardware
GPIO_LVDS_BLON_SCGMEN	10	0x1	Reserved for future use. This register controls no hardware
GPIO_CPU_SLPb_SCHMEN	11	0x1	Reserved for future use. This register controls no hardware
spare_15_12	15:12	0x0	Reserved for future use. This register controls no hardware
GPIO_TMDS_HPD_OE	16	0x0	Reserved for future use. This register controls no hardware
GPIO_DDC_DATA_OE	17	0x0	Reserved for future use. This register controls no hardware
GPIO_I2C_CLK_OE	18	0x0	Output enable control for the I2C_CLK pad when GPIO_I2C_CLK_OR is set 1=Output driver enabled 0=Output driver disabled
GPIO_I2C_DATA_OE	19	0x0	Output enable control for the I2C_DATA pad when GPIO_I2C_DATA_OR is set 1=Output driver enabled 0=Output driver disabled
GPIO_STRP_DATA_OE	20	0x0	Output enable control for the STRP_DATA pad when GPIO_STRP_DATA_OR is set 1=Output driver enabled 0=Output driver disabled
GPIO_DAC_SDA_OE	21	0x0	Reserved for future use. This register controls no hardware
GPIO_DAC_HSYNC_OE	22	0x0	Reserved for future use. This register controls no hardware
GPIO_DAC_VSYNC_OE	23	0x0	Reserved for future use. This register controls no hardware
GPIO_LVDS_ENA_BL_OE	24	0x0	Reserved for future use. This register controls no hardware
GPIO_LVDS_DIGON_OE	25	0x0	Reserved for future use. This register controls no hardware
GPIO_LVDS_BLON_OE	26	0x0	Reserved for future use. This register controls no hardware
GPIO_CPU_SLPb_OE	27	0x0	Reserved for future use. This register controls no hardware
spare_31_28	31:28	0x0	Reserved for future use. This register controls no hardware
GPIO_PAD_SCHMEM_OE			

GPIO_PAD_SP_SN - RW - 32 bits - NBMISCIND:0x43			
Field Name	**Bits**	**Default**	**Description**
GPIO_SRP	0	0x1	Reserved for future use. This register controls no hardware
GPIO_SRN	1	0x1	Reserved for future use. This register controls no hardware
GPIO_SP_3	2	0x0	Controls bit 3 of the P strength of PWM_GPIO, PCIE_RESET_GPIO, STRP_DATA, I2C_CLK and I2C_DATA pads when any of those pads are used in programmable GPIO mode

GPIO_SP_2	3	0x0	Controls bit 2 of the P strength of PWM_GPIO, PCIE_RESET_GPIO, STRP_DATA, I2C_CLK and I2C_DATA pads when any of those pads are used in programmable GPIO mode
GPIO_SP_1	4	0x1	Controls bit 1 of the P strength of PWM_GPIO, PCIE_RESET_GPIO, STRP_DATA, I2C_CLK and I2C_DATA pads when any of those pads are used in programmable GPIO mode
GPIO_SP_0	5	0x1	Controls bit 0 of the P strength of PWM_GPIO, PCIE_RESET_GPIO, STRP_DATA, I2C_CLK and I2C_DATA pads when any of those pads are used in programmable GPIO mode
GPIO_SN_3	6	0x0	Controls bit 3 of the N strength of PWM_GPIO, PCIE_RESET_GPIO, STRP_DATA, I2C_CLK and I2C_DATA pads when any of those pads are used in programmable GPIO mode
GPIO_SN_2	7	0x0	Controls bit 2 of the N strength of PWM_GPIO, PCIE_RESET_GPIO, STRP_DATA, I2C_CLK and I2C_DATA pads when any of those pads are used in programmable GPIO mode
GPIO_SN_1	8	0x1	Controls bit 1 of the N strength of PWM_GPIO, PCIE_RESET_GPIO, STRP_DATA, I2C_CLK and I2C_DATA pads when any of those pads are used in programmable GPIO mode
GPIO_SN_0	9	0x1	Controls bit 0 of the N strength of PWM_GPIO, PCIE_RESET_GPIO, STRP_DATA, I2C_CLK and I2C_DATA pads when any of those pads are used in programmable GPIO mode
GPIO_PAD_SP_SN			

GPIO_PAD - RW - 32 bits - NBMISCIND:0x46			
Field Name	**Bits**	**Default**	**Description**
GPIO_TMDS_HPD_OR	0	0x0	Reserved for future use. This register controls no hardware
GPIO_DDC_DATA_OR	1	0x0	Reserved for future use. This register controls no hardware
GPIO_I2C_CLK_OR	2	0x0	Converts the I2C_CLK pad to a software controllable GPIO pad
GPIO_I2C_DATA_OR	3	0x0	Converts the I2C_DATA pad to a software controllable GPIO pad
GPIO_STRP_DATA_OR	4	0x0	Converts the STRP_DATA pad to a software controllable GPIO pad
GPIO_DAC_SDA_OR	5	0x0	Reserved for future use. This register controls no hardware
GPIO_DAC_HSYNC_OR	6	0x0	Reserved for future use. This register controls no hardware
GPIO_DAC_VSYNC_OR	7	0x0	Reserved for future use. This register controls no hardware
GPIO_LVDS_ENA_BL_OR	8	0x0	Reserved for future use. This register controls no hardware
GPIO_LVDS_DIGON_OR	9	0x0	Reserved for future use. This register controls no hardware
GPIO_LVDS_BLON_OR	10	0x0	Reserved for future use. This register controls no hardware
GPIO_CPU_SLPb_OR	11	0x0	Reserved for future use. This register controls no hardware
PAD_0_spare_15_12	15:12	0x0	Reserved for future use. This register controls no hardware
GPIO_TMDS_HPD_A	16	0x0	Reserved for future use. This register controls no hardware
GPIO_DDC_DATA_A	17	0x0	Reserved for future use. This register controls no hardware
GPIO_I2C_CLK_A	18	0x0	Indicates the input state of the I2C_CLK pad
GPIO_I2C_DATA_A	19	0x0	Indicates the input state of the I2C_DATA pad
GPIO_STRP_DATA_A	20	0x0	Indicates the input state of the STRP_DATA pad
GPIO_DAC_SDA_A	21	0x0	Reserved for future use. This register controls no hardware
GPIO_DAC_HSYNC_A	22	0x0	Reserved for future use. This register controls no hardware
GPIO_DAC_VSYNC_A	23	0x0	Reserved for future use. This register controls no hardware
GPIO_LVDS_ENA_BL_A	24	0x0	Reserved for future use. This register controls no hardware
GPIO_LVDS_DIGON_A	25	0x0	Reserved for future use. This register controls no hardware
GPIO_LVDS_BLON_A	26	0x0	Reserved for future use. This register controls no hardware
GPIO_CPU_SLPb_A	27	0x0	Reserved for future use. This register controls no hardware
PAD_0_spare_31_28	31:28	0x0	Reserved for future use. This register controls no hardware
GPIO_PAD			

IOC_JTAG_CNTL - RW - 32 bits - NBMISCIND:0x47			
Field Name	**Bits**	**Default**	**Description**
JTAGARB_DEL	15:0	0xb	Selects delay between JTAG cycles issued to nb
JTAG arbitration control			

PCIE_GPP_P2P_CONTROL - RW - 32 bits - NBMISCIND:0x48			
Field Name	**Bits**	**Default**	**Description**
D2P2PSnoopMode	0	0x1	
D3P2PSnoopMode	1	0x1	
D11P2PSnoopMode	2	0x1	
D12P2PSnoopMode	3	0x1	
D2P2PRelaxMode	4	0x1	
D3P2PRelaxMode	5	0x1	
D11P2PRelaxMode	6	0x1	
D12P2PRelaxMode	7	0x1	
P2PPcieDis	8	0x1	
GPP1_DisBuffer	9	0x0	
GPP2_DisBuffer	10	0x0	
Eff_rr_mod	11	0x0	
CfgPciC_DisP2pLock	12	0x0	
Eff_rr_mode_GPP2	13	0x0	N-weighted round-robin instead of checking addresses
Eff_mask	31:16	0xffff	

PCIE_GPP_P2P_ARBITRER_CONTROL - RW - 32 bits - NBMISCIND:0x49			
Field Name	**Bits**	**Default**	**Description**
Eff_size_a	7:0	0x4	Number of times one selects a client a before forced to switch
Eff_size_b	15:8	0x4	Number of times one selects a client b before forced to switch
Eff_size_c	23:16	0x8	Number of times one selects a client c before forced to switch
Eff_size_c_GPP2	31:24	0x8	Number of times one selects a client c on GPP2 before forced to switch

EFUSE_CFG_HW_CONFIG_4 - RW - 32 bits - NBMISCIND:0x4A			
Field Name	**Bits**	**Default**	**Description**
Reserved	20:0		Reserved
E77FixCap	21		1 = Chipset is capable of supporting the workaround for erratum 77 0 = Chipset is not capable of supporting the workaround for erratum 77
Reserved	31:22		Reserved

CFG_IOC_TOM3 - RW - 32 bits - NBMISCIND:0x4E			
Field Name	**Bits**	**Default**	**Description**
TOM3_LIMIT	29:0	0x0	TOM3 defines the top of physical memory between 40-bit and 52-bit space inclusive of TOM3. This register contains address bits 51:22 of TOM3. Lower address bits are implicitly set to 1.
TOM3_ENABLE	31	0x0	Enables TOM3 for memory-space decoding between the 40 and 52-bit address space

PCIE_LINK_DISABLE_CONTROL2 - RW - 32 bits - NBMISCIND:0x4F			
Field Name	**Bits**	**Default**	**Description**
FATAL_GPP1_C_mask	0	0x0	When set to 1, fatal errors detected by the bridge 6 link result in the bridge 6 link being disabled
NON_FATAL_GPP1_C_mask	1	0x0	When set to 1, non-fatal errors detected by the bridge 6 link result in the bridge 6 link being disabled

CORR_GPP1_C_mask	2	0x0	When set to 1, correctable errors detected by the bridge 6 link result in the bridge 6 link being disabled
SYNCFLD_GPP1_C_mask	3	0x0	When set to 1, HyperTransport syncfloods result in the bridge 6 link being disabled
FATAL_GPP1_D_mask	4	0x0	When set to 1, fatal errors detected by the bridge 7 link result in the bridge 7 link being disabled
NON_FATAL_GPP1_D_mask	5	0x0	When set to 1, non-fatal errors detected by the bridge 7 link result in the bridge 7 link being disabled
CORR_GPP1_D_mask	6	0x0	When set to 1, correctable errors detected by the bridge 7 link result in the bridge 7 link being disabled
SYNCFLD_GPP1_D_mask	7	0x0	When set to 1, HyperTransport syncfloods result in the bridge 7 link being disabled
FATAL_GPP1_E_mask	8	0x0	When set to 1, fatal errors detected by the bridge 9 link result in the bridge 9 link being disabled
NON_FATAL_GPP1_E_mask	9	0x0	When set to 1, non-fatal errors detected by the bridge 9 link result in the bridge 9 link being disabled
CORR_GPP1_E_mask	10	0x0	When set to 1, correctable errors detected by the bridge 9 link result in the bridge 9 link being disabled
SYNCFLD_GPP1_E_mask	11	0x0	When set to 1, HyperTransport syncfloods result in the bridge 9 link being disabled
FATAL_GPP1_F_mask	12	0x0	When set to 1, fatal errors detected by the bridge 10 link result in the bridge 10 link being disabled
NON_FATAL_GPP1_F_mask	13	0x0	When set to 1, non-fatal errors detected by the bridge 10 link result in the bridge 10 link being disabled
CORR_GPP1_F_mask	14	0x0	When set to 1, correctable errors detected by the bridge 10 link result in the bridge 10 link being disabled
SYNCFLD_GPP1_F_mask	15	0x0	When set to 1, HyperTransport syncfloods result in the bridge 10 link being disabled
RESERVED_31_16	31:16	0x0	Reserved for future use. This register controls no hardware

IOC_PCIE_D2_CSR_Count - RW - 32 bits - NBMISCIND:0x50			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	Sets the delay in core clocks between re-issuing configuration space requests through PCI Express bridge 2 that previously returned CRS completion status when IOC_PCIE_D2_CNTL[CsrEnable] is set
CsrLimitCount	31:24	0x0	Sets the number of times configuration space requests through PCI Express bridge 2 are retried when IOC_PCIE_D2_CNTL[CsrEnable] is set before returning CRS back to the HTIU. HTIU converts CRS status to Master Abort when returning the response to the processor
CSR Register			

IOC_PCIE_D2_CNTL - RW - 32 bits - NBMISCIND:0x51			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	Forces DMA requests coming through PCI Express bridge 2 to have the relaxed ordering attribute set when IOC_PCIE_D2_CNTL[DmaFixAttrEn] is set
DmaForceSnoop	1	0x0	Forces DMA requests coming through PCI Express bridge 2 to have the snoop attribute set when IOC_PCIE_D2_CNTL[DmaFixAttrEn] is set
DmaFixAttrEn	2	0x0	Allow forcing of DMA attributes
P2pDis	3	0x0	Prevents peer to peer transactions from targetting devices behind this bridge
BMSetDis	7	0x0	Disables BMSTS from being set by DMA requests coming through this bridge

XactOrder	8	0x1	Forces ordering between DMA writes and cpu completions
BlockNonSp	9	0x0	Blocks Nonsnoop DMA
BlockSnoop	10	0x0	Blocks Snoop DMA
MstRelaxOrder	11	0x0	Forces relax ordering on cpu requests to this deivce
MstRelaxOrderEn	12	0x0	Allows Forcing of relax ordering on cpu requests to this device
MstNSoopEn	13	0x0	0=Host requests routed through PCI Express bridge 2 are issued with the no-snoop attribute 1=Host requests routed through PCI Express bridge 2 are issued with the snoop attribute
ExtDevPlug	16	0x0	Rorces logical detection of an external device on the PCI Express bridge 2 port
ExtDevCsrEn	17	0x0	When set, the CSR retry limit is ignored for PCI Express bridge 2 when a device is detected on the far side of the PCI Express link and the link is up
CsrEnable	18	0x0	When set, configuration requests through PCI Express bridge 2 that return CRS completion status are retried automatically
IntSelMod	19	0x0	Interrupt select between ABCD or EFGH
SetPowEn	20	0x0	Allows set slot power messages to this device
Device Specific controls			

IOC_PCIE_D3_CSR_Count - RW - 32 bits - NBMISCIND:0x52			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	Sets the delay in core clocks between re-issuing configuration space requests through PCI Express bridge 3 that previously returned CRS completion status when IOC_PCIE_D3_CNTL[CsrEnable] is set
CsrLimitCount	31:24	0x0	Sets the number of times configuration space requests through PCI Express bridge 3 are retried when IOC_PCIE_D3_CNTL[CsrEnable] is set before returning CRS back to the HTIU. HTIU converts CRS status to Master Abort when returning the response to the processor
CSR Register			

IOC_PCIE_D3_CNTL - RW - 32 bits - NBMISCIND:0x53			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	Forces DMA requests coming through PCI Express bridge 3 to have the relaxed ordering attribute set when IOC_PCIE_D3_CNTL[DmaFixAttrEn] is set
DmaForceSnoop	1	0x0	Forces DMA requests coming through PCI Express bridge 3 to have the snoop attribute set when IOC_PCIE_D3_CNTL[DmaFixAttrEn] is set
DmaFixAttrEn	2	0x0	Allows forcing of DMA attributes
P2pDis	3	0x0	Prevents peer to peer transactions from targetting devices behind this bridge
BMSetDis	7	0x0	Disables BMSTS from being set by DMA requests coming through this bridge
XactOrder	8	0x1	Forces ordering between DMA writes and cpu completions
BlockNonSp	9	0x0	Blocks Nonsnoop DMA
BlockSnoop	10	0x0	Blocks Snoop DMA
MstRelaxOrder	11	0x0	Forces relax ordering on cpu requests to this deivce
MstRelaxOrderEn	12	0x0	Allows Forcing of relax ordering on cpu requests to this device
MstNSoopEn	13	0x0	0=Host requests routed through PCI Express bridge 3 are issued with the no-snoop attribute 1=Host requests routed through PCI Express bridge 3 are issued with the snoop attribute
ExtDevPlug	16	0x0	Forces logical detection of an external device on the PCI Express bridge 3 port

ExtDevCsrEn	17	0x0	When set, the CSR retry limit is ignored for PCI Express bridge 3 when a device is detected on the far side of the PCI Express link and the link is up
CsrEnable	18	0x0	When set, configuration requests through PCI Express bridge 3 that return CRS completion status are retried automatically
IntSelMod	19	0x0	Interrupt select between ABCD or EFGH
SetPowEn	20	0x0	Allows set slot power messages to this device
Device Specific controls			

IOC_PCIE_D4_CSR_Count - RW - 32 bits - NBMISCIND:0x54			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	Sets the delay in core clocks between re-issuing configuration space requests through PCI Express bridge 4 that previously returned CRS completion status when IOC_PCIE_D4_CNTL[CsrEnable] is set
CsrLimitCount	31:24	0x0	Sets the number of times configuration space requests through PCI Express bridge 4 are retried when IOC_PCIE_D4_CNTL[CsrEnable] is set before returning CRS back to the HTIU. HTIU converts CRS status to Master Abort when returning the response to the processor
CSR Register			

IOC_PCIE_D4_CNTL - RW - 32 bits - NBMISCIND:0x55			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	Forces DMA requests coming through PCI Express bridge 4 to have the relaxed ordering attribute set when IOC_PCIE_D4_CNTL[DmaFixAttrEn] is set
DmaForceSnoop	1	0x0	Forces DMA requests coming through PCI Express bridge 4 to have the snoop attribute set when IOC_PCIE_D4_CNTL[DmaFixAttrEn] is set
DmaFixAttrEn	2	0x0	Allows forcing of DMA attributes
P2pDis	3	0x0	Prevents peer to peer transactions from targetting devices behind this bridge
BMSetDis	7	0x0	Disables BMSTS from being set by DMA requests coming through this bridge
XactOrder	8	0x1	Forces ordering between DMA writes and cpu completions
BlockNonSp	9	0x0	Blocks Nonsnoop DMA
BlockSnoop	10	0x0	Blocks Snoop DMA
MstRelaxOrder	11	0x0	Forces relax ordering on cpu requests to this deivce
MstRelaxOrderEn	12	0x0	Allows Forcing of relax ordering on cpu requests to this device
MstNSoopEn	13	0x0	0=Host requests routed through PCI Express bridge 4 are issued with the no-snoop attribute 1=Host requests routed through PCI Express bridge 4 are issued with the snoop attribute
ExtDevPlug	16	0x0	Forces logical detection of an external device on the PCI Express bridge 4 port
ExtDevCsrEn	17	0x0	When set, the CSR retry limit is ignored for PCI Express bridge 4 when a device is detected on the far side of the PCI Express link and the link is up
CsrEnable	18	0x0	When set, configuration requests through PCI Express bridge 4 that return CRS completion status are retried automatically
IntSelMod	19	0x0	Interrupt select between ABCD or EFGH
SetPowEn	20	0x0	Allows set slot power messages to this device
Device Specific controls			

IOC_PCIE_D5_CSR_Count - RW - 32 bits - NBMISCIND:0x56			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	Sets the delay in core clocks between re-issuing configuration space requests through PCI Express bridge 5 that previously returned CRS completion status when IOC_PCIE_D5_CNTL[CsrEnable] is set
CsrLimitCount	31:24	0x0	Sets the number of times configuration space requests through PCI Express bridge 5 are retried when IOC_PCIE_D5_CNTL[CsrEnable] is set before returning CRS back to the HTIU. HTIU converts CRS status to Master Abort when returning the response to the processor
CSR Register			

IOC_PCIE_D5_CNTL - RW - 32 bits - NBMISCIND:0x57			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	Forces DMA requests coming through PCI Express bridge 5 to have the relaxed ordering attribute set when IOC_PCIE_D5_CNTL[DmaFixAttrEn] is set
DmaForceSnoop	1	0x0	Forces DMA requests coming through PCI Express bridge 5 to have the snoop attribute set when IOC_PCIE_D5_CNTL[DmaFixAttrEn] is set

DmaFixAttrEn	2	0x0	Allows forcing of DMA attributes
P2pDis	3	0x0	Prevents peer to peer transactions from targetting devices behind this bridge
BMSetDis	7	0x0	Disables BMSTS from being set by DMA requests coming through this bridge
XactOrder	8	0x1	Forces ordering between DMA writes and cpu completions
BlockNonSp	9	0x0	Blocks Nonsnoop DMA
BlockSnoop	10	0x0	Blocks Snoop DMA
MstRelaxOrder	11	0x0	Forces relax ordering on cpu requests to this deivce
MstRelaxOrderEn	12	0x0	Allows Forcing of relax ordering on cpu requests to this device
MstNSoopEn	13	0x0	0=Host requests routed through PCI Express bridge 5 are issued with the no-snoop attribute 1=Host requests routed through PCI Express bridge 5 are issued with the snoop attribute
ExtDevPlug	16	0x0	Forces logical detection of an external device on the PCI Express bridge 5 port
ExtDevCsrEn	17	0x0	When set, the CSR retry limit is ignored for PCI Express bridge 5 when a device is detected on the far side of the PCI Express link and the link is up
CsrEnable	18	0x0	When set, configuration requests through PCI Express bridge 5 that return CRS completion status are retried automatically
IntSelMod	19	0x0	Interrupt select between ABCD or EFGH
SetPowEn	20	0x0	Allows set slot power messages to this device
Device Specific controls			

IOC_PCIE_D6_CSR_Count - RW - 32 bits - NBMISCIND:0x58			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	Sets the delay in core clocks between re-issuing configuration space requests through PCI Express bridge 6 that previously returned CRS completion status when IOC_PCIE_D6_CNTL[CsrEnable] is set
CsrLimitCount	31:24	0x0	Sets the number of times configuration space requests through PCI Express bridge 6 are retried when IOC_PCIE_D6_CNTL[CsrEnable] is set before returning CRS back to the HTIU. HTIU converts CRS status to Master Abort when returning the response to the processor
CSR Register			

IOC_PCIE_D6_CNTL - RW - 32 bits - NBMISCIND:0x59			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	Forces DMA requests coming through PCI Express bridge 6 to have the relaxed ordering attribute set when IOC_PCIE_D6_CNTL[DmaFixAttrEn] is set
DmaForceSnoop	1	0x0	Forces DMA requests coming through PCI Express bridge 6 to have the snoop attribute set when IOC_PCIE_D6_CNTL[DmaFixAttrEn] is set
DmaFixAttrEn	2	0x0	Allows forcing of DMA attributes
P2pDis	3	0x0	Prevents peer to peer transactions from targetting devices behind this bridge
BMSetDis	7	0x0	Disables BMSTS from being set by DMA requests coming through this bridge
XactOrder	8	0x1	Forces ordering between DMA writes and cpu completions
BlockNonSp	9	0x0	Blocks Nonsnoop DMA
BlockSnoop	10	0x0	Blocks Snoop DMA
MstRelaxOrder	11	0x0	Forces relax ordering on cpu requests to this deivce
MstRelaxOrderEn	12	0x0	Allows Forcing of relax ordering on cpu requests to this device

MstNSoopEn	13	0x0	0=Host requests routed through PCI Express bridge 6 are issued with the no-snoop attribute 1=Host requests routed through PCI Express bridge 6 are issued with the snoop attribute
ExtDevPlug	16	0x0	Forces logical detection of an external device on the PCI Express bridge 6 port
ExtDevCsrEn	17	0x0	When set, the CSR retry limit is ignored for PCI Express bridge 6 when a device is detected on the far side of the PCI Express link and the link is up
CsrEnable	18	0x0	When set, configuration requests through PCI Express bridge 6 that return CRS completion status are retried automatically
IntSelMod	19	0x0	Interrupt select between ABCD or EFGH
SetPowEn	20	0x0	Allows set slot power messages to this device
Device Specific controls			

IOC_PCIE_D7_CSR_Count - RW - 32 bits - NBMISCIND:0x5A			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	Sets the delay in core clocks between re-issuing configuration space requests through PCI Express bridge 7 that previously returned CRS completion status when IOC_PCIE_D7_CNTL[CsrEnable] is set
CsrLimitCount	31:24	0x0	Sets the number of times configuration space requests through PCI Express bridge 7 are retried when IOC_PCIE_D7_CNTL[CsrEnable] is set before returning CRS back to the HTIU. HTIU converts CRS status to Master Abort when returning the response to the processor
CSR Register			

IOC_PCIE_D7_CNTL - RW - 32 bits - NBMISCIND:0x5B			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	Forces DMA requests coming through PCI Express bridge 7 to have the relaxed ordering attribute set when IOC_PCIE_D7_CNTL[DmaFixAttrEn] is set
DmaForceSnoop	1	0x0	Forces DMA requests coming through PCI Express bridge 7 to have the snoop attribute set when IOC_PCIE_D7_CNTL[DmaFixAttrEn] is set
DmaFixAttrEn	2	0x0	Allows forcing of DMA attributes
P2pDis	3	0x0	Prevents peer to peer transactions from targetting devices behind this bridge
BMSetDis	7	0x0	Disables BMSTS from being set by DMA requests coming through this bridge
XactOrder	8	0x1	Forces ordering between DMA writes and cpu completions
BlockNonSp	9	0x0	Blocks Nonsnoop DMA
BlockSnoop	10	0x0	Blocks Snoop DMA
MstRelaxOrder	11	0x0	Forces relax ordering on cpu requests to this deivce
MstRelaxOrderEn	12	0x0	Allows Forcing of relax ordering on cpu requests to this device
MstNSoopEn	13	0x0	0=Host requests routed through PCI Express bridge 7 are issued with the no-snoop attribute 1=Host requests routed through PCI Express bridge 7 are issued with the snoop attribute
ExtDevPlug	16	0x0	Forces logical detection of an external device on the PCI Express bridge 7 port
ExtDevCsrEn	17	0x0	When set, the CSR retry limit is ignored for PCI Express bridge 7 when a device is detected on the far side of the PCI Express link and the link is up
CsrEnable	18	0x0	When set, configuration requests through PCI Express bridge 7 that return CRS completion status are retried automatically

IntSelMod	19	0x0	Interrupt select between ABCD or EFGH
SetPowEn	20	0x0	Allows set slot power messages to this device
Device Specific controls			

IOC_PCIE_D9_CSR_Count - RW - 32 bits - NBMISCIND:0x5C			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	Sets the delay in core clocks between re-issuing configuration space requests through PCI Express bridge 9 that previously returned CRS completion status when IOC_PCIE_D9_CNTL[CsrEnable] is set
CsrLimitCount	31:24	0x0	Sets the number of times configuration space requests through PCI Express bridge 9 are retried when IOC_PCIE_D9_CNTL[CsrEnable] is set before returning CRS back to the HTIU. HTIU converts CRS status to Master Abort when returning the response to the processor
CSR Register			

IOC_PCIE_D9_CNTL - RW - 32 bits - NBMISCIND:0x5D			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	Forces DMA requests coming through PCI Express bridge 9 to have the relaxed ordering attribute set when IOC_PCIE_D9_CNTL[DmaFixAttrEn] is set
DmaForceSnoop	1	0x0	Forces DMA requests coming through PCI Express bridge 9 to have the snoop attribute set when IOC_PCIE_D9_CNTL[DmaFixAttrEn] is set
DmaFixAttrEn	2	0x0	Allows forcing of DMA attributes
P2pDis	3	0x0	Prevents peer to peer transactions from targetting devices behind this bridge
BMSetDis	7	0x0	Disables BMSTS from being set by DMA requests coming through this bridge
XactOrder	8	0x1	Forces ordering between DMA writes and cpu completions
BlockNonSp	9	0x0	Blocks Nonsnoop DMA
BlockSnoop	10	0x0	Blocks Snoop DMA
MstRelaxOrder	11	0x0	Forces relax ordering on cpu requests to this deivce
MstRelaxOrderEn	12	0x0	Allows Forcing of relax ordering on cpu requests to this device
MstNSoopEn	13	0x0	0=Host requests routed through PCI Express bridge 9 are issued with the no-snoop attribute 1=Host requests routed through PCI Express bridge 9 are issued with the snoop attribute
ExtDevPlug	16	0x0	Forces logical detection of an external device on the PCI Express bridge 9 port
ExtDevCsrEn	17	0x0	When set, the CSR retry limit is ignored for PCI Express bridge 9 when a device is detected on the far side of the PCI Express link and the link is up
CsrEnable	18	0x0	When set, configuration requests through PCI Express bridge 9 that return CRS completion status are retried automatically
IntSelMod	19	0x0	Interrupt select between ABCD or EFGH
SetPowEn	20	0x0	Allows set slot power messages to this device
Device Specific controls			

IOC_PCIE_D10_CSR_Count - RW - 32 bits - NBMISCIND:0x5E			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	Sets the delay in core clocks between re-issuing configuration space requests through PCI Express® bridge 10 that previously returned CRS completion status when IOC_PCIE_D10_CNTL[CsrEnable] is set
CsrLimitCount	31:24	0x0	Sets the number of times configuration space requests through PCI Express bridge 10 are retried when IOC_PCIE_D10_CNTL[CsrEnable] is set before returning CRS back to the HTIU. HTIU converts CRS status to Master Abort when returning the response to the processor
CSR Register			

IOC_PCIE_D10_CNTL - RW - 32 bits - NBMISCIND:0x5F			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	Forces DMA requests coming through PCI Express bridge 10 to have the relaxed ordering attribute set when IOC_PCIE_D10_CNTL[DmaFixAttrEn] is set
DmaForceSnoop	1	0x0	Forces DMA requests coming through PCI Express bridge 10 to have the snoop attribute set when IOC_PCIE_D10_CNTL[DmaFixAttrEn] is set
DmaFixAttrEn	2	0x0	Allows forcing of DMA attributes
P2pDis	3	0x0	Prevents peer to peer transactions from targetting devices behind this bridge
BMSetDis	7	0x0	Disables BMSTS from being set by DMA requests coming through this bridge
XactOrder	8	0x1	Forces ordering between DMA writes and cpu completions
BlockNonSp	9	0x0	Blocks Nonsnoop DMA
BlockSnoop	10	0x0	Blocks Snoop DMA
MstRelaxOrder	11	0x0	Forces relax ordering on cpu requests to this deivce
MstRelaxOrderEn	12	0x0	Allows Forcing of relax ordering on cpu requests to this device
MstNSoopEn	13	0x0	0=Host requests routed through PCI Express bridge 10 are issued with the no-snoop attribute 1=Host requests routed through PCI Express bridge 10 are issued with the snoop attribute
ExtDevPlug	16	0x0	Forces logical detection of an external device on the PCI Express bridge 10 port
ExtDevCsrEn	17	0x0	When set, the CSR retry limit is ignored for PCI Express bridge 10 when a device is detected on the far side of the PCI Express link and the link is up
CsrEnable	18	0x0	When set, configuration requests through PCI Express bridge 10 that return CRS completion status are retried automatically
IntSelMod	19	0x0	Interrupt select between ABCD or EFGH
SetPowEn	20	0x0	Allows set slot power messages to this device
Device Specific controls			

IOC_PCIE_D11_CSR_Count - RW - 32 bits - NBMISCIND:0x60			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	Sets the delay in core clocks between re-issuing configuration space requests through PCI Express bridge 11 that previously returned CRS completion status when IOC_PCIE_D11_CNTL[CsrEnable] is set
CsrLimitCount	31:24	0x0	Sets the number of times configuration space requests through PCI Express bridge 11 are retried when IOC_PCIE_D11_CNTL[CsrEnable] is set before returning CRS back to the HTIU. HTIU converts CRS status to Master Abort when returning the response to the processor
CSR Register			

IOC_PCIE_D11_CNTL - RW - 32 bits - NBMISCIND:0x61			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	Forces DMA requests coming through PCI Express bridge 11 to have the relaxed ordering attribute set when IOC_PCIE_D11_CNTL[DmaFixAttrEn] is set
DmaForceSnoop	1	0x0	Forces DMA requests coming through PCI Express bridge 11 to have the snoop attribute set when IOC_PCIE_D11_CNTL[DmaFixAttrEn] is set
DmaFixAttrEn	2	0x0	Allows forcing of DMA attributes
P2pDis	3	0x0	Prevents peer to peer transactions from targetting devices behind this bridge
BMSetDis	7	0x0	Disables BMSTS from being set by DMA requests coming through this bridge
XactOrder	8	0x1	Forces ordering between DMA writes and cpu completions
BlockNonSp	9	0x0	Blocks Nonsnoop DMA
BlockSnoop	10	0x0	Blocks Snoop DMA
MstRelaxOrder	11	0x0	Forces relax ordering on cpu requests to this deivce
MstRelaxOrderEn	12	0x0	Allows Forcing of relax ordering on cpu requests to this device
MstNSoopEn	13	0x0	0=Host requests routed through PCI Express bridge 11 are issued with the no-snoop attribute 1=Host requests routed through PCI Express bridge 11 are issued with the snoop attribute
ExtDevPlug	16	0x0	Forces logical detection of an external device on the PCI Express bridge 11 port
ExtDevCsrEn	17	0x0	When set, the CSR retry limit is ignored for PCI Express bridge 11 when a device is detected on the far side of the PCI Express link and the link is up
CsrEnable	18	0x0	When set, configuration requests through PCI Express bridge 11 that return CRS completion status are retried automatically
IntSelMod	19	0x0	Interrupt select between ABCD or EFGH
SetPowEn	20	0x0	Allows set slot power messages to this device
Device Specific controls			

IOC_PCIE_D12_CSR_Count - RW - 32 bits - NBMISCIND:0x62			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	Sets the delay in core clocks between re-issuing configuration space requests through PCI Express bridge 12 that previously returned CRS completion status when IOC_PCIE_D12_CNTL[CsrEnable] is set
CsrLimitCount	31:24	0x0	Sets the number of times configuration space requests through PCI Express bridge 12 are retried when IOC_PCIE_D12_CNTL[CsrEnable] is set before returning CRS back to the HTIU. HTIU converts CRS status to Master Abort when returning the response to the processor
CSR Register			

IOC_PCIE_D12_CNTL - RW - 32 bits - NBMISCIND:0x63			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	Forces DMA requests coming through PCI Express bridge 12 to have the relaxed ordering attribute set when IOC_PCIE_D12_CNTL[DmaFixAttrEn] is set
DmaForceSnoop	1	0x0	Forces DMA requests coming through PCI Express bridge 12 to have the snoop attribute set when IOC_PCIE_D12_CNTL[DmaFixAttrEn] is set
DmaFixAttrEn	2	0x0	Allows forcing of DMA attributes
P2pDis	3	0x0	Prevents peer to peer transactions from targetting devices behind this bridge
BMSetDis	7	0x0	Disables BMSTS from being set by DMA requests coming through this bridge
XactOrder	8	0x1	Forces ordering between DMA writes and cpu completions
BlockNonSp	9	0x0	Blocks Nonsnoop DMA
BlockSnoop	10	0x0	Blocks Snoop DMA
MstRelaxOrder	11	0x0	Forces relax ordering on cpu requests to this deivce
MstRelaxOrderEn	12	0x0	Allows Forcing of relax ordering on cpu requests to this device
MstNSoopEn	13	0x0	0=Host requests routed through PCI Express bridge 12 are issued with the no-snoop attribute 1=Host requests routed through PCI Express bridge 12 are issued with the snoop attribute
ExtDevPlug	16	0x0	Forces logical detection of an external device on the PCI Express bridge 12 port
ExtDevCsrEn	17	0x0	When set, the CSR retry limit is ignored for PCI Express bridge 12 when a device is detected on the far side of the PCI Express link and the link is up
CsrEnable	18	0x0	When set, configuration requests through PCI Express bridge 12 that return CRS completion status are retried automatically
IntSelMod	19	0x0	Interrupt select between ABCD or EFGH
SetPowEn	20	0x0	Allows set slot power messages to this device
Device Specific controls			

StrapsOutputMux_4 - RW - 32 bits - NBMISCIND:0x64			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_4	31:0	0x0	

StrapsOutputMux_5 - RW - 32 bits - NBMISCIND:0x65			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_5	31:0	0x0	

StrapsOutputMux_6 - RW - 32 bits - NBMISCIND:0x66			
Field Name	**Bits**	**Default**	**Description**
detector_enable_all_valid	0	0x0	
B_PG2REFCLK_TERM_EN_FC_sb	1	0x0	PCIe reference clock termination enable
B_PRX_PDNB_STRAP_all_valid	2	0x0	
STRAP_BIF_TX_PDNB_MODE_all_valid	3	0x0	Controls TX_PDNB signal to the PHY 0: low during global rest, toggles high after global reset de-asserted. 1: always high during boot-up sequence.
STRAP_BIF_SYMALIGN_HW_DEBUG_sb	4	0x0	This strap is for debug purpose: 0: debug off 1: debug on
STRAP_BIF_SYMALIGN_MODE_sb	5	0x0	This strap controls 'Data Valid' generation bit in PHY 0: Relax Mode - update symbols immediately when any bit shift is detected, i.e., 'Data Valid' will always assert. 1: Aggressive Mode - requires confirmation before muxing out the data
spare_7_6	7:6	0x0	
B_PG2REFCLK_TERM_VAL_sb	9:8	0x0	PCIe reference clock termination value: 00: 100 Ohms differential 01: 100 - x Ohms differential 10: 100 + x Ohms differential 11: 100 + 2x Ohms differential
STRAP_BIF_BYPASS_SCRAMBLER_sb	10	0x0	Debug: Bypass the scrambling circuitry across all lanes. 0: normal 1: bypass
STRAP_PHY_RX_INCAL_FORCE_all_valid	11	0x0	Use RX_PDNB to gate off FRONTEND_EN for inactive lanes.
STRAP_BIF_SKIP_INTERVAL_sb	14:12	0x0	Frequency of skip generation 000: 1 SKIP every 1506 clocks 001: 1 SKIP every 1538 clocks 010: 1 SKIP every 1359 clocks 011: 1 SKIP every 1180 clocks 100: 1 SKIP every 2048 clocks 101: 1 SKIP every 512 clocks 110: 1 SKIP every 128 clocks 111: SKIP insertion disabled
STRAP_BIF_EXIT_LATENCY_sb	18:15	0x0	See Latency Table below
STRAP_BIF_REVERSE_LC_LANES_sb	19	0x0	Reverse lanes per port in the LC (1 bit per port), this is for EP
STRAP_BIF_REVERSE_LANES_sb	20	0x0	Reverse lanes per port in the PHY (1 bit per port)
STRAP_BIF_REVERSE_ALL_sb	21	0x0	Reverse all lanes (lane 0->3, lane 3->0). This is independent of port reversal
STRAP_BIF_FTS_yTSx_COUNT_sb	23:22	0x0	STRAP_BIF_FTS_yTSx_COUNT 00: N_FTS training sets 01: 512 + N_FTS training sets 10: 4096 + N_FTS training sets 11: 4608 + N_FTS training sets This is an encoded 3-bit field: yTSx_COUNT.
STRAP_BIF_SHORT_yTSx_COUNT_sb	25:24	0x0	STRAP_BIF_MED_yTSx_COUNT 00: 16 sets 01: N/A 10: 128 sets 11: 144 sets This is an encoded 3-bit field: yTSx_COUNT.

STRAP_BIF_MED_yTSx_COUNT_sb	27:26	0x0	STRAP_BIF_MED_yTSx_COUNT 00: 16 sets 01: N/A 10: 128 sets 11: 144 sets This is an encoded 3-bit field: yTSx_COUNT.
STRAP_BIF_LONG_yTSx_COUNT_sb	29:28	0x0	STRAP_BIF_LONG_yTSx_COUNT 00 1024 sets of selected types have been sent (TS1, TS2, FTS, training sets, skips, electrical idles, etc.) 01: Not allowable 10: 8096 sets of selected types 11: 9120 sets of selected types This is an encoded 3-bit field: yTSx_COUNT.
STRAP_BIF_FORCE_GEN2_MODE_sb	30	0x0	To force PHY to operate at GEN2 speed without LC to go through GEN2 speed negotiation. This mode is intended to be used in ATE only.
B_PRX_DET_BLOCK_sb	31	0x0	When asserted, sets P_BRX_ELEC_IDLE low.

StrapsOutputMux_6 for PCIe

Latency Table for STRAP_BIF_EXIT_LATENCY_sb

		L0s Exit Latency	L1 Exit Latency	N_FTS	L0s Acceptable Exit Latency	L1 Acceptable Exit Latency	L0 Supported	L1 Supported
0	**sure to be enabled**	<64ns	<1us	24	2-4us	>64us	1	1
1	**disabled**	>4us	>64us	255	<64ns	<1us	0	0
2	**no L0s**	>4us	<1us	255	<64ns	>64us	0	1
3	**sub-optimal**	128-256ns	1-2us	24	512-1000ns	>64us	1	1
4	**optimal**	64-128ns	<1us	12	256-512ns	>64us	1	1
5	**sub-optimal, no L0s**	>4us	1-2us	255	<64ns	>64us	0	1
6	**sub-optimal, no L1**	128-256ns	>64us	24	512-1000ns	<1us	1	0
7	**less acc latency**	64-128ns	<1us	12	128-256ns	>64us	1	1
8	**more acc latency**	64-128ns	<1us	12	512-1000ns	>64us	1	1
9	**more exit latency**	128-256ns	1-2us	24	256-512ns	>64us	1	1
A	**no L1**	64-128ns	>64us	12	256-512ns	<1us	1	0
B	**less FTS**	64-128ns	<1us	4	256-512ns	>64us	1	1
C	**still more exit latency**	512-1us	4-8us	48	256-512ns	>64us	1	1
D	**aggressive**	<64ns	<1us	6	128-256ns	>64us	1	1
E	**slack**	512-1us	8-16us	48	512-1us	>64us	1	1
F	**slackest**	2-4us	>64us	255	2-4us	>64us	1	1

StrapsOutputMux_7 - RW - 32 bits - NBMISCIND:0x67			
Field Name	**Bits**	**Default**	**Description**
STRAP_BIF_LINK_CONFIG	4:0	0x1	12 possible configurations (A-L)
STRAP_BIF_BYPASS_RCVR_DET_sb	5	0x0	1: bypass receiver detection in LTSSM 0: do spec compliant rcvr detection
STRAP_BIF_COMPLIANCE_DIS_sb	6	0x0	Strap Compliance Disable: Used in LTSSM 0: Allow LTSSM to enter compliance state 1: Disable compliance state
spare_7	7	0x0	
EFUSE_OVERRIDE_sb	8	0x0	Using EFUSE to overwrite some PHY control input
spare_9	9	0x0	
B_PG2PLL_IDLEDET_TH_sb	11:10	0x0	Idle detector threshold control. 00: VDD/22 01: VDD/34 10: VDD/18 11: VDD/14
STRAP_BIF_MSTCPL_TIMEOUT_EN_sb	12	0x0	Enable 2.0 PCIe mstcpl programmable timeout
STRAP_BIF_PHY_RCVRDET_3NF_sb	13	0x1	Enable support for 3nF load cap.
STRAP_BIF_LINK_BW_NOTIFICATION_CAP_EN_sb	14	0x0	Select the default value of the Link Bandwidth Notification Capability feature.
B_P90RX_CRFR_sb	20:15	0x0	Bypass value for the clock recovery Freq Estimator output. Selected by asserting B_PRX_CRFR_BPASS.
B_P90RX_CRFR_ON_sb	22:21	0x0	Higher bit for GEN2, lower bit for GEN1 0: Clock recovery frequency loop disabled 1: Clock recovery frequency loop enabled
STRAP_BIF_ECN1P1_EN_sb	23	0x1	Enable PCIe Spec1.1 ECN support
B_P90RX_CRFRSIZE_sb	25:24	0x1	Clock recovery Freq Filter size, higher two bits for GEN2, lower two bits for GEN1.

B_P90RX_CLKG_EN_sb	26	0x1	When de-asserted, disables clock gating in power saving modes.
B_PTX_PWRS_ENB_sb	27	0x1	PCI Express transmitter power-saving enable bar 0: 50% Tx output swing for mobile applications 1: Full output swing
STRAP_BIF_GEN2_COMPLIANCE_sb	28	0x0	Enable PCIe GEN 2 config features
B_PRX_LBACK_EN_sb	29	0x0	When asserted, the Rx receives its input from txrx_lback_d_p and txrx_lback_d_n. See rxtx_lback_en in Tx.
B_P90RX_CROUT_SEL_all_valid	30	0x1	Select which registers are output to P90_BRX_CROUT[6:0]. 0: 6-bit clock recovery frequency estimator output 1: 6-bit clock recovery phase counter output
STRAP_INC_PLLCAL_PHASE_all_valid	31	0x0	This register will increase the upper phase (15:13) for the PLL lock time timer (16 bit timer)

StrapsOutputMux_7 for PCIe

StrapsOutputMux_8 - RW - 32 bits - NBMISCIND:0x68			
Field Name	**Bits**	**Default**	**Description**
B_P90TX_DEEMPH_STR_sb	7:0	0x1	De-emphasis settings for the PHY, this value is used when STRAP_DEEMPH_STR_SEL=1
B_P90TX_DRV_STR_sb	9:8	0x1	Output driver strength control. 00: 26mA nominal 01: 20mA nominal 10: 22mA nominal 11: 24mA nominal
STRAP_BIF_ALWAYS_USE_FAST_TXCLK	10	0x0	For SB, to bypass the txclk_switch and use the 500MHz PLL clk directly for TXCLK for the bif_core, regardless of the port speed
B_P90TX_CLKG_EN_sb	11	0x1	Transmitter Clock Gating Enable 0: Disable clock gating 1: Enable clock gating for power savings
spare_12	12	0x0	
B_P90RX_CRFR_BPASS_sb	13	0x0	When asserted, bypasses the clock recovery Freq Estimator output with B_PRX_CRFR[5:0].
B_PG2PLL_CREN_MODE_sb	14	0x0	Clock Recovery Enable mode. 0: Clock recovery is enabled when B_PG2RX_CR_EN=1 and disabled when B_PG2RX_CR_EN=0 and P90_BRX_ELEC_IDLE_ASYNC=1 1: Clock recovery enable is independent of B_PG2RX_CR_EN
spare_15	15	0x1	
B_P90RX_CRPHSIZE_sb	19:16	0x1	Receiver Clock Recovery Phase Filter size, higher two bits for GEN2, lower two bits for GEN1 00: N=2, effective % ratio = 8 01: N=4, effective % ratio = 16 10: N=8, effective % ratio = 32 11: N=16, effective % ratio = 64
B_PTX_DEEMPH_EN_sb	21:20	0x1	PCI Express transmitter de-emphasis enable, higher bit for GEN2, lower bit for GEN1 0: de-emphasis disabled for mobile 1: de-emphasis enabled
B_P90RX_CRFRSIZE_sb	23:22	0x1	Clock recovery Freq Filter size, higher two bits for GEN2, lower two bits for GEN1.
B_P90PLL_CLKF_sb	30:24	0x1	Feedback clock divider setting (NF). NF = B_P90PLL_CLKF[6:0] + 1 0: divide by 2 1: divide by 3 2: divide by 2 3: divide by 3 4: divide by 4
B_PG2RX_IDLEDET_EN_sb	31	0x1	0: Idle detector is disabled. P90_BRX_ELEC_IDLE_ASYNC is forced low. 1: Idle detector is enabled.

StrapsOutputMux_8 for PCIe

StrapsOutputMux_9 - RW - 32 bits - NBMISCIND:0x69			
Field Name	**Bits**	**Default**	**Description**
B_P90PLL_IBIAS_sb	9:0	0x1	Bankwdith control of PLL
B_P90RX_CRCTRL_sb	16:10	0x0	Bypass value for the clock recovery Phase Counter output. Selected by asserting B_PRX_CRCTRL_BPASS
B_P90RX_CRCTRL_BPASS_sb	17	0x0	When asserted, bypasses the clock recovery Phase Counter output with B_PRX_CRCTRL[6:0].
B_P90PLL_CLKR_sb	19:18	0x0	Reference clock divider setting (NR). NR = B_P90PLL_CLKR[1:0] + 1 Bit 1 not used. 0: divide by 1 1: divide by 2
B_P90PLL_RESET_sb	20	0x0	PLL reset (active high).
B_P90PLL_RESET_EN_sb	21	0x0	PLL reset enable. 0: PLL reset comes from internal counter (triggered by B_PPLL_PDNB). 1: PLL reset comes from B_P90PLL_RESET
B_P90PLL_TEST_sb	22	0x0	Test mode control for the PLL counters. When asserted, the reference divider and the feedback divider are cascaded and the output is observed through P90_BPLL_TESTOUT. The REFCLK to P90_BPLL_TESTOUT divide ratio is given by NR NF. When either NR or NF is one, P90_BPLL_TESTOUT will not toggle.
STRAP_BIF_PAD_TX_MANUAL_IMPEDANCE_all_valid	26:23	0x0	Controls default impedance of TX IO pads
STRAP_BIF_PAD_RX_MANUAL_IMPEDANCE_all_valid	30:27	0x0	Controls default impedance of RX IO pads
STRAP_BIF_VC_EN	31	0x1	Virtual Channel CFG register Enable

StrapsOutputMux_9 for PCIe

StrapsOutputMux_A - RW - 32 bits - NBMISCIND:0x6A			
Field Name	**Bits**	**Default**	**Description**
STRAP_BIF_AUTO_RC_SPEED_NEGOTIATION_DIS_A_sb	0	0x1	When set, disables the ability for the RC to automatically start link negotiation
REG_Expxbar_srr_mode_GPP1_GPP2	1	0x0	GPP1/GPP2 Expxbar simple arbitration mode for downstream cycles.
STRAP_BIF_ACS_EN_all_valid	2	0x1	Enable PCIe Extended Capabillity for ACS (enable linked-list pointer
CHIP_BIF_reqid_en_all_valid	3	0x0	
spare_9_4	9:4	0x0	
STRAP_BIF_LC_CDR_SET_TYPE_sb	11:10	0x1	Determines the default value for the LC_CDR_SET_TYPE register which selects the type of ordered set that is sent out in CDR test mode.
STRAP_BIF_LC_CDR_TEST_OFF_sb	23:12	0x1	Determines the default value for the LC_CDR_TEST_OFF register which selects the detect timeout value when in CDR test mode.
spare_24	24	0x0	
STRAP_BIF_FORCE_CDR_MODE_sb	25	0x0	Enable CDR test mode.
spare_31_26	31:26	0x0	

StrapsOutputMux_A for PCIe

StrapsOutputMux_B - RW - 32 bits - NBMISCIND:0x6B			
Field Name	**Bits**	**Default**	**Description**
STRAP_BIF_LC_CDR_TEST_SETS_sb	11:0	0x1	Determines the default value for the LC_CDR_TEST_SETS register which selects the type of ordered set that is sent out in CDR test mode.
spare_14_12	14:12	0x0	

STRAP_BIF_I2C_SLV_ADR_sb	18:15	0x1	I2C Slave Address used to talk to the I2C Master when back door register access is performed
STRAP_BIF_DBG_I2C_EN_all_valid	19	0x0	I2C slave Enable; to enable the back door bif register access
spare_23_20	23:20	0x0	
STRAP_BIF_TEST_TOGGLE_MODE_sb	24	0x0	Debug mode to send 1010 pattern through the transmitter. On the receive side, the pattern is checked to make sure that the 1010 pattern is received correctly.
spare_26_25	26:25	0x0	
B_P90RX_INCAL_FORCE_GPP3b	27	0x0	When B_PRX_INCAL_FORCE is asserted, the analog offset calibration is disabled.
B_P90RX_INCAL_FORCE_sb	28	0x0	When B_PRX_INCAL_FORCE is asserted, the analog offset calibration is disabled.
B_P90RX_INCAL_FORCE_GPP1	29	0x0	When B_PRX_INCAL_FORCE is asserted, the analog offset calibration is disabled.
B_P90RX_INCAL_FORCE_GPP2	30	0x0	When B_PRX_INCAL_FORCE is asserted, the analog offset calibration is disabled.
B_P90RX_INCAL_FORCE_GPP3a	31	0x0	When B_PRX_INCAL_FORCE is asserted, the analog offset calibration is disabled.

StrapsOutputMux_B for PCIe

StrapsOutputMux_C - RW - 32 bits - NBMISCIND:0x6C			
Field Name	**Bits**	**Default**	**Description**
STRAP_BIF_FORCE_COMPLIANCE_sb	0	0x0	Required for Tester: 0: Normal Operation 1: Force LC into compliance mode (used for testing TX without waiting for RX to be trained on the tester)
STRAP_BIF_FORCE_COMPLIANCE_GPP1	1	0x0	Required for Tester: 0: Normal Operation 1: Force LC into compliance mode (used for testing TX without waiting for RX to be trained on the tester)
STRAP_BIF_FORCE_COMPLIANCE_GPP2	2	0x0	Required for Tester: 0: Normal Operation 1: Force LC into compliance mode (used for testing TX without waiting for RX to be trained on the tester)
STRAP_BIF_FORCE_COMPLIANCE_GPP3a	3	0x0	Required for Tester: 0: Normal Operation 1: Force LC into compliance mode (used for testing TX without waiting for RX to be trained on the tester)
STRAP_BIF_BACKGROUND_IMP_CAL_sb	4	0x0	Enables calibration of the PHY to run in the background
B_P90PLL_BACKUP_1_0_sb	6:5	0x0	B_P90PLL_BACKUP[0] (distributed to Rx as pllrxg2_bypass_sel): 0: select rxcr_data_clk for rxtxg2_bypass_data from Rx to high speed Tx bypass path. 1: select rxcr90_elec_idle_async for rxtxg2_bypass_data from Rx to high speed Tx bypass path. B_P90PLL_BACKUP[1] (distributed to Tx as plltxg2_bypass_sel): 0: select B_P90TX_TEST_DATA[0] for high speed Tx bypass path. 1: select for rxtxg2_bypass_data for high Tx bypass path.
STRAP_BIF_IMP_MANUAL_OVERRIDE_all_valid	7	0x0	Overrides the internal impedance calibration with values from straps.
STRAP_BIF_FORCE_COMPLIANCE_A_GPP3b	8	0x0	Required for Tester: 0: Normal Operation 1: Force LC into compliance mode (used for testing TX without waiting for RX to be trained on the tester)
P_BREFCLK_GPP1	9	0x0	The select register of reference clock source 0: reference clock is from SB reference clock 1: reference clock is from its own reference clock
B_P90_PLL_BACKUP_3_2_sb	11:10	0x0	

STRAP_BIF_ERR_REPORTING_DIS_sb	12	0x1	Disable error reporting.
spare_13	13	0x1	
CHIP_BIF_mode_sb	14	0x0	Identifies to the hardware whether it is the upstream or downstream component. 0: BIF is the downstream component 1: BIF is the updstream component
PHY_DEBUG_EN_sb	15	0x0	PHY debug mode enable
B_PG2RX_EQ_sb	19:16	0x0	higher two bits for GEN2, lower two bits for GEN1, Rx Equalization setting, 00 is minimum equalization; 11 is maximum equalization
spare_23_20	23:20	0x1	
spare_29_24	29:24	0x1	
B_PG2TX_TAPINV_sb	30	0x1	When asserted, inverts the third de-emphasis filter tap
P_BREFCLK_GPP2	31	0x0	The select register of reference clock source 0: reference clock is from SB reference clock 1: reference clock is from its own reference clock

StrapsOutputMux_C for PCIe

StrapsOutputMux_D - RW - 32 bits - NBMISCIND:0x6D			
Field Name	**Bits**	**Default**	**Description**
	31:0	0x0	

StrapsOutputMux_E - RW - 32 bits - NBMISCIND:0x6E			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_E	31:0	0x0	

StrapsOutputMux_F - RW - 32 bits - NBMISCIND:0x6F			
Field Name	**Bits**	**Default**	**Description**
STRAP_DEEMPH_STR_SEL_sb	0	0x0	Using B_P90TX_DEEMPH_STR to control De-emphasis settings for the PHY, this function has a higher priority than STRAP_BIF_TX_DEEMPH_STR
STRAP_BIF_DE_EMPHASIS_SEL_A_sb	1	0x1	This controls the default value of the Selectable De-emphasis field (bit 6) of the Link Control 2 configuration register. 1 = RC advertises -3.5dB de-emphasis 0 = the RC advertises -6dB de-emphasis.
STRAP_BIF_DEEMPH_BIF_SEL_A_sb	2	0x1	Allow the bif_core to select the LTSSM Deemphasis value that goes to the PHY (based on PCIe 2.0, rev0.9 specification). When set to '0', the value comes from the STRAP_BIF_TX_DEEMPH_STR straps.
spare_3	3	0x0	
STRAP_BIF_LC_SELECT_DEEMPHASIS_sb	4	0x0	Default value of the LC_SELECT_DEEMPHASIS private register.
spare_6_5	6:5	0x0	
STRAP_BIF_LC_DONT_DEASSERT_RX_EN_IN_TEST_sb	7	0x0	Control LC_PI_RcvrEn in s_Poll_Compliance_Idle and s_Rcvd_Loopback_Speed. 0: De-assert RcvrEn in s_Poll_Compliance_Idle and s_Rcvd_Loopback_Speed after the EIOS have been transmitted. 1: Don't de-assert RcvrEn in s_Poll_Compliance_Idle or s_Rcvd_Loopback_Speed.
spare_8	8	0x1	
STRAP_BIF_TX_DEEMPH_STR_sb	16:9	0x1	De-emphasis and Transmit Margin settings for the PHY
STRAP_BIF_LC_TARGET_LINK_SPEED_OVERRIDE_EN_A_sb	17	0x0	Default value for the LC_TARGET_LINK_SPEED_OVERRIDE_EN private register bit. Set this strap to '1' in order to force the advertised Target Link Speed to 2.5GT/s during boot up.

spare_31_18	31:18	0x0	

StrapsOutputMux_F for PCIe

StrapsOutputMux_0 - RW - 32 bits - NBMISCIND:0x70			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_0	31:0	0x0	Bit [10]=STRAP_FULL_EDRDY or BondingOptionBit7 from efuse

StrapsOutputMux_1 - RW - 32 bits - NBMISCIND:0x71			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_1	31:0	0x0	

StrapsOutputMux_2 - RW - 32 bits - NBMISCIND:0x72			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_2	31:0	0x0	

StrapsOutputMux_3 - RW - 32 bits - NBMISCIND:0x73			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_3	31:0	0x0	

PCIE_CORE_ARB_2 - RW - 32 bits - NBMISCIND:0x74			
Field Name	**Bits**	**Default**	**Description**
PCIE_GPPSB_ARB	29:0	0x24924924	Control for GPPSB Weighted Round Robin arbiter in the IOC. Arbitrates between traffic from PCIe cores GPP3a, GPP3b, and SB. Every two bits assign the core with the highest priority during that arbitration round; during the next arbitration round, the next two bits are used. Two bit encodings: 00 - SB PCIe core 01 - GPP3a PCIe core 10 - GPP3b PCIe core
Reserved	31:30	0x0	Reserved for future use. This register controls no hardware.

IOC_FEATURE_CNTL - RW - 32 bits - NBMISCIND:0x75			
Field Name	**Bits**	**Default**	**Description**

IOC_FEATURE_CNTL_10_0	10:0	0x0	[0] - Enable access to Device 0 Function 2 [1] - NMI_EN. Enable DFT_GPIO0 to be used as NMI# input pin. [2] - Direct INTx, HotPlug and PM_PME messages to HT. This register should be set for secondary SR5690/5670/5650s in order to route INTx, HotPlug and PM_PME messages to the southbridge. This register should still be set even if the SR5690/5670/5650 IOAPIC is enabled. [3] - Enable decoding of downstream HT INTx, HotPlug (VDM) and PM_PME (VDM) messages to the southbridge using PCIe message formats. This register should be set on the primary SR5690/5670/5650. [8:4] - HT vendor defined message offset. [10:9] - P2P decoding mode - 00 = Abort non-memory reads. Directly route local P2P writes. Send memory writes to the CPU. Abort all other writes. - 01 = Abort non-memory reads. Directly route local P2P writes. Send all other writes up to the CPU as P2P to remote root complexes. - 10 = Abort non-memory reads. Send all writes up to the CPU. CPU may reflect these back down as P2P requests. - 11 = Reserved
IOC_FEATURE_CNTL_12_11	12:11	0x3	[11] - JTAG host access enable. This register is automatically cleared by the execution of the SKINIT CPU instruction [12] - MCU host access enable. This register is automatically cleared by the execution of the SKINIT CPU instruction
IOC_FEATURE_CNTL_27_13	27:13	0x0	[27:25] - Number of credits on AER interface between IOC and IOMMU_L1_GPP3b. If '0' then AER is disabled. [24:22] - Number of credits on AER interface between ioc and IOMMU_L1_GPP3a. If '0' then AER is disabled. [21:19] - Number of credits on AER interface between ioc and IOMMU_L1_sb. If '0' then AER is disabled. [18:16] - Number of credits on AER interface between ioc and IOMMU_L1_GPP2. If '0' then AER is disabled. [15:13] - Number of credits on AER interface between ioc and IOMMU_L1_GPP. If '0' then AER is disabled.
IOC_FEATURE_CNTL_28	28	0x0	[28] - #NMI Status bit for software read-back. Write 1 to clear.
IOC_FEATURE_CNTL_31_29	31:29	0x0	[29] - If set then request id for HP/PM_PME messages to SB carries device ID of the port that initiated the message, otherwise the request id is 0. [30] - MSI 64-bit Enable [31] - Reserved

MMIO_BASE_LIMIT_UPPER - RW - 32 bits - NBMISCIND:0x76			
Field Name	**Bits**	**Default**	**Description**
MMIO_BASE_UPPER	11:0	0x0	Defines MMIOBASE [51:40]
MMIO_LIMIT_UPPER	27:16	0x0	Defines MMIOLIMIT [51:40]

SERR_PIN_CONTROL - RW - 32 bits - NBMISCIND:0x77			
Field Name	**Bits**	**Default**	**Description**
SERR_NBCFG_EN	0	0x0	Asserts SERR_FATAL# when SERR is asserted in device 0 by HyperTransport or internal parity error
HT_SYNCFLOOD_DETECT_EN	1	0x0	
SERR_DEV2_EN	2	0x0	Asserts SERR_FATAL# when SERR is asserted in bridge 2 (before device remapping)
SERR_DEV3_EN	3	0x0	Asserts SERR_FATAL# when SERR is asserted in bridge 3 (before device remapping)
SERR_DEV4_EN	4	0x0	Asserts SERR_FATAL# when SERR is asserted in bridge 4 (before device remapping)
SERR_DEV5_EN	5	0x0	Asserts SERR_FATAL# when SERR is asserted in bridge 5 (before device remapping)
SERR_DEV6_EN	6	0x0	Asserts SERR_FATAL# when SERR is asserted in bridge 6 (before device remapping)
SERR_DEV7_EN	7	0x0	Asserts SERR_FATAL# when SERR is asserted in bridge 7 (before device remapping)
SERR_DEV8_EN	8	0x0	Asserts SERR_FATAL# when SERR is asserted in bridge 8 (before device remapping)
SERR_DEV9_EN	9	0x0	Asserts SERR_FATAL# when SERR is asserted in bridge 9 (before device remapping)
SERR_DEV10_EN	10	0x0	Asserts SERR_FATAL# when SERR is asserted in bridge 10 (before device remapping)
SERR_DEV11_EN	11	0x0	Asserts SERR_FATAL# when SERR is asserted in bridge 11 (before device remapping)
SERR_DEV12_EN	12	0x0	Asserts SERR_FATAL# when SERR is asserted in bridge 12 (before device remapping)
SERR_DEV13_EN	13	0x0	Asserts SERR_FATAL# when SERR is asserted in bridge 13 (before device remapping)
SERR_EN	31	0x0	Enables SERR conditions to trigger the SERR_FATAL# pin
SERR_FATAL# Pin Control			

FATAL_PIN_CONTROL - RW - 32 bits - NBMISCIND:0x78			
Field Name	**Bits**	**Default**	**Description**
FATAL_PAR_EN	0	0x0	Asserts SERR_FATAL# when a fatal error is asserted in device 0 by internal parity error
FATAL_HT_EN	1	0x0	Asserts SERR_FATAL# when a fatal error is asserted in device 0 by HyperTransport
FATAL_DEV2_EN	2	0x0	Asserts SERR_FATAL# when a fatal error is asserted in bridge 2 (before device remapping)
FATAL_DEV3_EN	3	0x0	Asserts SERR_FATAL# when a fatal error is asserted in bridge 3 (before device remapping)
FATAL_DEV4_EN	4	0x0	Asserts SERR_FATAL# when a fatal error is asserted in bridge 4 (before device remapping)
FATAL_DEV5_EN	5	0x0	Asserts SERR_FATAL# when a fatal error is asserted in bridge 5 (before device remapping)
FATAL_DEV6_EN	6	0x0	Asserts SERR_FATAL# when a fatal error is asserted in bridge 6 (before device remapping)
FATAL_DEV7_EN	7	0x0	Asserts SERR_FATAL# when a fatal error is asserted in bridge 7 (before device remapping)
FATAL_DEV8_EN	8	0x0	Asserts SERR_FATAL# when a fatal error is asserted in bridge 8 (before device remapping)
FATAL_DEV9_EN	9	0x0	Asserts SERR_FATAL# when a fatal error is asserted in bridge 9 (before device remapping)
FATAL_DEV10_EN	10	0x0	Assert sSERR_FATAL# when a fatal error is asserted in bridge 10 (before device remapping)
FATAL_DEV11_EN	11	0x0	Asserts SERR_FATAL# when a fatal error is asserted in bridge 11 (before device remapping)

FATAL_DEV12_EN	12	0x0	Asserts SERR_FATAL# when a fatal error is asserted in bridge 12 (before device remapping)
FATAL_DEV13_EN	13	0x0	Asserts SERR_FATAL# when a fatal error is asserted in bridge 13 (before device remapping)
FATAL_EN	31	0x0	Enables fatal error conditions to trigger the SERR_FATAL# pin
SERR_FATAL# Pin Control			

NON_FATAL_PIN_CONTROL - RW - 32 bits - NBMISCIND:0x79			
Field Name	**Bits**	**Default**	**Description**
NON_FATAL_PAR_EN	0	0x0	Asserts NON_FATAL_CORR# when a non-fatal error is asserted in device 0 by internal parity error
NON_FATAL_HT_EN	1	0x0	Asserts NON_FATAL_CORR# when a non-fatal error is asserted in device 0 by HyperTransport
NON_FATAL_DEV2_EN	2	0x0	Asserts NON_FATAL_CORR# when a non-fatal error is asserted in bridge 2 (before device remapping)
NON_FATAL_DEV3_EN	3	0x0	Asserts NON_FATAL_CORR# when a non-fatal error is asserted in bridge 3 (before device remapping)
NON_FATAL_DEV4_EN	4	0x0	Asserts NON_FATAL_CORR# when a non-fatal error is asserted in bridge 4 (before device remapping)
NON_FATAL_DEV5_EN	5	0x0	Asserts NON_FATAL_CORR# when a non-fatal error is asserted in bridge 5 (before device remapping)
NON_FATAL_DEV6_EN	6	0x0	Asserts NON_FATAL_CORR# when a non-fatal error is asserted in bridge 6 (before device remapping)
NON_FATAL_DEV7_EN	7	0x0	Asserts NON_FATAL_CORR# when a non-fatal error is asserted in bridge 7 (before device remapping)
NON_FATAL_DEV8_EN	8	0x0	Asserts NON_FATAL_CORR# when a non-fatal error is asserted in bridge 8 (before device remapping)
NON_FATAL_DEV9_EN	9	0x0	Asserts NON_FATAL_CORR# when a non-fatal error is asserted in bridge 9 (before device remapping)
NON_FATAL_DEV10_EN	10	0x0	Asserts NON_FATAL_CORR# when a non-fatal error is asserted in bridge 10 (before device remapping)
NON_FATAL_DEV11_EN	11	0x0	Asserts NON_FATAL_CORR# when a non-fatal error is asserted in bridge 11 (before device remapping)
NON_FATAL_DEV12_EN	12	0x0	Asserts NON_FATAL_CORR# when a non-fatal error is asserted in bridge 12 (before device remapping)
NON_FATAL_DEV13_EN	13	0x0	Asserts NON_FATAL_CORR# when a non-fatal error is asserted in bridge 13 (before device remapping)
NON_FATAL_EN	31	0x0	Enables non-fatal error conditions to trigger the NON_FATAL_CORR# pin
NON_FATAL_CORR# Pin Control			

CORR_PIN_CONTROL - RW - 32 bits - NBMISCIND:0x7A			
Field Name	**Bits**	**Default**	**Description**
CORR_PAR_EN	0	0x0	Asserts NON_FATAL_CORR# when a correctable error is asserted in device 0 by internal parity error
CORR_DEV2_EN	2	0x0	Asserts NON_FATAL_CORR# when a correctable error is asserted in bridge 2 (before device remapping)
CORR_DEV3_EN	3	0x0	Asserts NON_FATAL_CORR# when a correctable error is asserted in bridge 3 (before device remapping)
CORR_DEV4_EN	4	0x0	Asserts NON_FATAL_CORR# when a correctable error is asserted in bridge 4 (before device remapping)
CORR_DEV5_EN	5	0x0	Asserts NON_FATAL_CORR# when a correctable error is asserted in bridge 5 (before device remapping)
CORR_DEV6_EN	6	0x0	Asserts NON_FATAL_CORR# when a correctable error is asserted in bridge 6 (before device remapping)
CORR_DEV7_EN	7	0x0	Asserts NON_FATAL_CORR# when a correctable error is asserted in bridge 7 (before device remapping)

CORR_DEV8_EN	8	0x0	Asserts NON_FATAL_CORR# when a correctable error is asserted in bridge 8 (before device remapping)
CORR_DEV9_EN	9	0x0	Asserts NON_FATAL_CORR# when a correctable error is asserted in bridge 9 (before device remapping)
CORR_DEV10_EN	10	0x0	Asserts NON_FATAL_CORR# when a correctable error is asserted in bridge 10 (before device remapping)
CORR_DEV11_EN	11	0x0	Asserts NON_FATAL_CORR# when a correctable error is asserted in bridge 11 (before device remapping)
CORR_DEV12_EN	12	0x0	Asserts NON_FATAL_CORR# when a correctable error is asserted in bridge 12 (before device remapping)
CORR_DEV13_EN	13	0x0	Asserts NON_FATAL_CORR# when a correctable error is asserted in bridge 13 (before device remapping)
CORR_EN	31	0x0	Enables correctable error conditions to trigger the NON_FATAL_CORR# pin
NON_FATAL_CORR# Pin Control			

DFT_CNTL3 - RW - 32 bits - NBMISCIND:0x7B			
Field Name	**Bits**	**Default**	**Description**
TEST_DEBUG_MULTIBLOCKEN	0	0x0	Enables the dual debug bus feature
TEST_DEBUG_BUS_BLK1	1	0x0	Selects the high or low mux for blk1 0=Low mux 1=High mux
TEST_DEBUG_BUS_BLK2	2	0x0	Select the high or low mux for blk2 0=Low mux 1=High mux
TEST_DEBUG_MUX_BLK2	8:3	0x0	Debug bus mux select for blk 2
GPIO_DEBUG_BUS_MUX_SEL4	18:15	0x0	Selects which bit of the internal 16-bit debug bus to route to DBG_GPIO0
GPIO_DEBUG_BUS_MUX_SEL5	22:19	0x0	Selects which bit of the internal 16-bit debug bus to route to DBG_GPIO1
GPIO_DEBUG_BUS_MUX_SEL6	26:23	0x0	Selects which bit of the internal 16-bit debug bus to route to DBG_GPIO2
GPIO_DEBUG_BUS_MUX_SEL7	30:27	0x0	Selects which bit of the internal 16-bit debug bus to route to DBG_GPIO3
spare	31	0x0	Reserved for future use. This register controls no hardware

DFT_SPARE - RW - 32 bits - NBMISCIND:0x7F			
Field Name	**Bits**	**Default**	**Description**
DFT_SPARE	31:0	0x0	Reserved for future use. This register controls no hardware

2.5.6 L1CFGIND Registers

L1_DEBUG_0 - RW - 32 bits - L1CFGIND:0x6			
Field Name	**Bits**	**Default**	**Description**
L1DEBUG0	31:0	0x0	Bit[0] - When written to 1, causes interrupt smaller than a DW status bit to reset. Bits[31:1] - Reserved for ECOs

ECO controls bit 0

L1_DEBUG_1 - RW - 32 bits - L1CFGIND:0x7			
Field Name	**Bits**	**Default**	**Description**
L1DEBUG1	31:0	0x0	Bit[0] - When set to 0, causes function number to be ignored for phantom functions. Bit[1] - Reserved. Bit[2] - When set, command wait does not wait for workqueue to empty before completing. Bit[3] - When set, command wait does not wait for reads to complete before completing. Bit[4] - When set, invalidation does not wait for workqueue to empty before completing invalidation. Bit[5] - When set, invalidation does not wait for reads to complete before completing invalidation. Bit[6] - Disables ECO for invalidation filter to take effect only for page or dev inval. Bit[7] - Disables ECO for ignoring r/w perm on DT non-ats completion. Bit[8] - Disables ECO for using write scoreboard as a workqueue scoreboard. Bit[9] - Bit[2] - Disables ECO for removing mask on L2 to L1 completion when iommu is not enabled. Bit[10] - Disables ECO for L1 workqueue bug fix. Bit[11] - Enables filtering using outstanding special requests. Bits[31:12] - Reserved.

ECO controls bit 1

L1_DEBUG_STATUS - RW - 32 bits - L1CFGIND:0x8			
Field Name	**Bits**	**Default**	**Description**
L1DEBUG_STATUS	31:0	0x0	Bit[0] - Detected Interrupt smaller than 1 DW - clear using L1_DEBUG_0 bit[0]. Bit[31:1] - Reserved.

HW status bits reserved for ECOs

L1_CNTRL_0 - RW - 32 bits - L1CFGIND:0xC			
Field Name	**Bits**	**Default**	**Description**
Unfilter_dis	0	0x0	Disable unfiltering in L1 wq of aborted L2 requests
Fragment_dis	1	0x0	Disable variable page size support in L1 cache - only 4K pages
CacheIR_only	2	0x1	Cache read only pages in L1
CacheIW_only	3	0x1	Cache write only pages in L1
Reserved0 (R)	4	0x0	

Replacement_Sel	5	0x0	N/A
L2Credits	13:8	0x4	Controls credits for L1 to L2 interface
Reserved1 (R)	19:14	0x0	
L1Banks (R)	21:20	0x1	Set by hardware - number of caches in L1
L1Entries (R)	27:24	0x0	Set by hardware - number of entries in each L1 cache, 2^ L1 entries
L1VirtOrderQueues (R)	30:28	0x0	Controls number of virtual queues in L1 workqueue 0x0 - 1 vq 0x1 - 2 vq 0x2 - 4 vq 0x3 - 8 vq 0x4 - 16 vq

L1_CNTRL_1 - RW - 32 bits - L1CFGIND:0xD			
Field Name	**Bits**	**Default**	**Description**
VOQPortBits	2:0	0x0	When not 0x0, enables virtual queue hashing using port id, controls number of bits to use from port id for hashing
VOQFuncBits	6:4	0x0	N/A
VOQXorMode	8	0x0	N/A
CacheByPass	9	0x0	Enables L1 cache bypass
L1CacheParityEn	10	0x0	Enables forced miss of L1 cache due to failed parity check
L1ParityEn	11	0x0	
L1DTEDis	12	0x0	Disables L1 caching of DTE
BlockL1Dis (R)	13	0x0	N/A
WQ_EntryDis	18:14	0x0	Value indicates how many cache entries in L1 to disable
ATS_nobuffer_insert	19	0x0	Disables buffering of read completion data when inserting ats responses
Snd_filter_dis	20	0x0	Disables filtering of requests to L2
L1Order_en	21	0x0	Enables strict ordering of all requests through L1
L1CacheInvAllEn	22	0x0	Enables invalidation of entire cache when invalidation command is sent
Select_timeout_pulse	25:23	0x0	
L1_cache_sel_reqid	26	0x0	When set, will allow the reqid to be used in hashing between multiple L1 caches
L1_cache_sel_interleave	27	0x0	When set, causes cache updates to toggle between multiple caches
Pretrans_noVA_filterEn	28	0x0	When set, VA is not used for filtering pretrans requests
UnTrans_2M_filterEn	29	0x0	Enables filtering of requests on a 2M boundry instead of 4K
L1_debug_cntr_mode	30	0x0	Mode control for debug bus

L1_CNTRL_2 - RW - 32 bits - L1CFGIND:0xE			
Field Name	**Bits**	**Default**	**Description**
Reserved0 (R)	3:0	0x0	
INT_type_resvd	27:4	0xFF0C	Field to be inserted into interrupt when wrong mode is detected

L1_CNTRL_3 - RW - 32 bits - L1CFGIND:0xF			
Field Name	**Bits**	**Default**	**Description**
ATS_tlbinv_pulse_width	31:0	0x51615	Sets the pulse width of the ats invalidation counters

L1_BANK_SEL_0 - RW - 32 bits - L1CFGIND:0x10			
Field Name	**Bits**	**Default**	**Description**
L1CacheBankSel_0	15:0	0x0	Value is used to determine the virtual address bit that selects between the 2 banks of the L1 cache (if present). The bank is selected by bitwise ANDing this register against virtual address bits 19:12 and XORing the result

L1_BANK_DISABLE_0 - RW - 32 bits - L1CFGIND:0x11			
Field Name	**Bits**	**Default**	**Description**
L1CacheLineDis_0	5:0	0x0	Sets the number of cache entries to disable in cache 0
L1CacheLineDis_1	13:8	0x0	Sets the number of cache entries to disable in cache 1

L1_WQ_STATUS_0 - RW - 32 bits - L1CFGIND:0x20			
Field Name	**Bits**	**Default**	**Description**
EntryStatus0 (R)	2:0	0x0	For all fields:
EntryStatus1 (R)	5:3	0x0	
EntryStatus2 (R)	8:6	0x0	0x0 -> idle
EntryStatus3 (R)	11:9	0x0	0x1 -> wait_l1
EntryStatus4 (R)	14:12	0x0	0x2 -> wait_l2
EntryStatus5 (R)	17:15	0x0	0x3 -> sending special request to L2
EntryStatus6 (R)	20:18	0x0	0x4 -> waiting for completion of special request from L2
EntryStatus7 (R)	23:21	0x0	0x5 -> done
EntryStatus8 (R)	26:24	0x0	
EntryStatus9 (R)	29:27	0x0	

L1_WQ_STATUS_1 - RW - 32 bits - L1CFGIND:0x21			
Field Name	**Bits**	**Default**	**Description**
EntryStatus10 (R)	2:0	0x0	For all fields:
EntryStatus11 (R)	5:3	0x0	
EntryStatus12 (R)	8:6	0x0	0x0 -> idle
EntryStatus13 (R)	11:9	0x0	0x1 -> wait_l1
EntryStatus14 (R)	14:12	0x0	0x2 -> wait_l2
EntryStatus15 (R)	17:15	0x0	0x3 -> sending special request to L2
EntryStatus16 (R)	20:18	0x0	0x4 -> waiting for completion of special request from L2
EntryStatus17 (R)	23:21	0x0	0x5 -> done
EntryStatus18 (R)	26:24	0x0	
EntryStatus19 (R)	29:27	0x0	

L1_WQ_STATUS_2 - RW - 32 bits - L1CFGIND:0x22			
Field Name	**Bits**	**Default**	**Description**
EntryStatus20 (R)	2:0	0x0	For all fields: 0x0 -> idle 0x1 -> wait_l1 0x2 -> wait_l2 0x3 -> sending special request to L2 0x4 -> waiting for completion of special request from L2 0x5 -> done
EntryStatus21 (R)	5:3	0x0	
EntryStatus22 (R)	8:6	0x0	
EntryStatus23 (R)	11:9	0x0	
EntryStatus24 (R)	14:12	0x0	
EntryStatus25 (R)	17:15	0x0	
EntryStatus26 (R)	20:18	0x0	
EntryStatus27 (R)	23:21	0x0	
EntryStatus28 (R)	26:24	0x0	
EntryStatus29 (R)	29:27	0x0	

L1_WQ_STATUS_3 - RW - 32 bits - L1CFGIND:0x23			
Field Name	**Bits**	**Default**	**Description**
EntryStatus30 (R)	2:0	0x0	For status 30 and status 31: 0x0 -> idle 0x1 -> wait_l1 0x2 -> wait_l2 0x3 -> sending special request to L2 0x4 -> waiting for completion of special request from L2 0x5 -> done
EntryStatus31 (R)	5:3	0x0	
Invalidation_status (R)	15:8	0x0	Status of invalidation state machine

2.5.7 L2CFGIND Registers

L2_DEBUG_0 - RW - 32 bits - L2CFGIND:0x6			
Field Name	**Bits**	**Default**	**Description**
L2DEBUG0	31:0	0x0	Bits[4:0] - Reserved Bit[5] - Enable fix to avoid corruption of DTE.EX attribute when IOMMU has cached device table entries. Bit[6] - Enable fix to avoid corruption of DTE.SE attribute when IOMMU has cached device table entries. Bit[7] - Enable fix to handle DTE page mode attributes combined with IoCtl and SysMgt. Bit[8] - Enable fix to abort address translation requests to the exclusion range when the corresponding device table entries have both EX and TV bits cleared. Bits[31:9] - Reserved

Reserved for ECOs

L2_DEBUG_1 - RW - 32 bits - L2CFGIND:0x7			
Field Name	**Bits**	**Default**	**Description**
L2DEBUG1	31:0	0x0	Bit[0] - Reserved
			Bit[1] - Enable fix to avoid aborting untranslated memory requests or address translation requests, when any of these - exclusion range address, system management range address, or IO space range address - are configured to block or pass trough requests and are located above the largest virtual address defined in the device table page mode field.
			Bit[2] - Enable fix to abort address translation requests in the system management address range when device table entry has SysMgt=0x0, 0x1 or 0x2 and IntTaLen[3:2]=0x3 or when device table entry has SysMgt=0x3, IntTaLen[3:2]= 0x3, V=0x1 and TV=0x0.
			Bit[3] - Enable fix to avoid treating interrupt requests as untranslated memory requests or address translation requests from exclusion range under specific conditions.
			Bit[4] - Enable fix to abort DMA read requests in the HT interrupt address range when the corresponding device table entry has the IV bit cleared
			Bit[5] - Enable fix to avoid access right checks for pretranslated requests.
			Bit[6] - Enable fix to avoid corruption of the DTE.IG bit for Startup and EOI interrupts.
			Bit[7] - Enable fix to detect address translation request in the interrupt address range under all conditions.
			Bit[31:8] - Reserved

Reserved for ECOs

L2_STATUS_0 - RW - 32 bits - L2CFGIND:0x8			
Field Name	**Bits**	**Default**	**Description**
L2STATUS0 (R)	31:0	0x0	Internal IOMMU L2A status

L2_CONTROL_0 - RW - 32 bits - L2CFGIND:0xC			
Field Name	**Bits**	**Default**	**Description**
PTCAddrTransReqCheck	0	0x0	0=Address translation requests do not check the PTC 1=Address translation requests check the PTC
AllowL1CacheVZero	1	0x0	0=L2 does not allow L1 to cache DTEs where V=0 1=L2 allows L1 to cache DTEs where V=1. L1 stores IR and IW as if they are both set to 1
AllowL1CacheATSRsp	2	0x0	0=L2 does not allow L1 to cache responses to ATS address translation requests 1=L2 allows L1 to cache responses to ATS address translation requests
DTCHitVZeroOrIVZero	3	0x0	0=A DTE is refetched if a DTE with V=0 for a memory request or IV=1 for an interrupt request is hit in the DTC 1=A DTE is not refetched if a DTE with V=0 for a memory request or IV=1 for an interrupt request is hit in the DTC. This DTE is used
IFifoTWCredits	9:4	0x4	Controls the initial number of credits for the ififo to TW interface. Credits are loaded whenever the register changes value. This register may only be programmed when IOMMU is not enabled to preserve correct operation.
SIDEPTEOnUntransExcl	10	0x0	0=Caches return DTE to L1 on an untranslated exclusion range access 1=Caches return PTE to L1 on an untranslated exclusion range access
SIDEPTEOnAddrTransExcl	11	0x0	0=Caches return DTE to L1 on an address translation exclusion range access 1=Caches return PTE to L1 on an address translation exclusion range access
IFifoCMBCredits	17:12	0x4	Controls the initial number of credits for the ififo to fault/CMB interface. Credits are loaded whenever the register value changes. This register may only be programmed when IOMMU is not enabled to preserve correct operation.
FLTCMBPriority	18	0x0	0=Round-robin arbitration between cache responses and table-walker responses at the fault combiner. 1=Table-walker responses always win arbitration at the fault combiner.
IFifoBurstLength	23:20	0x1	Sets the burst length when arbitrating between clients coming into the L2
IFifoClientPriority	31:24	0x0	Each bit of this register controls whether the corresponding L1 client is arbitrated as high priority or not. Not all implementations will use all of the priority bits due to a lower number of clients versus the register width

L2_CONTROL_0 - RW - 32 bits - L2CFGIND:0xC			
Field Name	**Bits**	**Default**	**Description**
AddrTransReqCheckPTC	0	0x0	0=Address translation requests do not check the PTC 1=Address translation requests check the PTC
IFifoTWCredits	9:4	0x4	Controls the initial number of credits for the ififo to TW interface. Credits are loaded whenever the register changes value. This register may only be programmed when IOMMU is not enabled to preserve correct operation.
IFifoCMBCredits	17:12	0x4	Controls the initial number of credits for the ififo to fault/CMB interface. Credits are loaded whenever the register value changes. This register may only be programmed when IOMMU is not enabled to preserve correct operation.

L2_CONTROL_1 - RW - 32 bits - L2CFGIND:0xD			
Field Name	**Bits**	**Default**	**Description**
SeqInvBurstLimitInv	7:0	0x8	Sets the number of consecutive invalidation requests to perform when doing sequential invalidation. Regular L2 and invalidation requests will alternate access to the main L2 caches based upon SeqInvBurstLimitInv and SeqInvBurstLimitL2Req.
SeqInvBurstLimitL2Req	15:8	0x8	Sets the number of consecutive iommu L2 requests to perform when doing sequential invalidation. Regular L2 and invalidation requests will alternate access to the main L2 caches based upon SeqInvBurstLimitInv and SeqInvBurstLimitL2Req.
SeqInvBurstLimitEn	16	0x1	Enable stalling L2 requests to allow invalidation cycles to make forward progress based upon SeqInvBurstLimitInv and SeqInvBurstLimitL2Req
PerfThreshold	31:24	0x0	Fifo threshold level used to calculate certain performance counter values.

L2_DTC_CONTROL - RW - 32 bits - L2CFGIND:0x10			
Field Name	**Bits**	**Default**	**Description**
DTCReplacementSel	1:0	0x1	Selects the DTC replacement algorithm. Implementation may not support all replacement algorithms
	3		0=Reads update replacement state bits when there is a simultaneous read and write to the same DTC index 1=Writes update replacement state bits when there is a simultaneous read and write to the same DTC index
DTCParityEn	4	0x0	Enables parity protection of the DTC
DTCInvalidationSel	9:8	0x0	Selects the DTC invalidation algorithm 00=Invalidate the entire DTC 01=Fast imprecise invalidation 10=Sequential precise invalidation 11=Partial sequential precise invalidation
DTCSoftInvalidate	10	0x0	Software may write this register to 1 to invalidate all entries in the DTC
DTCBypass	13	0x0	When set, all requests bypass the DTC.
DTCParitySupport (R)	15	0x0	0=The DTC does not support parity protection 1=The DTC supports parity protection
DTCWays (R)	23:16	0x0	Indicates the number of ways in the DTC
DTCEntries (R)	31:28	0x0	The number of entries in the DTC is indicated as 2^DTCEntries

L2_DTC_HASH_CONTROL - RW - 32 bits - L2CFGIND:0x11			
Field Name	**Bits**	**Default**	**Description**
DTCFuncBits	1:0	0x2	Sets the number of function bits to use when using ReqID to form the DTC address
DTCDevBits	4:2	0x0	Sets the number of device bits to use when using ReqID to form the DTC address

DTCBusBits	8:5	0x3	Sets the number of bus bits to use when using ReqID to form the DTC address. The following equation must be satisified. Func_bits + Dev_Bits + Bus_Bits <= log2(DTC entries / DTC associativity)

L2_DTC_WAY_CONTROL - RW - 32 bits - L2CFGIND:0x12			
Field Name	**Bits**	**Default**	**Description**
DTCWayDisable	15:0	0x0	Each bit in this register disables a way in the DTC when set to 1. An implementation may have less than 32 ways. The entire cache may be disabled by setting the DTCWays lower bits of this register.
DTCWayAccessDisable	31:16	0x0	

L2_ITC_CONTROL - RW - 32 bits - L2CFGIND:0x14			
Field Name	**Bits**	**Default**	**Description**
ITCReplacementSel	1:0	0x1	Selects the ITC replacement algorithm. Implementation may not support all replacement algorithms
ITCLRUUpdatePri	3	0x0	0=Reads update replacement state bits when there is a simultaneous read and write to the same ITC index 1=Writes update replacement state bits when there is a simultaneous read and write to the same ITC index
ITCParityEn	4	0x0	Enables parity protection of the ITC
ITCInvalidationSel	9:8	0x0	Selects the ITC invalidation algorithm 00=Invalidate the entire ITC 01=Fast imprecise invalidation 10=Sequential precise invalidation 11=Partial sequential precise invalidation
ITCSoftInvalidate	10	0x0	Software may write this register to 1 to invalidate all entries in the ITC
ITCBypass	13	0x0	When set, all requests bypass the ITC.
ITCParitySupport (R)	15	0x0	0=The ITC does not support parity protection 1=The ITC supports parity protection
ITCWays (R)	23:16	0x0	Indicates the number of ways in the ITC
ITCEntries (R)	31:28	0x0	The number of entries in the ITC is indicated as 2^ITCEntries

L2_ITC_HASH_CONTROL - RW - 32 bits - L2CFGIND:0x15			
Field Name	**Bits**	**Default**	**Description**
ITCFuncBits	1:0	0x2	Sets the number of function bits to use when using ReqID to form the ITC address
ITCDevBits	4:2	0x0	Sets the number of device bits to use when using ReqID to form the ITC address
ITCBusBits	8:5	0x3	Sets the number of bus bits to use when using ReqID to form the ITC address. The following equation must be satisified. Func_bits + Dev_Bits + Bus_Bits <= log2(ITC entries / ITC associativity)
ITCAddressMask	31:16	0xffff	This register is a bit-wise AND mask that selects which bits from the untranslated interrupt MT[2:0],Vector are used to index into the ITC.

L2_ITC_WAY_CONTROL - RW - 32 bits - L2CFGIND:0x16			
Field Name	**Bits**	**Default**	**Description**
ITCWayDisable	15:0	0x0	Each bit in this register disables a way in the ITC when set to 1. An implementation may have less than 32 ways. The entire cache may be disabled by setting the ITCWays lower bits of this register.
ITCWayAccessDisable	31:16	0x0	

L2_PTC_A_CONTROL - RW - 32 bits - L2CFGIND:0x18			
Field Name	**Bits**	**Default**	**Description**
PTCAReplacementSel	1:0	0x1	Selects the PTC A sub-cache replacement algorithm. Implementation may not support all replacement algorithms
PTCALRUUpdatePri	3	0x0	0=Reads update replacement state bits when there is a simultaneous read and write to the same PTCA index 1=Writes update replacement state bits when there is a simultaneous read and write to the same PTCA index
PTCAParityEn	4	0x0	Enables parity protection of the PTC A sub-cache
PTCAInvalidationSel	9:8	0x0	Selects the PTC A sub-cache invalidation algorithm 00=Invalidate the entire PTC A sub-cache 01=Fast imprecise invalidation 10=Sequential precise invalidation 11=Partial sequential precise invalidation
PTCASoftInvalidate	10	0x0	Software may write this register to 1 to invalidate all entries in the PTC A sub-cache
PTCA2MMode	11	0x0	When set, the PTC A sub-cache stores 2M pages instead of 4K pages
PTCABypass	13	0x0	When set, all requests bypass the PTC A sub-cache.
PTCAParitySupport (R)	15	0x0	0=The PTC A sub-cache does not support parity protection 1=The PTC A sub-cache supports parity protection
PTCAWays (R)	23:16	0x0	Indicates the number of ways in the PTC A sub-cache
PTCAEntries (R)	31:28	0x0	The number of entries in the PTC A sub-cache is indicated as 2^PTCAEntries

L2_PTC_A_HASH_CONTROL - RW - 32 bits - L2CFGIND:0x19			
Field Name	**Bits**	**Default**	**Description**
PTCAFuncBits	1:0	0x2	Sets the number of function bits to use when using ReqID to form the PTC A sub-cache address
PTCADevBits	4:2	0x0	Sets the number of device bits to use when using ReqID to form the PTC A sub-cache address
PTCABusBits	8:5	0x3	Sets the number of bus bits to use when using ReqID to form the PTC A sub-cache address. The following equation must be satisified. FuncBits + DevBits + BusBits <= log2(PTC A sub-cache entries / PTC A sub-cache associativity)
PTCAAddressMask	31:16	0xffff	This register is a bit-wise AND mask that selects which virtual address bits are used to index into the PTC A sub-cache.

L2_PTC_A_WAY_CONTROL - RW - 32 bits - L2CFGIND:0x1A			
Field Name	**Bits**	**Default**	**Description**
PTCAWayDisable	15:0	0x0	Each bit in this register disables a way in the PTC A sub-cache when set to 1. An implementation may have less than 32 ways. The entire cache may be disabled by setting the PTCAWays lower bits of this register.
PTCAWayAccessDisable	31:16	0x0	

L2_PTC_B_CONTROL - RW - 32 bits - L2CFGIND:0x1C			
Field Name	**Bits**	**Default**	**Description**
PTCBReplacementSel	1:0	0x1	Selects the PTC B sub-cache replacement algorithm. Implementation may not support all replacement algorithms
PTCBLRUUpdatePri	3	0x0	0=Reads update replacement state bits when there is a simultaneous read and write to the same PTCB index 1=Writes update replacement state bits when there is a simultaneous read and write to the same PTCB index
PTCBParityEn	4	0x0	Enables parity protection of the PTC B sub-cache
PTCBInvalidationSel	9:8	0x0	Selects the PTC B sub-cache invalidation algorithm 00=Invalidate the entire PTC B sub-cache 01=Fast imprecise invalidation 10=Sequential precise invalidation 11=Partial sequential precise invalidation
PTCBSoftInvalidate	10	0x0	Softwares may write this register to 1 to invalidate all entries in the PTC B sub-cache
PTCB2MMode	11	0x0	When set, the PTC B sub-cache stores 2M pages instead of 4K pages.
PTCBBypass	13	0x0	When set, all requests bypass the PTC B sub-cache.
PTCBParitySupport (R)	15	0x0	0=The PTC B sub-cache does not support parity protection 1=The PTC B sub-cache supports parity protection
PTCBWays (R)	23:16	0x0	Indicates the number of ways in the PTC B sub-cache
PTCBEntries (R)	31:28	0x0	The number of entries in the PTC B sub-cache is indicated as 2^PTCBEntries

L2_PTC_B_HASH_CONTROL - RW - 32 bits - L2CFGIND:0x1D			
Field Name	**Bits**	**Default**	**Description**
PTCBFuncBits	1:0	0x2	Sets the number of function bits to use when using ReqID to form the PTC B sub-cache address
PTCBDevBits	4:2	0x0	Sets the number of device bits to use when using ReqID to form the PTC B sub-cache address
PTCBBusBits	8:5	0x3	Sets the number of bus bits to use when using ReqID to form the PTC B sub-cache address. The following equation must be satisified. FuncBits + DevBits + BusBits <= log2(PTC B sub-cache entries / PTC B sub-cache associativity)
PTCBAddressMask	31:16	0xffff	This register is a bit-wise AND mask that selects which virtual address bits are used to index into the PTC B sub-cache.

L2_PTC_B_WAY_CONTROL - RW - 32 bits - L2CFGIND:0x1E			
Field Name	**Bits**	**Default**	**Description**
PTCBWayDisable	15:0	0x0	
PTCBWayAccessDisable	31:16	0x0	

L2_CREDIT_CONTROL_2 - RW - 32 bits - L2CFGIND:0x20			
Field Name	**Bits**	**Default**	**Description**
QUEUECredits	5:0	0x0	QUEUE credit override value
QUEUEOverride	7	0x0	Changing this register from 0 to 1 overrides the QUEUE credit counter with QUEUECredits. This should only be performed when the IOMMU is idle
FLTCMBCredits	13:8	0x0	FLTCMB credit override value
FLTCMBOverride	15	0x0	Changing this register from 0 to 1 overrides the FLTCMB credit counter with FLTCMBCredits. This should only be performed when the IOMMU is idle
FCELCredits	21:16	0x0	FCEL credit override value
FCELOverride	23	0x0	Changing this register from 0 to 1 overrides the FCEL credit counter with FCELCredits. This should only be performed when the IOMMU is idle

L2_ERR_RULE_CONTROL_3 - RW - 32 bits - L2CFGIND:0x30			
Field Name	**Bits**	**Default**	**Description**
ERRRuleLock1	0	0x0	This register is write-once. Setting this register bit locks the error detection rule set in ERRRuleDisable3/4/5
ERRRuleDisable3	31:4	0x0	Each bit in this register disables an error detection rule in the IOMMU

L2_ERR_RULE_CONTROL_4 - RW - 32 bits - L2CFGIND:0x31			
Field Name	**Bits**	**Default**	**Description**
ERRRuleDisable4	31:0	0x0	Each bit in this register disables an error detection rule in the IOMMU

L2_ERR_RULE_CONTROL_5 - RW - 32 bits - L2CFGIND:0x32			
Field Name	**Bits**	**Default**	**Description**
ERRRuleDisable5	31:0	0x0	Each bit in this register disables an error detection rule in the IOMMU

L2_DEBUG_2 - RW - 32 bits - L2CFGIND:0x43			
Field Name	**Bits**	**Default**	**Description**
L2DEBUG2	31:0	0x0	Reserved for ECOs

L2_DEBUG_3 - RW - 32 bits - L2CFGIND:0x44			
Field Name	**Bits**	**Default**	**Description**
L2DEBUG3	31:0	0x0	Bit[0] - Enable fix to handle DTE page mode attributes combined with IoCtl and SysMgt. Bit[1] - Enable fix to avoid aborting untranslated memory requests to the exclusion range, system management address range or IO space range address when they are configured to block or pass trough requests, and the corresponding device table entry has translation valid bit cleared Bit[2] - Reserved Bit[3] - Enable fix to avoid treating interrupt requests as untranslated memory requests or address translation requests from exclusion range under specific conditions Bit[4] - Enable fix to avoid access right checks for pretranslated requests. Bit[31:5] - Reserved

Reserved for ECOs

L2_STATUS_1 - RW - 32 bits - L2CFGIND:0x45			
Field Name	**Bits**	**Default**	**Description**
L2STATUS1 (R)	31:0	0x0	Internal IOMMU L2B status

L2_CONTROL_5 - RW - 32 bits - L2CFGIND:0x4C			
Field Name	**Bits**	**Default**	**Description**
QueueArbFBPri	0	0x1	0=Requests in the miss queue and the feedback queue are arbitrated in a round-robin manner 1=Requests in the feedback queue are given priority over requests in the miss queue
PTCAddrTransReqUpdate	1	0x1	0=PTEs from address translation requests are not cached 1=PTEs from address translation requests are cached in the L2 according to the Cache bit in the DTE
FC1Dis	2	0x0	0=FC1 flow control loop enabled 1=FC1 flow control loop disabled
DTCUpdateVOneIVZero	3	0x0	0=DTEs with V=1 and IV=0 are not cached in the DTC 1=DTEs with V=1 and IV=0 are cached in the DTC
DTCUpdateVZeroIVOne	4	0x0	0=DTEs with V=0 and IV=1 are not cached in the DTC 1=DTEs with V=0 and IV=1 are cached in the DTC
FC2Dis	5	0x0	0=FC2 flow-control loop is enabled 1=FC2 flow-control look is disabled
FC3Dis	6	0x0	0=FC3 flow-control loop is enabled 1=FC3 flow-control look is disabled
FC2AltMode	7	0x0	0=FC2 primary flow-control mode 1=FC2 alternate flow-control mode
Reserved	31:8	0x0	

L2_CONTROL_6 - RW - 32 bits - L2CFGIND:0x4D			
Field Name	**Bits**	**Default**	**Description**
SeqInvBurstLimitInv	7:0	0x8	Sets the number of consecutive invalidation requests to perform when doing sequential invalidation. PDC and invalidation requests will alte rnate access to the PDC based upon SeqInvBurstLimitInv and SeqInvBurstLimitPDCReq.
SeqInvBurstLimitPDCReq	15:8	0x8	Sets the number of consecutive iommu PDC requests to perform when doing sequential invalidation. PDC and invalidation requests will alternat e access to the PDC based upon SeqInvBurstLimitInv and SeqInvBurstLimitPDCReq.
SeqInvBurstLimitEn	16	0x1	Enable stalling PDC requests to allow invalidation cycles to make forward progress based upon SeqInvBurstLimitInv and SeqInvBurstLimitPDCReq
Perf2Threshold	31:24	0x0	Fifo threshold level used to calculate certain performance counter values.

L2_PDC_CONTROL - RW - 32 bits - L2CFGIND:0x50			
Field Name	**Bits**	**Default**	**Description**
PDCReplacementSel	1:0	0x1	Selects the PDC replacement algorithm. Implementation may not support all replacement algorithms
PDCLRUUpdatePri	3	0x0	0=Reads update replacement state bits when there is a simultaneous read and write to the same PDC index 1=Writes update replacement state bits when there is a simultaneous read and write to the same PDC index
PDCParityEn	4	0x0	Enables parity protection of the PDC if the device supports parity
PDCInvalidationSel	9:8	0x0	Selects the PDC invalidation algorithm 00=Invalidate the entire PDC 01=Fast imprecise invalidation 10=Sequential precise invalidation 11=Partial sequential precise invalidation
PDCSoftInvalidate	10	0x0	Software may write this register to 1 to invalidate all entries in the PDC
PDCSearchDirection	12	0x0	0=Search PDC from higher levels down 1=Search PDC from lower levels up
PDCBypass	13	0x0	When set, all requests bypass the PDC. This prevents the multiple issue of requests and increases maximum rate of requests to the table-walker.
PDCParitySupport (R)	15	0x0	0=The PDC does not support parity protection 1=The PDC supports parity protection
PDCWays (R)	23:16	0x0	Indicates the number of ways in the PDC
PDCEntries (R)	31:28	0x0	Indicates the number of entries in the PDC is indicated as 2^PDCEntries

L2_PDC_HASH_CONTROL - RW - 32 bits - L2CFGIND:0x51			
Field Name	**Bits**	**Default**	**Description**
PDCDomainBits	5:0	0x7	Selects the number of domain bits to use as part of the index into the PDC
PDCLvlHash	8	0x1	When set to 1, the PDE level is used as part of the hash for the cache index.
PDCUpperLvlAddrHash	9	0x1	When set to 1, the PDC cache index is partially formed using the xor of the LSBs of virtual address bits for all levels greater than or equal to the stored/searched level.
PDCAddressMask	31:16	0xffff	This register is a bit-wise AND mask that selects which virtual address bits are used to index into the PDC.

L2_PDC_WAY_CONTROL - RW - 32 bits - L2CFGIND:0x52			
Field Name	**Bits**	**Default**	**Description**
PDCWayDisable	15:0	0x0	Each bit in this register disables a way in the PDC when set to 1. An implementation may have less than 32 ways. The entire cache may be disabled by setting the PDCWays lower bits of this register.
PDCWayAccessDisable	31:16	0x0	

L2_TW_CONTROL - RW - 32 bits - L2CFGIND:0x54			
Field Name	**Bits**	**Default**	**Description**
TWQueueLimit	5:0	0x10	Limits the number of outstanding table-walker requests
TWForceCoherent	6	0x0	1=Table-walker always genereates coherent requests. The DTE SD bit is ignored when this bit is set to 1.
TWPrefetchEn	8	0x0	Enables prefetching in the table-walker
TWPrefetchOnly4KDis	9	0x0	1=Allow non-4K pages to be prefetched 0=Only 4K pages are prefetched
TWPTEOnUntransExcl	10	0x0	0=Table walker returns DTE to L1 on an untranslated exclusion range access 1=Table walker returns PTE to L1 on an untranslated exclusion range access
TWPTEOnAddrTransExcl	11		0=Table walker returns DTE to L1 on an address translation exclusion range access 1=Table walker returns PTE to L1 on an address translation exclusion range access
TWPrefetchRange	14:12	0x1	Selects the number of pages to prefetch

L2_CP_CONTROL - RW - 32 bits - L2CFGIND:0x56			
Field Name	**Bits**	**Default**	**Description**
CPPrefetchDis	0	0x0	1=Command processor fetches and executes only one command at a time 0=Command processor prefetches available commands into its internal storage
CPFlushOnWait	1	0x0	1=Command processor flushes out old requests on completion wait 0=No flush is performed on completion wait

CPFlushOnInv	2	0x1	1=Command processor flushes out old requests on every invalidation command 0=No flush is performed during invalidations
CPRdDelay	31:16	0x0	Command processor read delay

L2_TW_CONTROL_1 - RW - 32 bits - L2CFGIND:0x60			
Field Name	**Bits**	**Default**	**Description**
TWDebugEn	0	0x0	Enables table-walker trace debug mode
TWDebugNoWrap	1	0x0	1=Table-walker trace to stop at the top of the trace buffer 0=Table-walker trace wraps around at the top of the trace buffer
TWDebugForceDisable	2	0x0	When set to 1, this register disables the TW Debug feature until a cold-reset is performed
TWDebugMask	31:15	0x0	Defines the table-walker trace buffer size by masking address bits 31:16

L2_TW_CONTROL_2 - RW - 32 bits - L2CFGIND:0x61			
Field Name	**Bits**	**Default**	**Description**
TWDebugAddrLo	31:12	0x0	Base address bits 31:12 for table-walker trace debug

L2_TW_CONTROL_3 - RW - 32 bits - L2CFGIND:0x62			
Field Name	**Bits**	**Default**	**Description**
TWDebugAddrHi	31:0	0x0	Base address bits 51:32 for table-walker trace debug

L2_INT_CONTROL - RW - 32 bits - L2CFGIND:0x6A			
Field Name	**Bits**	**Default**	**Description**
IntEventOrderEn	0	0x1	Enable ordering between interrupts and event log writes
IntCPOrderEn	1	0x1	Enable ordering between interrupts and command processor writes

L2_CREDIT_CONTROL_0 - RW - 32 bits - L2CFGIND:0x70			
Field Name	**Bits**	**Default**	**Description**
FC1Credits	5:0	0x0	FC1 credit override value
FC1Override	7	0x0	Changing this register from 0 to 1 overrides the FC1 credit counter with FC1Credits. This should only be performed when the IOMMU is idle
FC2Credits	13:8	0x0	FC2 credit override value
FC2Override	15	0x0	Changing this register from 0 to 1 overrides the FC2 credit counter with FC2Credits. This should only be performed when the IOMMU is idle
FC3Credits	21:16	0x0	FC3 credit override value
FC3Override	23	0x0	Changing this register from 0 to 1 overrides the FC3 credit counter with FC3Credits. This should only be performed when the IOMMU is idle
DTECredits	29:24	0x0	DTE credit override value

DTEOverride	31	0x0	Changing this register from 0 to 1 overrides the DTE credit counter with DTECredits. This should only be performed when the IOMMU is idle

L2_CREDIT_CONTROL_1 - RW - 32 bits - L2CFGIND:0x71			
Field Name	**Bits**	**Default**	**Description**
PDTIECredits	5:0	0x0	PDTIE credit override value
PDTIEOverride	7	0x0	Changing this register from 0 to 1 overrides the PDTIE credit counter with PDTIECredits. This should only be performed when the IOMMU is idle
TWELCredits	13:8	0x0	TWEL credit override value
TWELOverride	15	0x0	Changing this register from 0 to 1 overrides the TWEL credit counter with TWELCredits. This should only be performed when the IOMMU is idle

L2_MCIF_CONTROL - RW - 32 bits - L2CFGIND:0x78			
Field Name	**Bits**	**Default**	**Description**
MCIFBaseReadCredits	4:0	0x8	Sets the number of base-channel read credits between the IOMMU L2 and the HTIU/ORB. This register requires a warm-reset to take effect
MCIFIsocReadCredits	12:8	0x8	Sets the number of isoc-channel read credits between the IOMMU L2 and the HTIU/ORB. This register requires a warm-reset to take effect
MCIFBaseWriteHdrCredits	20:16	0x8	Sets the number of base-channel write header credits between the IOMMU L2 and the HTIU/ORB. This register requires a warm-reset to take effect
MCIFBaseWriteDataCredits	28:24	0x8	Sets the number of base-channel write data credits between the IOMMU L2 and the HTIU/ORB. This register requires a warm-reset to take effect

L2_ERR_RULE_CONTROL_0 - RW - 32 bits - L2CFGIND:0x80			
Field Name	**Bits**	**Default**	**Description**
ERRRuleLock0	0	0x0	This register is write-once. Setting this register bit locks the error detection rule set in ERRRuleDisable0/1/2
ERRRuleDisable0	31:4	0x0	Each bit in this register disables an error detection rule in the IOMMU

L2_ERR_RULE_CONTROL_1 - RW - 32 bits - L2CFGIND:0x81			
Field Name	**Bits**	**Default**	**Description**
ERRRuleDisable1	31:0	0x0	Each bit in this register disables an error detection rule in the IOMMU

L2_ERR_RULE_CONTROL_2 - RW - 32 bits - L2CFGIND:0x82			
Field Name	**Bits**	**Default**	**Description**
ERRRuleDisable2	31:0	0x0	Each bit in this register disables an error detection rule in the IOMMU

2.5.8 HTIUNBIND Registers

NB_HT_CLK_CNTL_RECEIVER_COMP_CNTL - RW - 32 bits - HTIUNBIND:0x0			
Field Name	**Bits**	**Default**	**Description**
RX_COMPDATA	4:0	0x10	Transmitter rising edge compensation circuitry data value
RX_CTL	6:5	0x0	Receiver rising edge PHY control value 00=Apply RX_CALCOMP directly as the compensation 01=Apply RX_COMPDATA directly as the compensation 10=Apply the sum of RX_CALCOMP and RX_COMPDATA 11=Apply the diff of RX_CALCOMP and RX_COMPDATA
PCIE_STICKY_STATUS_EN	7	0x0	1=PCIe sticky error status registers are preserved across warm reset 0=PCIe sticky error status registers are cleared during warm reset
RX_CALCCOMP (R)	12:8	0x10	Calculated compensation value for the receiver
RESERVED_14_13	14:13	0x0	Bit [14]=CfgHTiu_HT_RX_COMPOVR Bit [13]=CfgHTiu_HT_RX_FCOMPCYC
SUCU	15	0x0	Speed up compensation update: 0=Link PHY compensation values are allowed to changed every 1ms 1=Link PHY compensation values are allowed to changed every 1us
ICGSMAF	23:16	0x0	Internal clock gating system management: 0=No power reduction 1=IC power is reduced through gatind of internal clocks
REVERVED_25to24 (R)	25:24	0x0	Bit 25 - CfgHTiu_HT_TX_UPDATE Bit 24 - CfgHTiu_HT_RX_UPDATE
RESERVED_29to26	29:26	0x0	Reserved for future use. This register controls no hardware
SULS	30	0x0	Speeds up connection sequence for frequency change 0=PLL lock timer is 100 us 1=PLL lock timer is 1us
CGEN	31	0x0	Clock gating enable: 0=Internal clock gating is disabled 1=Internal clock gating is enabled
HT_CLK_CNTL_RECEIVER_COMP_CNTL			

NB_HT_TRANS_COMP_CNTL - RW - 32 bits - HTIUNBIND:0x1			
Field Name	**Bits**	**Default**	**Description**
TXP_COMPDATA	4:0	0xc	Calculates the compensation value for the transmitter falling edge
TXP_CTL	6:5	0x0	Transmitter falling edge PHY control value: 00=Apply TXP_CALCCOMP directly 01=Apply TXP_COMPDATA directly 10=Apply the sum of TXP_CALCCOMP and TXP_COMPDATA 11=Apply the diff of TXP_CALCCOMP and TXP_COMPDATA
RESERVED_7	7	0X0	Reserved for future use. This register controls no hardware
TXP_CALCCOMP (R)	12:8	0xc	Transmitter falling edge compensation circuitry data value
RESERVED_15_13	15:13	0x0	Bit [15]=CfgHTiu_HT_EMP_EN_TST Bit [14]=CfgHTiu_HT_TX_COMPOVR Bit [13]=CfgHTiu_HT_TX_FCOMPCYC
TXN_COMPDATA	20:16	0xc	Transmitter falling edge compensation circuitry data value

TXN_CTL	22:21	0x0	Transmitter falling edge PHY control value: 00=Apply TXN_CALCCOMP directly 01=Apply TXN_COMPDATA directly 10=Apply the sum of TXN_CALCCOMP and TXN_COMPDATA 11=Apply the diff of TXN_CALCCOMP and TXN_COMPDATA
RESERVED_23	23	0X0	Reserved for future use. This register controls no hardware
TXN_CALCCOMP (R)	28:24	0xc	
RESERVED_31to29	31:29	0x0	Reserved for future use. This register controls no hardware
HT transmitter comp control			

HTIU_DEBUG - RW - 32 bits - HTIUNBIND:0x5			
Field Name	**Bits**	**Default**	**Description**
HTIU_DEBUG_1_0	1:0	0x0	Bit 1 - Enable TXCLKs on debug bus - Do not turn this on in production Bit 0 - Enable RXCLKs on debug bus - Do not turn this on in production
HTIU_DEBUG_31_2	31:2	0x0	Bit 31 - Enable GSM Hysterisis timer for Bug4122 Bit 30 - Timer value for GSM Hysterisis logic (count in LCLK, related to Bug4122) Bit 19 - Improve power reduction during link disconnect Bit 18 - Reduce false retry reporting due to LDTSTOP disconnect Bit 17 - Enable proper handling of 64 bit register access to IOMMU/IOAPIC space Bit 16 - Prevent Nop insertion in extended address command in HT1 Bit 15 - Enable proper parity error reporting for IOMMU L2A and L2B Bit 14 - Enhance error detection during training2 Bit 13 - Enable earlier CDR freeze prior to disconnect Bit 12 - Allow DMA P request to pass NP request Bit 11 - Reserved Bit 10 - Fix Data Rate Matching feature for 16 bit link Bit 9 - Interrupt Hi Priority Control Bit 8 - Fix HT3 flow-control buffer release procedure Bit 7 - GSMinC3Only - Detect GSM traffic in C3 only Bit 6 - Prevent false error logging due to reset skew Bit 5 - Disable response fix Bit 4 - Reduce HT1 LDTSTOP disconnect delay Bit 3 - Generate Disconnect Nop without credit release Bit 2 - Extend DLL reset to be 100ns coming out of reset

HTIU debug

HTIU_DOWNSTREAM_CONFIG - RW - 32 bits - HTIUNBIND:0x6			
Field Name	**Bits**	**Default**	**Description**
HTdSafeIssue	0	0x1	Setting this bit causes outstanding non-posted transactions to block the posted channel. It should be cleared to avoid a deadlock scenario 0=PW before NP done 1=PW after NP done
HTdPStreamEn	1	0x0	Downstream posted-write streaming. This register requires LDTSTOP or RESET to take effect 0=PW Streaming Disabled 1=PW Streaming Enabled

CfgHTiuRdRspPassPWMode	3:2	0x0	PassPW for upstream read responses 0=00 - From request packet 1=01 - From IOC/PCIe 2=10 - Always 0 3=11 - Always 1
CfgHTiuTgtDonePassPWMode	5:4	0x0	PassPW for upstream tgtdone 0=00 - Normally 1 but 0 for I/O cycle 1=01 - From IOC/PCIe 2=10 - Always 0 3=11 - Always 1
CfgHTiuReqPassPWMode	7:6	0x0	PassPW for downstream requests to IOC 0=00 - From request packet 1=01 - reserved 2=10 - Always 0 3=11 - Always 1
CfgHTiuDisableNPDWait	8	0x0	This bit should always be set to 0 for proper operation
CfgHTiuPDStage2En	9	0x0	Enables larger buffer for downstream posted data and higher performance
CfgHTiuLockIOCArb	10	0x0	Lock IOC arbiter. Should always be set to 0
CfgHTiuHtdNoErr	11	0x0	Setting this bit prevents the chipset from sending error bits in upstream responses to the CPU
CfgHtiuTxMaxRspCnt	12	0x0	Reserved. This register controls no hardware
CfgHTiuLargeRspCnt	13	0x0	Enable 127 response buffer mode
ReqCompatModeDis	14	0x0	Disables Compat bit decoding in htiu. Should be set to 0 for proper operation
FIDStpGntDetect	15	0x0	Enables wait for display on StpGnt with FID SMAF detection. Should be disabled if no internal gfx
C3StpGntDetect	16	0x0	Enables wait for display on StpGnt with C3 SMAF detection. Should be disabled if no internal gfx
AllowNPPassPW	17	0x0	Enables PassPW functionality in non-posted transactions
FastNPAvail	18	0x1	Enables faster turnaround of NP buffer availability. Should be set to 1
GCMDelay	21:19	0x3	Delay between back-to-back transactions issued by GCM. It should not be set lower than 0x3
GCMPCDelay	24:22	0x3	Delays between back-to-back PC transactions issued by GCM. It should not be set lower than 0x3
DispIntAck	25	0x0	Ignores ACK from Display on StpGnt wait and generate ACK internally
PCIE_HT_NP_MEM_WRITE	26	0x0	Enables NP protocol over PCIe for memory-mapped writes targeting LPC. Set this bit to avoid a deadlock condition
SCAS_EN	27	0x0	Enables SCAS feature. All traffic between 1 and 2GB is mapped onto a special 64 byte storage space. Should be used for testing only
DbgCntrMode	28	0x0	Enables rotating htiu debug bus
Reserved_31_29	31:29	0x0	Bit [29]=Reserved. This register controls no hardware. Bit [30]=Enables a fix for tagging downstream NP requests. Bit [31]=RReserved. This register controls no hardware.

HTIU_UPSTREAM_ARB_CONTROL_0 - RW - 32 bits - HTIUNBIND:0x7			
Field Name	**Bits**	**Default**	**Description**
ioc_bw_opt_en	0	0x0	Optimize IOC byte write by detecting Consecutive DW mask and translate the request to DW write. 0 - Disable
Intr_ppw	1	0x0	Sets the PassPW attribute for HTIU internally generated interrupt requests
Intr_coherent	2	0x0	Sets the coherent attribute for HTIU internally generated interrupt requests

ReqPoisonDis	3	0x0	Disable propagation of upstream poison attribute
IommuBwOptEn	4	0x0	Enable bandwidth optimization for byte writes coming from IOMMU
VC1WrAbort	5	0x1	When set, this register disables write requests propagated from the VC1 interface. This register must be clear for IOAPIC to operate properly
DropZeroMaskWrEn	15	0x0	Enable zero-byte DMA writes to be dropped
UnadjustThrottlingStpclk	30	0x0	1 = Throttling stpclk messages do not have their unitid altered. 0 = Throttling stpclk messages have their unitid altered to avoid a deadlock condition in older processors.
HTIU upstream configuration 0			

HTIU_UPSTREAM_ARB_CONTROL_1 - RW - 32 bits - HTIUNBIND:0x8			
Field Name	**Bits**	**Default**	**Description**
NpWrrLenA	7:0	0x8	NP arbiter round-robin burst length
NpWrrLenB	15:8	0x8	NP arbiter round-robin burst length
NpWrrLenC	23:16	0x8	NP arbiter round-robin burst length
HTIU upstream arbitration control			

HTIU_UPSTREAM_ARB_CONTROL_2 - RW - 32 bits - HTIUNBIND:0x9			
Field Name	**Bits**	**Default**	**Description**
PWrrLenaA	7:0	0x8	P arbiter round-robin burst length
PWrrLenaB	15:8	0x8	P arbiter round-robin burst length
PWrrLenaC	23:16	0x8	P arbiter round-robin burst length
PWrrLenaD	31:24	0x8	P arbiter round-robin burst length
HTIU upstream arbitration control			

HTIU_UPSTREAM_ARB_CONTROL_3 - RW - 32 bits - HTIUNBIND:0xA			
Field Name	**Bits**	**Default**	**Description**
PWrrLenE	7:0	0x8	P arbiter round-robin burst length
PWrrLenF	15:8	0x8	P arbiter round-robin burst length
HTIU upstream arbitration control			

HTIU_UPSTREAM_ARB_CONTROL_4 - RW - 32 bits - HTIUNBIND:0xB			
Field Name	**Bits**	**Default**	**Description**
IsocWrrLenA	7:0	0x8	Isoc arbiter round-robin burst length
IsocWrrLenB	15:8	0x8	Isoc arbiter round-robin burst length
HTIU upstream arbitration control			

HTIU_UPSTREAM_ARB_CONTROL_5 - RW - 32 bits - HTIUNBIND:0xC			
Field Name	**Bits**	**Default**	**Description**
GCMWrrLenA	7:0	0x8	read-write arbiter round-robin burst length
GCMWrrLenB	15:8	0x8	read-write arbiter round-robin burst length
HTIU upstream arbitration control			

HTIU_UPSTREAM_ARB_CONTROL_6 - RW - 32 bits - HTIUNBIND:0xD			
Field Name	**Bits**	**Default**	**Description**
ForceReqToIsoc	31:0	0x0	Each bit in this register forces requests from the corresponding unitID to go into the high priority channel.
HTIU upstream arbitration control			

HTIU_SCRATCH_0 - RW - 32 bits - HTIUNBIND:0xF			
Field Name	**Bits**	**Default**	**Description**
HTIU_SCRATCH_0	31:0	0x0	Reserved for future use. This register controls no hardware.

HTIU_STATUS_0 - RW - 32 bits - HTIUNBIND:0x10			
Field Name	**Bits**	**Default**	**Description**
HTIUStatus	31:0	0x0	Reserved for future use. This register controls no hardware.

HTIU_SCRATCH_2 - RW - 32 bits - HTIUNBIND:0x11			
Field Name	**Bits**	**Default**	**Description**
HTIU_SCRATCH_2	31:0	0x0	Reserved for future use. This register controls no hardware.

HTIU_SCRATCH_3 - RW - 32 bits - HTIUNBIND:0x12			
Field Name	**Bits**	**Default**	**Description**
HTIU_SCRATCH_3	31:0	0x0	Reserved for future use. This register controls no hardware.

HTIU_SCRATCH_4 - RW - 32 bits - HTIUNBIND:0x13			
Field Name	**Bits**	**Default**	**Description**
HTIU_SCRATCH_4	31:0	0x0	Reserved for future use. This register controls no hardware.

HTIU_SCRATCH_5 - RW - 32 bits - HTIUNBIND:0x14			
Field Name	**Bits**	**Default**	**Description**
HTIU_SCRATCH_5	31:0	0x0	Reserved for future use. This register controls no hardware.

Link_State_Control_0 - RW - 32 bits - HTIUNBIND:0x15			
Field Name	**Bits**	**Default**	**Description**
HT2InitTmr	19:0	0xfffff	Timeout time for HT1 initialization sequence in HT2 mode. This counter counts in LCLK cycles. This register is cleared on POWERGOOD and not RESET

HT1Bypass	20	0x0	Reserved. This register controls no hardware. This register is cleared on POWERGOOD and not RESET
ExtendedSMCEn	21	0x0	Enables upstream decoding of 12-bit system management messages. This register is cleared on POWERGOOD and not RESET
StrictTM4Detection	22	0x0	Ensures that all active lanes see Training Marker 4 at the same time during HT3 initialization. A failure of this check results in an immediate retry. This register is cleared on POWERGOOD and not RESET
GSMAllMode	23	0x0	GSM All Mode. This register is cleared on POWERGOOD and not RESET. 1=In lta stage, identify all requests as GSM requests 0=In lta stage, only indicate GSM requests as GSM requests
LS2HotMode	24	0x0	HT LS2 Hot Mode. This register is cleared on POWERGOOD and not RESET. 1=Use HT transmit clock to keep receiver DLLs running during LS2 0=DLLs are placed into either reset or powerdown state during LS2
HT3HiZMode	25	0x0	HT LS3 Transmitter HiZ Mode. This register is cleared on POWERGOOD and not RESET. 1=HT transmitter goes into the HiZ state during LS3 0=HT transmitter goes into the TxGndTrm state during LS3
LS3TermDis	26	0x0	HT LS3 Receiver Termination Disable 1=HT receiver termination is disabled during LS3 0=HT receiver termination is enabled during LS3
LS2DLLPwrDn	27	0x0	HT LS2 DLL Power Down Mode 1=HT receiver DLLs are powered down during LS2 0=HT receiver DLLs are not powered down during LS2.
TimeMarginMode	28	0x0	HT Receiver Time Margining Mode 1=Enable time margining only during operational, bist and loopback modes 0=Enable time margining whenever clock recovery is active including training 1,2,3 states
MinDisconTmr	29	0x0	HT Minimum Disconnection Time Timer 1=Force link state controller to stay in the disconnected state for at least 100ns. This applies to both HT1 and HT3 modes. 0=No minimum time to stay in the disconnected state
RxVBControl	30	0x0	Receiver VBias Control 1=HT receiver VBias is disabled whenever receiver termination is disabled 0=HT receiver VBias is always enabled
TxVBControl	31	0x0	Transmitter VBias Control 1=HT transmitter VBias is disabled whenever all lanes are in HiZ 0=HT transmitter VBias is always enabled

Link_State_Control_1 - RW - 32 bits - HTIUNBIND:0x16			
Field Name	**Bits**	**Default**	**Description**
HT1ReconCnt	9:0	0x190	HT1 reconnection timer. This timer determines the delay before HT1 initialization used to enable the transmitter and allow it to stabilize. It counts on LCLK

spare_15_10	15:10	0x0	Bit [10]=ExtendDLLReset. When set to 1, DLL reset is extended to 100ns Bit [11]=When set to 1 enables proper resetting of the TX PHY in HT1 mode when toggling LDTSTOP Bits [14:12]=Controls the RX_BIAS_SEL 0, 1, 2 respectively; Default=000
HT1ReconCntRxEn	25:16	0xc8	HT1 receiver reconnection timer. This timer determines when during HT1ReconCnt, the receiver is enabled before HT1 initialization. It counts on LCLK
All bits in this register are reset on POWERGOOD and not RESET			

Link_State_Control_2 - RW - 32 bits - HTIUNBIND:0x17			
Field Name	**Bits**	**Default**	**Description**
HT1AltCTLInit	0	0x0	Reserved. This register controls no hardware
InfiniteShortRetry	1	0x0	Enables an infinite number of HT3 short retry attempts.
InfiniteLongRetry	2	0x0	Enables an infinite number of HT3 long retry attempts.
ForceHT2AtHT3Freq	3	0x0	Enables HyperTransport 2 behaviour even at HyperTransport 3 frequencies
TmrDlyToTR1	11:4	0xf	Control the number of LCLK the link state controller is delayed before entering the Training 1 state.
TmrExitDisc1usOverride	15	0x0	Allows the timer used to exit the HT3 disconnected state to be overridden.
TmrExitDisc1us	26:16	0x0	Controls the override value for the time used in exiting the HT3 disconnected state. It counts in LCLKs
DisableResetTmr1	27	0x1	
All bits in this register are reset on POWERGOOD and not RESET			

Link_State_Control_3 - RW - 32 bits - HTIUNBIND:0x18			
Field Name	**Bits**	**Default**	**Description**
Tmr200ns	7:0	0x0	Controls the override value for the 200ns timers. It counts in LCLKs.
Tmr0_200us	27:8	0x0	Controls the override value for the 200us timer used by Tmr0. It counts in LCLKs.
Tmr200nsOverride	30	0x0	Allows the 200ns timers used by the ht link state controller to be overridden.
Tmr0_200usOverride	31	0x0	Allows the 200us timer used for Tmr0 to be overridden.
All bits in this register are reset on POWERGOOD and not RESET			

Link_State_Control_4 - RW - 32 bits - HTIUNBIND:0x19			
Field Name	**Bits**	**Default**	**Description**
Tmr1	19:0	0x0	Controls the override value for Tmr1. It counts in LCLKs.
Tmr1Override	31	0x0	Allows Tmr1 to be overridden.
All bits in this register are reset on POWERGOOD and not RESET			

Link_State_Control_5 - RW - 32 bits - HTIUNBIND:0x1A			
Field Name	**Bits**	**Default**	**Description**
Tmr2	19:0	0x0	Controls the override value for Tmr2. It counts in LCLKs.
Tmr2Override	31	0x0	Allows Tmr2 to be overridden.
All bits in this register are reset on POWERGOOD and not RESET			

Link_State_Control_6 - RW - 32 bits - HTIUNBIND:0x1B			
Field Name	**Bits**	**Default**	**Description**
Tmr3	19:0	0x0	Controls the override value for Tmr3. It counts in LCLKs.
Tmr3Override	31	0x0	Allows Tmr3 to be overridden.
All bits in this register are reset on POWERGOOD and not RESET			

Link_State_Control_7 - RW - 32 bits - HTIUNBIND:0x1C			
Field Name	**Bits**	**Default**	**Description**
IdleTmrLimit	15:0	0x0	Controls the initial value of the Idle Timer. It counts in increments of 100ns. This register is cleared on POWERGOOD and not RESET.
IdleTmrEnable	16	0x0	Enables the HT3 Idle Timer. If the Idle Timer is expires during the disconnected state, then a full 200us period is used for training 0. This register is cleared on POWERGOOD and not RESET.
GSMConditionEnable	31:17	0x0	Enables pipeline conditions to detect GSM requests Bit [0]=HT link initialization Bit [1]=ioc_slave P request Bit [2]=ioc_slave NP request Bit [3]=pcie_slave NP request Bit [4]=arb_p request Bit [5]=arb_np request Bit [6]=arb_np isoc request Bit [7]=txl request Bit [8]=lta request Bit [9]=lretry request Bit [10]=txcrc request Bit [11]=htioc_tagxlt tags outstanding

Receiver_Control_0 - RW - 32 bits - HTIUNBIND:0x1D			
Field Name	**Bits**	**Default**	**Description**
T1PhaseLock	0	0x0	Receiver Training 1 Phase Lock. This register is cleared on POWERGOOD and not RESET : 1=HT receiver obtains symbol lock in during Training 1 state. 0=HT receiver obtains symbol lock in during Training 2 state
StrictT2ToT3	1	0x1	Reciever Strict Training 2 to Training 3 Mode. This register is cleared on POWERGOOD and not RESET : 1=HT receiver only transitions from training 2 to training 3 states on a training sequence boundary. 0=HT receiver can transition from training 2 to training 3 in the middle of a training sequence
DataRateMatchDis	2	0x0	Data-rate Matching Disable. This register is cleared on POWERGOOD and not RESET : 1=Disable data-rate matching capabilities in the HT receiver. 0=Enable data-rate matching capabilities in the HT receiver.
HT3ModeAllowAnyInsertion	3	0x0	HT3 Receiver Inserted Command Mode. This register is cleared on POWERGOOD and not RESET : 1=HT receiver can handle only NOP inserted commands in HT3 mode. 0=HT receiver can handle non-NOP non-data inserted commands in HT3 mode.
DisableSyncFloodDetect	4	0x0	Sync Flood Detection Disable. This register is for debugging pruposes. This register is cleared on POWERGOOD and not RESET : 1=HT receiver can detect the sync flood pattern and propagate that state to the transmitter. 0=HT receiver cannot detect the sync flood state.
SaferSyncFlood	5	0x0	Reserved. This register controls no hardware. This register is cleared on POWERGOOD and not RESET

HT3HardDisconnect	6	0x0	HT3 Receiver Hard Disconnect Mode. This register is cleared on POWERGOOD and not RESET : 1=HT receiver shuts off immediately after receiving disconnect NOP. 0=HT receiver stays on after receiving disconnect NOP to look for additional disconnect NOPs.
RxScramblerDisable	7	0x0	Receiver Scrambler Disable. This register is cleared on POWERGOOD and not RESET : 1=HT receiver scrambler is turned off. 0=HT receiver scrambler is controlled by the standard scrambler enable bit.
CRCErrorStorageEn	8	0x0	Enables CRC Error Storage: 1=Enable CRC Error Storage. 1 incorrect CRC is stored for debugging purposes. 0=Disable CRC Error Storage.
CRCErrorStorageMode	9	0x0	CRC Error Storage Mode: 1=Capture last CRC Error. 0=Capture first CRC Error.
CRCErrorStorageClear	10	0x0	CRC Error Storage Clear: 1=Clear CRC Error Storage register. 0=CRC Error Storage register is writable by hardware.
CrcErrorStorageValid (R)	11	0x0	CRC Error Storage Valid: 1=CRC Error Storage contains valid data. 0=CRC Error Storage does not contains valid data..
SEMDecode	12	0x0	SEM Decode: 1=Enable explicit decoding of SEM packets. 0=Use default decoding for SEM packets.
ExtendedSMDecode	13	0x0	Extended System Management Decode: 1=Enable decoding of 12-bit system management packets from the host. 0=Only decode 8-bit system management packets from the host.
ForceBCToSB	14	0x0	Forces Broadcast Packets to Southbridge: 1=All broadcast packets are forced to go to southbridge. 0=Broadcast packet addresses are decoded by IOC.
PMask	31:16	0xffff	Posted FCB Masking. This register is reset on POWERGOOD and requires a warm reset to take effect. All bits that are set to 1 mask off a posted flow-control buffer. This register is used to test reduced hardware configurations.

Receiver_Control_1 - RW - 32 bits - HTIUNBIND:0x1E			
Field Name	**Bits**	**Default**	**Description**
ProtocolDecodeCheckEn	31:0	0x0	[0] Too much data [1] Not enough data [2] Expected 2nd part of a 2DW cmd but got data [3] Expected 2nd part of a 2DW cmd but got CRC [4] Didn't expect data but got Data CRC [5] Got data when no data is expected [6] Missing CRC [7] Invalid command is observed [8] Per-packet CRC is observed while in HT1 mode [9] Received a non-NOP inserted command in HT3 mode [10] Received a non-nop inserted command without using inscmd CTL code in HT3 mode [11] Invalid CRC pattern (two adjacent CRC) [12] Invalid CRC pattern [13] A packet missed CRC check [14] A packet has duplicate CRC checks [15] Retry Flush when Response Error is seen in HTIU Rx [16] PC FCB has no available spot but an outstanding PC is available [17] NC FCB has no available spot but an outstanding NC is available [18] ND FCB has no available spot but an outstanding ND is available [19] RC FCB has no available spot but an outstanding RC is available [20] PC FCB overflow [21] NC FCB overflow [22] ND FCB overflow [23] RC FCB overflow [24] Invalid CTL signal pattern [25] Not in use [26] Exclude downstream Master-Abort or Target-Aboort from Protocol Error (Retry Flush) [27] Not in use [28] Not in use [29] NOt enoguh data (HT1) [30] Clear outstanding NOPs on RetryFlush event [31] Check for any unacknowledged NOP

Receiver_Control_2 - R - 32 bits - HTIUNBIND:0x1F			
Field Name	**Bits**	**Default**	**Description**
CRCErrorStorageExpected	31:0	0x0	

Receiver_Control_3 - R - 32 bits - HTIUNBIND:0x20			
Field Name	**Bits**	**Default**	**Description**
CRCErrorStorageReceived	31:0	0x0	

HT_BIST_Extended_Control_0 - RW - 32 bits - HTIUNBIND:0x21			
Field Name	**Bits**	**Default**	**Description**
ErrCountLaneSel	4:0	0x0	
prbs_enable	5	0x0	
HT1_BIST_MODE	6	0x0	
llmClone_Ctl0	7	0x0	

HT_BIST_Extended_Control_1 - R - 32 bits - HTIUNBIND:0x22			
Field Name	**Bits**	**Default**	**Description**
ErrCountLane	31:0	0x0	

Transmiter_Control_0 - RW - 32 bits - HTIUNBIND:0x23			
Field Name	**Bits**	**Default**	**Description**
TxPipeOkToRd	3:0	0x7	Defines the number of entry seperating the read and write pointer in the Transmit Fifo: (Acceptable values are 1-7. Do not program to 0. Need LDTSTOP/Reset to update the value)
TxScrambleDisable	4	0x0	Disables the Transmit Scrambler: 0=Force Tx Scrambler to be disable 1=Allow Tx Scrambler to be control by HT3 standard register
ZeroReqCrc	5	0x0	Forces a single per packet crc error on a request (the event is edge detect): 0=STOP per packet crc error on a request 1=Trigger per packet crc error on a request
TxTmrOverride	6	0x0	Enables Override for 200ns timer. Change the delay to different value 0=Normal 200ns delay 1=Delay base on TxTmr
Spare (R)	7	0x0	
TxTmr	15:8	0x0	Override Value for the 200ns timer. (LCLK period * TxTmr = New delay)
CheckInvalidSMC	16	0x0	Detects Invalid SMC and transform it to all zero command: 0=Disable checking for invalid SMC, forward all SMC upstream 1=Enable checking for invalid SMC
NopAccumEn	17	0x0	Accumulates Buffer release info in Nop: 0=Disable Nop Buffer release Accumulation (more single buffer release) 1=Enable Nop Buffer release to accumulate over period of 4 LCLK before pushing into the Nop fifo
CrcWrapDisable	18	0x0	NA. Consider as spare
AckDetCnt	22:19	0x0	Wait time before detect changes in RxNextPktToAck and trigger Nop insertion. (Need to set InsertAckNopEn for this counter to take effect)
InsertAckNopEn	23	0x0	Insert Nop base on perodic detection of RxNextPktToAck 0=Normal mode, detect change of RxNextPktToAck every cycle 1=Periodic mode, detect change of RxNextPktToAck base on a counter. (Period is defined by AckDetCnt)

HalfRetryBuf	24	0x0	Half the size of retry buffer (update on reset only): 0=Use full retry buffer (64 entries) 1=Use half retry buffer (32 entries)
WaitForRetryAck	25	0x0	Wait until all the retry request got acknowledged: 0=Do not wait for retry request acknowledge, send other request right after retry buffer is empty 1=Wait for retry request acknowledge, delay sending any new request
TxResetHT1Dis	26	0x0	NA. Consider as spare
TxClkGateEn	27	0x0	Reserved for future use. This register controls no hardware.
TxResetHT3En	28	0x0	Transmitter Reset Control 0 = HT transmitter is not reset when exiting the disconnected state in LS0 or LS1 modes 1 = Force HT transmitter to reset when exiting the disconnected state in LS0 or LS1 modes

Transmitter_Control_1 - RW - 32 bits - HTIUNBIND:0x24			
Field Name	**Bits**	**Default**	**Description**
VC1UrAddrUpper	19:0	0x0	Upper address that invalid VC1 reads are redirected to. This should be programmed to a safe physical memory address.

Transmitter_Control_2 - RW - 32 bits - HTIUNBIND:0x25			
Field Name	**Bits**	**Default**	**Description**
VC1UrAddrLower	31:6	0x0	Lower address that invalid VC1 reads are redirected to. This should be programmed to a safe physical memory address.

HT3PHY_CNTL_1 - RW - 32 bits - HTIUNBIND:0x26			
Field Name	**Bits**	**Default**	**Description**
RX_DATA_DEL_0	1:0	0x0	HT1 receiver low data 0 delay setting
RX_DATA_DEL_1	3:2	0x0	HT1 receiver low data 1 delay setting
RX_DATA_DEL_2	5:4	0x0	HT1 receiver low data 2 delay setting
RX_DATA_DEL_3	7:6	0x0	HT1 receiver low data 3 delay setting
RX_DATA_DEL_4	9:8	0x0	HT1 receiver low data 4 delay setting
RX_DATA_DEL_5	11:10	0x0	HT1 receiver low data 5 delay setting
RX_DATA_DEL_6	13:12	0x0	HT1 receiver low data 6 delay setting
RX_DATA_DEL_7	15:14	0x0	HT1 receiver low data 7 delay setting
RX_DATA_DEL_8	17:16	0x0	HT1 receiver low control delay setting
RX_DATA_DEL_9	19:18	0x0	HT1 receiver high data 0 delay setting
RX_DATA_DEL_10	21:20	0x0	HT1 receiver high data 1 delay setting
RX_DATA_DEL_11	23:22	0x0	HT1 receiver high data 2 delay setting
RX_DATA_DEL_12	25:24	0x0	HT1 receiver high data 3 delay setting
RX_DATA_DEL_13	27:26	0x0	HT1 receiver high data 4 delay setting
RX_DATA_DEL_14	29:28	0x0	HT1 receiver high data 5 delay setting
RX_DATA_DEL_15	31:30	0x0	HT1 receiver high data 6 delay setting

HT3PHY_CNTL_2 - RW - 32 bits - HTIUNBIND:0x27			
Field Name	**Bits**	**Default**	**Description**
RX_DATA_DEL_16	1:0	0x0	HT1 receiver high data 7 delay setting
RX_DATA_DEL_17	3:2	0x0	HT1 receiver high control delay setting
RX_CLK_DEL_0	5:4	0x0	HT1 receiver low clock 0 delay setting
RX_CLK_DEL_1	7:6	0x0	HT1 receiver low clock 1 delay setting
RX_CLK_DEL_2	9:8	0x0	HT1 receiver low clock 2 delay setting
RX_CLK_DEL_3	11:10	0x0	HT1 receiver low clock 3 delay setting
RX_CLK_DEL_4	13:12	0x0	HT1 receiver low clock 4 delay setting
RX_CLK_DEL_5	15:14	0x0	HT1 receiver low clock 5 delay setting
RX_CLK_DEL_6	17:16	0x0	HT1 receiver low clock 6 delay setting
RX_CLK_DEL_7	19:18	0x0	HT1 receiver low clock 7 delay setting
RX_CLK_DEL_8	21:20	0x0	HT1 receiver low clock 8 delay setting
RX_CLK_DEL_9	23:22	0x0	HT1 receiver high clock 0 delay setting
RX_CLK_DEL_10	25:24	0x0	HT1 receiver high clock 1 delay setting
RX_CLK_DEL_11	27:26	0x0	HT1 receiver high clock 2 delay setting
RX_CLK_DEL_12	29:28	0x0	HT1 receiver high clock 3 delay setting
RX_CLK_DEL_13	31:30	0x0	HT1 receiver high clock 4 delay setting

HT3PHY_CNTL_3 - RW - 32 bits - HTIUNBIND:0x28			
Field Name	**Bits**	**Default**	**Description**
RX_CLK_DEL_14	1:0	0x0	HT1 receiver high clock 5 delay setting
RX_CLK_DEL_15	3:2	0x0	HT1 receiver high clock 6 delay setting
RX_CLK_DEL_16	5:4	0x0	HT1 receiver high clock 7 delay setting
RX_CLK_DEL_17	7:6	0x0	HT1 receiver high clock 8 delay setting
OFFSET_C_EN	8	0x0	Enables Rx receiver offset cancelation 1=Enable 0=Disable (default)
RX_CROUT_SEL	9	0x1	CR observability setting for RX_CROUT[6:0] 0: 7-bit clock recovery frequency estimator output 1: 7-bit clock recovery phase counter output
RX_CRFR_ON	10	0x0	0=Clock recovery frequency loop disabled 1=Clock recovery frequency loop enabled
RX_CRFR_BPASS	11	0x0	When asserted, bypasses the clock recovery Freq Estimator output with RX_CRFR[5:0].
RX_CRCTRL_BPASS	12	0x0	When asserted, bypasses the clock recovery Phase Counter output with RX_CRCTRL[6:0]
RX_CRFR	18:13	0x0	Bypass value for the clock recovery Freq Estimator output. Selected by asserting RX_CRFR_BPASS.
RX_CRFRSIZE	20:19	0x1	Clock recovery Freq Filter size.
RX_CRPHSIZE	22:21	0x1	Clock recovery Phase Filter size
RX_CRCTRL	29:23	0x0	Bypass value for the clock recovery Phase Counter output. Selected by asserting RX_CRCTRL_BPASS
RX_CR_ENABLE	30	0x1	Clock recovery (Rx_cdr) enable 0=Clock recovery parameter locked 1=Clock recovery parameter allowed to be updated according to the Rx input.
RX_CR_ENABLE_CNTL	31	0x0	External CR_ENABLE control 0=Core control 1=Register control

HT3PHY_CNTL_4 - RW - 32 bits - HTIUNBIND:0x29			
Field Name	**Bits**	**Default**	**Description**
RX_DLL_bypass	0	0x0	DLL bypass for test mode 0=Normal Operation 1=Bypass DLL
RX_DLL_reset	2:1	0x3	Reset DLL 0=Normal operation 1=Reset
RX_DLL_PWRDN	4:3	0x3	DLL power down 0=Normal operation 1=Power down
RX_DLL_CLKSEL	22:5	0x0	DLL clock inputs selection 0=clk_ina 1=clk_inb
RX_PDNB	24:23	0x3	Receiver power down (active low) 0=Power down 1=Normal operation
RX_DLL_CNTL_EN	25	0x0	External DLL control 0=Core control 1=Register control
TSTCTRL_3	26	0x0	Test control for DLL, bit [3]
PAD_UPDATE_RATE	31:27	0x3	Calibration pad update interval

HT3PHY_CNTL_5 - RW - 32 bits - HTIUNBIND:0x2A			
Field Name	**Bits**	**Default**	**Description**
CORE_TX_DRV_STR	1:0	0x0	Drive strength
TX_CLKL_PDWN	2	0x0	Powers down the low clock buffers 0=Disable 1=Enable
TX_CLKH_PDWN	3	0x0	Powers down the high clock buffers 0=Disable 1=Enabled
TX_CLKL_TXGNDTRM_EN	4	0x0	Special HT3 power mode 0=Disable 1=Enabled
TX_CLKH_TXGNDTRM_EN	5	0x0	Special HT3 power mode 0=Disable 1=Enable
CORE_TX_POWERDOWN_EN	23:6	0x0	Powers down is used to disable a bit 0=Active 1=Powered down
TSTCTRL_2_0	26:24	0x7	Test control for DLL, bits [2:0]
PAD_SAMPLE_DELAY	31:27	0x2	Delay in between samples for calibration

HT3PHY_CNTL_6 - RW - 32 bits - HTIUNBIND:0x2B			
Field Name	**Bits**	**Default**	**Description**
CORE_TX_TXGNDTRM_EN	17:0	0x0	Disables termination and pull down on both sides of the driver 0=Active 1=Disable
PAD_INC_THRESHOLD	22:18	0x8	Upper limit for calibration threshold
PAD_DEC_THRESHOLD	27:23	0x6	Lower limit for calibration threshold

TX_BIAS_3_0	31:28	0x0	BIAS control for transmitter, enable the bias circuits in every bit as follows TX_BIAS_3: bits 3, 7, 11, 15 TX_BIAS_2: bits 1, 5, 9, 13 TX_BIAS_1: bits 0, 4, 8, 12 TX_BIAS_0: bits CLKH, CLKL, CTLH, CTLL Bias circuits for bits 2, 6, 10, 14 are always enabled.

CFG_HT_DIV_CTRL - RW - 32 bits - HTIUNBIND:0x2C			
Field Name	**Bits**	**Default**	**Description**
CFG_HT_FBDIV	6:0	0x0	HTPLL feedback divider override value
CFG_HT_FBDIV_EN	7	0x0	HTPLL feedback divider override enable
CFG_HT_REFDIV	9:8	0x0	HTPLL reference divider override value
CFG_HT_REFDIV_EN	11	0x0	HTPLL reference divider override enable
CFG_HT_CORECLK_DIV	13:12	0x0	HTPLL core clock post divider override value
CFG_HT_CORECLK_DIV_EN	15	0x0	HTPLL core clock post divider override enable

HTIU_IOMMU_CONTROL_0 - RW - 32 bits - HTIUNBIND:0x2E			
Field Name	**Bits**	**Default**	**Description**
IOMMUUrAddrUpper	19:0	0x0	Lower address that invalid IOMMU reads are redirected to. This should be programmed to a safe physical memory address.

HTIU_IOMMU_CONTROL_1 - RW - 32 bits - HTIUNBIND:0x2F			
Field Name	**Bits**	**Default**	**Description**
IOMMUUrAddrLower	31:6	0x0	Upper address that invalid IOMMU reads are redirected to. This should be programmed to a safe physical memory address.

NB_LOWER_TOP_OF_DRAM2 - RW - 32 bits - HTIUNBIND:0x30			
Field Name	**Bits**	**Default**	**Description**
ENABLE	0	0x0	Enable decoding of memory space between 4GB up to TOM2. TOM2 defines the top of physical memory between 4GB and 1TB. All addresses below TOM2 (i.e. TOM2 itself is not a physical memory address) and above 4GB are considered to be part of physical memory.
LOWER_TOM2	31:23	0x0	This register defines the lower address bits of TOM2
Top of lower Extended RAM			

NB_UPPER_TOP_OF_DRAM2 - RW - 32 bits - HTIUNBIND:0x31			
Field Name	**Bits**	**Default**	**Description**
UPPER_TOM2	7:0	0x0	This register defines the upper address bits of TOM2
Top of upper Extended RAM			

NB_HTIU_CFG - RW - 32 bits - HTIUNBIND:0x32			
Field Name	**Bits**	**Default**	**Description**
spare_27_0	27:0	0x0	Reserved for future use. This register controls no hardware
NB_BAR3_PCIEXP_ENABLE	28	0x0	Enables decoding of memory-mapped BAR3 for accessing extended PCI configuration space registers. 0=Disable 1=Enable
spare_30_29	30:29	0x0	Reserved for future use. this register controls no hardware
HT_CTL1_FREEZE	31	0x1	Keeps CTL[1] bit always high 0=Disable 1=Enable

HT3PHY_CNTL_15 - RW - 32 bits - HTIUNBIND:0x33			
Field Name	**Bits**	**Default**	**Description**
RxCRPhaseReadback (R)	7:0	0x0	
RxCRPhaseSel	20:16	0x0	

HTIU_TAG_XTL_CONTROL_0 - RW - 32 bits - HTIUNBIND:0x38			
Field Name	**Bits**	**Default**	**Description**
IOMMUBaseOutstandingMask	31:0	0x0	

HTIU_TAG_XTL_CONTROL_1 - RW - 32 bits - HTIUNBIND:0x39			
Field Name	**Bits**	**Default**	**Description**
IOMMUIsocOutstandingMask	31:0	0x0	Each bit in this register masks out a tag used by IOMMU isoc channel reads. This can be used to reduce the number of outstanding isoc channel reads from IOMMU issued over the HyperTransport link.

HTIU_PCIE_ERR_FLOOD_CONTROL_0 - RW - 32 bits - HTIUNBIND:0x3A			
Field Name	**Bits**	**Default**	**Description**
Bridge2FatalFloodEn	2	0x0	Enables fatal errors detected by bridge 2 to trigger a HyperTransport™ syncflood
Bridge3FatalFloodEn	3	0x0	Enables fatal errors detected by bridge 3 to trigger a HyperTransport syncflood
Bridge4FatalFloodEn	4	0x0	Enables fatal errors detected by bridge 4 to trigger a HyperTransport syncflood
Bridge5FatalFloodEn	5	0x0	Enables fatal errors detected by bridge 5 to trigger a HyperTransport syncflood
Bridge6FatalFloodEn	6	0x0	Enables fatal errors detected by bridge 6 to trigger a HyperTransport syncflood
Bridge7FatalFloodEn	7	0x0	Enables fatal errors detected by bridge 7 to trigger a HyperTransport syncflood
Bridge8FatalFloodEn	8	0x0	Enables fatal errors detected by bridge 8 to trigger a HyperTransport syncflood

Bridge9FatalFloodEn	9	0x0	Enables fatal errors detected by bridge 9 to trigger a HyperTransport syncflood
Bridge10FatalFloodEn	10	0x0	Enables fatal errors detected by bridge 10 to trigger a HyperTransport syncflood
Bridge11FatalFloodEn	11	0x0	Enables fatal errors detected by bridge 11 to trigger a HyperTransport syncflood
Bridge12FatalFloodEn	12	0x0	Enables fatal errors detected by bridge 12 to trigger a HyperTransport syncflood
Bridge13FatalFloodEn	13	0x0	Enables fatal errors detected by bridge 13 to trigger a HyperTransport syncflood

HTIU_PCIE_ERR_FLOOD_CONTROL_1 - RW - 32 bits - HTIUNBIND:0x3B			
Field Name	**Bits**	**Default**	**Description**
Bridge2NonFatalFloodEn	2	0x0	Enables non-fatal errors detected by bridge 2 to trigger a HyperTransport syncflood
Bridge3NonFatalFloodEn	3	0x0	Enables non-fatal errors detected by bridge 3 to trigger a HyperTransport syncflood
Bridge4NonFatalFloodEn	4	0x0	Enables non-fatal errors detected by bridge 4 to trigger a HyperTransport syncflood
Bridge5NonFatalFloodEn	5	0x0	Enables non-fatal errors detected by bridge 5 to trigger a HyperTransport syncflood
Bridge6NonFatalFloodEn	6	0x0	Enables non-fatal errors detected by bridge 6 to trigger a HyperTransport syncflood
Bridge7NonFatalFloodEn	7	0x0	Enables non-fatal errors detected by bridge 7 to trigger a HyperTransport syncflood
Bridge8NonFatalFloodEn	8	0x0	Enables non-fatal errors detected by bridge 8 to trigger a HyperTransport syncflood
Bridge9NonFatalFloodEn	9	0x0	Enables non-fatal errors detected by bridge 9 to trigger a HyperTransport syncflood
Bridge10NonFatalFloodEn	10	0x0	Enables non-fatal errors detected by bridge 10 to trigger a HyperTransport syncflood
Bridge11NonFatalFloodEn	11	0x0	Enables non-fatal errors detected by bridge 11 to trigger a HyperTransport syncflood
Bridge12NonFatalFloodEn	12	0x0	Enables non-fatal errors detected by bridge 12 to trigger a HyperTransport syncflood
Bridge13NonFatalFloodEn	13	0x0	Enables non-fatal errors detected by bridge 13 to trigger a HyperTransport syncflood

LS_History0 - R - 32 bits - HTIUNBIND:0x40			
Field Name	**Bits**	**Default**	**Description**
LS_History0	31:0	0x0	[5:0]=Current HT Link State [11:6]=Previous HT Link State 1 [17:12]=Previous HT Link State 2 [23:18]=Previous HT Link State 3 [29:24]=Previous HT Link State 4 [31:30]=Previous HT Link State 5

LS_History1 - R - 32 bits - HTIUNBIND:0x41			
Field Name	**Bits**	**Default**	**Description**
LS_History1	31:0	0x0	[3:0]=Previous HT Link State 5 [9:4]=Previous HT Link State 6 [15:10]=Previous HT Link State 7 [21:16]=Previous HT Link State 8 [27:22]=Previous HT Link State 9 [31:28]=Previous HT Link State 10

LS_History2 - R - 32 bits - HTIUNBIND:0x42			
Field Name	**Bits**	**Default**	**Description**
LS_History2	31:0	0x0	[1:0]=Previous HT Link State 10 [7:2]=Previous HT Link State 11 [13:8]=Previous HT Link State 12 [19:14]=Previous HT Link State 13 [25:20]=Previous HT Link State 14 [31:26]=Previous HT Link State 15

LS_History3 - R - 32 bits - HTIUNBIND:0x43			
Field Name	**Bits**	**Default**	**Description**
LS_History3	31:0	0x0	[5:0]=Previous HT Link State 16 [11:6]=Previous HT Link State 17 [17:12]=Previous HT Link State 18 [23:18]=Previous HT Link State 19 [29:24]=Previous HT Link State 20 [31:30]=Previous HT Link State 21

LS_History4 - R - 32 bits - HTIUNBIND:0x44			
Field Name	**Bits**	**Default**	**Description**
LS_History4	31:0	0x0	[3:0]=Previous HT Link State 21 [9:4]=Previous HT Link State 22 [15:10]=Previous HT Link State 23 [21:16]=Previous HT Link State 24 [27:22]=Previous HT Link State 25 [31:28]=Previous HT Link State 26

LS_History5 - R - 32 bits - HTIUNBIND:0x45			
Field Name	**Bits**	**Default**	**Description**
LS_History5	31:0	0x0	[1:0]=Previous HT Link State 26 [7:2]=Previous HT Link State 27 [13:8]=Previous HT Link State 28 [19:14]=Previous HT Link State 29 [25:20]=Previous HT Link State 30 [31:26]=Previous HT Link State 31

TX_B_P90PLL_IBias - RW - 32 bits - HTIUNBIND:0x46			
Field Name	**Bits**	**Default**	**Description**
P90PLL_IBias	9:0	0x54	Reserved for future use. This register controls no hardware

HT3PHY_CNTL_8 - RW - 32 bits - HTIUNBIND:0x47			
Field Name	**Bits**	**Default**	**Description**
RX_CRCTRL_1	6:0	0x0	Bypass value for the clock recovery Phase Counter output., bit 1. Selected by asserting RX_CRCTRL_BPASS
RX_CRCTRL_1_EN	7	0x0	Local phase code bypass for CAD1
RX_CRCTRL_2	14:8	0x0	Bypass value for the clock recovery Phase Counter output., bit 2. Selected by asserting RX_CRCTRL_BPASS
RX_CRCTRL_2_EN	15	0x0	Local phase code bypass for CAD2
RX_CRCTRL_3	22:16	0x0	Bypass value for the clock recovery Phase Counter output., bit 3. Selected by asserting RX_CRCTRL_BPASS
RX_CRCTRL_3_EN	23	0x0	Local phase code bypass for CAD3
RX_CRCTRL_4	30:24	0x0	Bypass value for the clock recovery Phase Counter output., bit 4. Selected by asserting RX_CRCTRL_BPASS
RX_CRCTRL_4_EN	31	0x0	Local phase code bypass for CAD4

HT3PHY_CNTL_9 - RW - 32 bits - HTIUNBIND:0x48			
Field Name	**Bits**	**Default**	**Description**
RX_CRCTRL_5	6:0	0x0	Bypass value for the clock recovery Phase Counter output., bit 5. Selected by asserting RX_CRCTRL_BPASS
RX_CRCTRL_5_EN	7	0x0	Local phase code bypass for CAD5
RX_CRCTRL_6	14:8	0x0	Bypass value for the clock recovery Phase Counter output., bit 6. Selected by asserting RX_CRCTRL_BPASS
RX_CRCTRL_6_EN	15	0x0	Local phase code bypass for CAD6
RX_CRCTRL_7	22:16	0x0	Bypass value for the clock recovery Phase Counter output., bit 7. Selected by asserting RX_CRCTRL_BPASS
RX_CRCTRL_7_EN	23	0x0	Local phase code bypass for CAD7
RX_CRCTRL_CTLL	30:24	0x0	Bypass value for the clock recovery Phase Counter output., low ctl. Selected by asserting RX_CRCTRL_BPASS
RX_CRCTRL_CTLL_EN	31	0x0	Local phase code bypass for CTL0

HT3PHY_CNTL_10 - RW - 32 bits - HTIUNBIND:0x49			
Field Name	**Bits**	**Default**	**Description**
RX_CRCTRL_8	6:0	0x0	Bypass value for the clock recovery Phase Counter output., bit 8. Selected by asserting RX_CRCTRL_BPASS
RX_CRCTRL_8_EN	7	0x0	Local phase code bypass for CAD8
RX_CRCTRL_9	14:8	0x0	Bypass value for the clock recovery Phase Counter output., bit 9. Selected by asserting RX_CRCTRL_BPASS
RX_CRCTRL_9_EN	15	0x0	Local phase code bypass for CAD9
RX_CRCTRL_10	22:16	0x0	Bypass value for the clock recovery Phase Counter output., bit 10. Selected by asserting RX_CRCTRL_BPASS
RX_CRCTRL_10_EN	23	0x0	Local phase code bypass for CAD10
RX_CRCTRL_11	30:24	0x0	Bypass value for the clock recovery Phase Counter output., bit 11. Selected by asserting RX_CRCTRL_BPASS
RX_CRCTRL_11_EN	31	0x0	Local phase code bypass for CAD11

HT3PHY_CNTL_11 - RW - 32 bits - HTIUNBIND:0x4A			
Field Name	**Bits**	**Default**	**Description**
RX_CRCTRL_12	6:0	0x0	Bypass value for the clock recovery Phase Counter output., bit 12. Selected by asserting RX_CRCTRL_BPASS
RX_CRCTRL_12_EN	7	0x0	Local phase code bypass for CAD12
RX_CRCTRL_13	14:8	0x0	Bypass value for the clock recovery Phase Counter output., bit 13. Selected by asserting RX_CRCTRL_BPASS
RX_CRCTRL_13_EN	15	0x0	Local phase code bypass for CAD13
RX_CRCTRL_14	22:16	0x0	Bypass value for the clock recovery Phase Counter output., bit 14. Selected by asserting RX_CRCTRL_BPASS
RX_CRCTRL_14_EN	23	0x0	Local phase code bypass for CAD14
RX_CRCTRL_15	30:24	0x0	Bypass value for the clock recovery Phase Counter output., bit 15. Selected by asserting RX_CRCTRL_BPASS
RX_CRCTRL_15_EN	31	0x0	Local phase code bypass for CAD15

HT3PHY_CNTL_12 - RW - 32 bits - HTIUNBIND:0x4B			
Field Name	**Bits**	**Default**	**Description**
RX_CRCTRL_CTLH	6:0	0x0	Bypass value for the clock recovery Phase Counter output., high ctl. Selected by asserting RX_CRCTRL_BPASS
RX_CRCTRL_CTLH_EN	7	0x0	Local phase code bypass for CTL1
TX_CLK_RESET_EN_LOW_B	8	0x0	Control of reset going to low clock pad: 0: clock pad sees tx_reset; 1: clock pad has the tx_reset blocked
TX_CLK_RESET_EN_HIGH_B	9	0x0	Control of reset going to high clock pad:0: clock pad sees tx_reset; 1: clock pad has the tx_reset blocked
RSVD17	31:10	0x0	Reserved for future use. This register controls no hardware

HT3PHY_CNTL_13 - RW - 32 bits - HTIUNBIND:0x4C			
Field Name	**Bits**	**Default**	**Description**
RCV_EQ_LOW	10:8	0x0	Receiver equalization setting for HT CAD[7:0] and CTL[0]. This register requires a warm reset or LDTSTOP to take effect
LowerClockInvert	12	0x0	When set, this register inverts the polarity of the lower transmitted HyperTransport clock. This register requires a warm reset or LDTSTOP to take effect

UpperClockInvert	13	0x0	When set, this register inverts the polarity of the upper transmitted HyperTransport clock. This register requires a warm reset or LDTSTOP to take effect
RX2TX_LOOPBACK_CNTRL	17:16	0x0	Enable receiver to transmitter internal PHY loopback on CTL[1:0]. This register requires a warm reset or LDTSTOP to take effect
RCV_EQ_HIGH	22:20	0x0	Receiver equalization setting for upper HT CAD[15:8] and CTL[1]. This register requires a warm reset or LDTSTOP to take effect
UpperDL1	27:24	0x0	Transmitter deemphasis for HT CAD[15:8] and CTL[1]. This register requires a warm reset or LDTSTOP to take effect
HT3ClockCenterLow	29	0x0	Enable the lower HT clock to transition in the center of the CAD/CTL data eye instead of at the same time as CAD/CTL. This register requires a warm reset or LDTSTOP to take effect
HT3ClockCenterHigh	30	0x0	Enable the upper HT clock to transition in the center of the CAD/CTL data eye instead of at the same time as CAD/CTL. This register requires a warm reset or LDTSTOP to take effect
SplitDeemphEn	31	0x0	Split HT transmitter deephmasis control and use UpperDL1 for HT CAD[15:8] and CTL[1]. This register requires a warm reset or LDTSTOP to take effect

HT3PHY_CNTL_14 - RW - 32 bits - HTIUNBIND:0x4D			
Field Name	**Bits**	**Default**	**Description**
SettlingTime	15:0	0x0	Controls the settling time for receiver time margining
DwellTime	31:16	0x0	Controls the dwell time for receiver time margining

HT3PHY_CNTL_15 - RW - 32 bits - HTIUNBIND:0x33			
Field Name	**Bits**	**Default**	**Description**
RxCRPhaseReadback (R)	7:0	0x0	Read back the receiver sampling phase code for the lane selected by RxCRPhaseSel
RxCRPhaseSel	20:16	0x0	Select the HT receive lane for RxCRPhaseReadback
NegativeTMIndex	31:28	0x0	Sets the amount of receiver time margining in the negative direction

SCRATCH_4 - RW - 32 bits - HTIUNBIND:0x50			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_4	31:0	0x0	All bits in this register can be written to, and read from, but it does not control anything.
SCRATCH_4			

SCRATCH_5 - RW - 32 bits - HTIUNBIND:0x51			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_5	31:0	0x0	All bits in this register can be written to, and read from, but it does not control anything.
SCRATCH_5			

SCRATCH_6 - RW - 32 bits - HTIUNBIND:0x52			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_6	31:0	0x0	All bits in this register can be written to, and read from, but it does not control anything.
SCRATCH_6			

SCRATCH_7 - RW - 32 bits - HTIUNBIND:0x53			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_7	31:0	0x0	All bits in this register can be written to, and read from, but it does not control anything.
SCRATCH_7			

SCRATCH_8 - RW - 32 bits - HTIUNBIND:0x54			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_8	31:0	0x0	All bits in this register can be written to, and read from, but it does not control anything.
SCRATCH_8			

SCRATCH_9 - RW - 32 bits - HTIUNBIND:0x55			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_9	31:0	0x0	All bits in this register can be written to, and read from, but it does not control anything.
SCRATCH_9			

SCRATCH_A - RW - 32 bits - HTIUNBIND:0x56			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_A	31:0	0x0	All bits in this register can be written to, and read from, but it does not control anything.
SCRATCH_A			

HTIU_UPSTREAM_ARB_CONTROL_8 - RW - 32 bits - HTIUNBIND:0x77			
Field Name	**Bits**	**Default**	**Description**
ForceNonZeroSeqID	31:0	0x0	Each bit in this register forces DMA requests from the corresponding UnitID to be issued with SeqID = UnitID. This register is intended for debug purposes only.

HTIU_ILA_CONTROL_0 - RW - 32 bits - HTIUNBIND:0x78			
Field Name	**Bits**	**Default**	**Description**
HTIU_ILA_CONTROL_0	31:0	0x0	Reserved for future use. This register controls no hardware

HTIU_ILA_CONTROL_1 - RW - 32 bits - HTIUNBIND:0x79			
Field Name	**Bits**	**Default**	**Description**
HTIU_ILA_CONTROL_1	31:0	0x0	Reserved for future use. This register controls no hardware

HTIU_ILA_CONTROL_2 - RW - 32 bits - HTIUNBIND:0x7A			
Field Name	**Bits**	**Default**	**Description**
HTIU_ILA_CONTROL_2	31:0	0x0	Reserved for future use. This register controls no hardware

HTIU_ILA_CONTROL_3 - RW - 32 bits - HTIUNBIND:0x7B			
Field Name	**Bits**	**Default**	**Description**
HTIU_ILA_CONTROL_3	31:0	0x0	Reserved for future use. This register controls no hardware

HTIU_ILA_CONTROL_4 - RW - 32 bits - HTIUNBIND:0x7C			
Field Name	**Bits**	**Default**	**Description**
HTIU_ILA_CONTROL_4	31:0	0x0	Reserved for future use. This register controls no hardware

HTIU_ILA_CONTROL_5 - RW - 32 bits - HTIUNBIND:0x7D			
Field Name	**Bits**	**Default**	**Description**
HTIU_ILA_CONTROL_5	31:0	0x0	Reserved for future use. This register controls no hardware

HT_ERROR_INJECTION_CNTL - RW - 32 bits - HTIUNBIND:0x7E			
Field Name	**Bits**	**Default**	**Description**
InjectHTProtocolErr	0	0x0	When set, this register forces the HT protocol error status bit to be set. This is done to help test error handling software
InjectHTResponseErr	1	0x0	When set, this register forces the HT response error status bit to be set. This is done to help test error handling software
InjectHTOverflowErr	2	0x0	When set, this register forces the HT overflow error status bit to be set. This is done to help test error handling software
InjectHTCrcErr	3	0x0	When set, this register forces the HT crc error status bit to be set. This is done to help test error handling software
InjectHTRetryErr	4	0x0	When set, this register forces the HT retry error status bit to be set. This is done to help test error handling software
InjectHTCountRolloverErr	5	0x0	When set, this register forces the HT retry counter rollover error status bit to be set. This is done to help test error handling software
SyncFloodInputPinEn	6	0x0	Enables DFT_GPIO5 to act as an input pin that can trigger a HyperTransport syncflood
SyncFloodInputPinStatus	7	0x0	This register is set by hardware to indicate that an external source has triggered a syncflood through the syncflood pin. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_INJECTION_CNTL - RW - 32 bits - HTIUNBIND:0x80			
Field Name	**Bits**	**Default**	**Description**
PerrGenBlockSel	7:0	0x0	Selects a block for parity error injection 0x0 = HTIU 0x1 = IOC 0x2 = MCU 0x3 = PCIE GPP1 0x4 = PCIE GPP2 0x5 = PCIE GPP3a 0x6 = PCIE GPP3b 0x7 = PCIE SB 0x8 = IOMMU L1 GPP1 0x9 = IOMMU L1 GPP2 0xA = IOMMU L1 GPP3a 0xB = IOMMU L1 GPP3b 0xC = IOMMU L1 SB 0xD = IOMMU L1 SB VC1 0xE = IOMMU L2 0xF = IOMMU L1 GPP1 Cache 0x10 = IOMMU L1 GPP2 Cache 0x11 = IOMMU L1 GPP3a Cache 0x12 = IOMMU L1 GPP3b Cache 0x13 = IOMMU L1 SB Cache 0x14 = IOMMU L1 SB VC1 Cache 0x15 = IOMMU L2B Cache 0x16 = IOMMU L2A Cache All other encodings reserved
PerrGenMacroSel	23:16	0x0	Selects a memory within the block chosen by PerrGenBlockSel for parity error injection
PerrGenInjectWrErr	30	0x0	Injects a parity error on the write side of the target memory. Hardware must exercise the memory using a normal operation to inject the error
PerrGenInjectRdErr	31	0x0	Injects a parity error on the read side of the target memory. Hardware must exercise the memory using a normal operation to inject the error

PARITY_ERROR_STATUS_0 - RW - 32 bits - HTIUNBIND:0x81			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected0	31:0	0x0	Parity error status for HTIU. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_STATUS_1 - RW - 32 bits - HTIUNBIND:0x82			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected1	31:0	0x0	Reserved for future use. This register controls no hardware

PARITY_ERROR_STATUS_2 - RW - 32 bits - HTIUNBIND:0x83			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected2	31:0	0x0	Parity error status for MCU. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_STATUS_3 - RW - 32 bits - HTIUNBIND:0x84			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected3	31:0	0x0	Parity error status for PCIE GPP1. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_STATUS_4 - RW - 32 bits - HTIUNBIND:0x85			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected4	31:0	0x0	Parity error status for PCIE GPP2. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_STATUS_5 - RW - 32 bits - HTIUNBIND:0x86			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected5	31:0	0x0	Parity error status for PCIE GPP3a. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_STATUS_6 - RW - 32 bits - HTIUNBIND:0x87			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected6	31:0	0x0	Parity error status for PCIE GPP3b. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_STATUS_7 - RW - 32 bits - HTIUNBIND:0x88			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected7	31:0	0x0	Parity error status for PCIE SB. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_STATUS_8 - RW - 32 bits - HTIUNBIND:0x89			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected8	31:0	0x0	Parity error status for IOMMU L1 GPP1. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_STATUS_9 - RW - 32 bits - HTIUNBIND:0x8A			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected9	31:0	0x0	Parity error status for IOMMU L1 GPP2. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_STATUS_10 - RW - 32 bits - HTIUNBIND:0x8B			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected10	31:0	0x0	Parity error status for IOMMU L1 GPP3a. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_STATUS_11 - RW - 32 bits - HTIUNBIND:0x8C			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected11	31:0	0x0	Parity error status for IOMMU L1 GPP3b. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_STATUS_12 - RW - 32 bits - HTIUNBIND:0x8D			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected12	31:0	0x0	Parity error status for IOMMU L1 SB. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_STATUS_13 - RW - 32 bits - HTIUNBIND:0x8E			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected13	31:0	0x0	Reserved for future use. This register controls no hardware

PARITY_ERROR_STATUS_14 - RW - 32 bits - HTIUNBIND:0x8F			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected14	31:0	0x0	Reserved for future use. This register controls no hardware

PARITY_ERROR_STATUS_15 - RW - 32 bits - HTIUNBIND:0x90			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected15	31:0	0x0	Parity error status for IOMMU L1 GPP1 cache. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_STATUS_16 - RW - 32 bits - HTIUNBIND:0x91			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected16	31:0	0x0	Parity error status for IOMMU L1 GPP2 cache. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_STATUS_17 - RW - 32 bits - HTIUNBIND:0x92			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected17	31:0	0x0	Parity error status for IOMMU L1 GPP3a cache. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_STATUS_18 - RW - 32 bits - HTIUNBIND:0x93			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected18	31:0	0x0	Parity error status for IOMMU L1 GPP3b cache. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_STATUS_19 - RW - 32 bits - HTIUNBIND:0x94			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected19	31:0	0x0	Parity error status for IOMMU L1 SB cache. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_STATUS_20 - RW - 32 bits - HTIUNBIND:0x95			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected20	31:0	0x0	Reserved for future use. This register controls no hardware

PARITY_ERROR_STATUS_21 - RW - 32 bits - HTIUNBIND:0x96			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected21	31:0	0x0	Parity error status for IOMMU L2B cache. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_STATUS_22 - RW - 32 bits - HTIUNBIND:0x97			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected22	31:0	0x0	Parity error status for IOMMU L2A cache. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_STATUS_23 - RW - 32 bits - HTIUNBIND:0x98			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected23	31:0	0x0	Parity error status for IOMMU L2A cache. This register's state is preserved across a warm reset. Write 1 to clear.

PARITY_ERROR_STATUS_24 - RW - 32 bits - HTIUNBIND:0x99			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected24	31:0	0x0	Reserved for future use. This register controls no hardware

PARITY_ERROR_STATUS_25 - RW - 32 bits - HTIUNBIND:0x9A			
Field Name	**Bits**	**Default**	**Description**
ParityErrorDetected25	31:0	0x0	Reserved for future use. This register controls no hardware

GPIO_1_4 - RW - 32 bits - HTIUNBIND:0xA4			
Field Name	**Bits**	**Default**	**Description**
GPIO1_OE	0	0x0	Output enable control for the PWM_GPIO1 pad when GPIO1_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO1_A	1	0x0	Output value for PWM_GPIO1 pad when GPIO1_OR is set
GPIO1_OR	2	0x0	When set, converts the PWM_GPIO1 pad to a software controllable GPIO pad
GPIO1_PU	3	0x1	Weak pull up control for the PWM_GPIO1 pad when GPIO1_OR is set 1 - Weak pull up disabled 0 - Weak pull up enabled
GPIO1_PD	4	0x0	Weak pull down control for the PWM_GPIO1 pad when GPIO1_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled
GPIO1_SCHMEN	5	0x1	Schmidt trigger enable control for the PWM_GPIO1 pad receiver when GPIO1_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO1_Y (R)	6	0x0	Input value sampled by PWM_GPIO1
GPIO2_OE	8	0x0	Output enable control for the PWM_GPIO2 pad when GPIO2_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO2_A	9	0x0	Output value for PWM_GPIO2 pad when GPIO2_OR is set
GPIO2_OR	10	0x0	When set, converts the PWM_GPIO2 pad to a software controllable GPIO pad
GPIO2_PU	11	0x1	Weak pull up control for the PWM_GPIO2 pad when GPIO2_OR is set 1 - Weak pull up disabled 0 - Weak pull up enabled

GPIO2_PD	12	0x0	Weak pull down control for the PWM_GPIO2 pad when GPIO2_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled
GPIO2_SCHMEN	13	0x1	Schmidt trigger enable control for the PWM_GPIO2 pad receiver when GPIO2_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO2_Y (R)	14	0x0	Input value sampled by PWM_GPIO2
GPIO3_OE	16	0x0	Output enable control for the PWM_GPIO3 pad when GPIO3_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO3_A	17	0x0	Output value for PWM_GPIO3 pad when GPIO3_OR is set
GPIO3_OR	18	0x0	When set, converts the PWM_GPIO3 pad to a software controllable GPIO pad
GPIO3_PU	19	0x1	Weak pull up control for the PWM_GPIO3 pad when GPIO3_OR is set 1 - Weak pull up disabled 0 - Weak pull up enabled
GPIO3_PD	20	0x0	Weak pull down control for the PWM_GPIO3 pad when GPIO3_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled
GPIO3_SCHMEN	21	0x1	Schmidt trigger enable control for the PWM_GPIO3 pad receiver when GPIO3_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO3_Y (R)	22	0x0	Input value sampled by PWM_GPIO3
GPIO4_OE	24	0x0	Output enable control for the PWM_GPIO4 pad when GPIO4_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO4_A	25	0x0	Output value for PWM_GPIO4 pad when GPIO4_OR is set
GPIO4_OR	26	0x0	When set, converts the PWM_GPIO4 pad to a software controllable GPIO pad
GPIO4_PU	27	0x1	Weak pull up control for the PWM_GPIO4 pad when GPIO4_OR is set 1 - Weak pull up disabled 0 - Weak pull up enabled
GPIO4_PD	28	0x0	Weak pull down control for the PWM_GPIO4 pad when GPIO4_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled
GPIO4_SCHMEN	29	0x1	Schmidt trigger enable control for the PWM_GPIO4 pad receiver when GPIO4_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO4_Y (R)	30	0x0	Input value sampled by PWM_GPIO4
GPIO_PWM_GPIO1_4			

GPIO_5_8 - RW - 32 bits - HTIUNBIND:0xA5			
Field Name	**Bits**	**Default**	**Description**
GPIO5_OE	0	0x0	Output enable control for the PWM_GPIO5 pad when GPIO5_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO5_A	1	0x0	Output value for PWM_GPIO5 pad when GPIO5_OR is set

GPIO5_OR	2	0x0	When set, converts the PWM_GPIO5 pad to a software controllable GPIO pad
GPIO5_PU	3	0x1	Weak pull up control for the PWM_GPIO5 pad when GPIO5_OR is set 1 - Weak pull up disabled 0 - Weak pull up enabled
GPIO5_PD	4	0x0	Weak pull down control for the PWM_GPIO5 pad when GPIO5_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled
GPIO5_SCHMEN	5	0x1	Schmidt trigger enable control for the PWM_GPIO5 pad receiver when GPIO5_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO5_Y (R)	6	0x0	Input value sampled by PWM_GPIO5
GPIO6_OE	8	0x0	Output enable control for the PWM_GPIO6 pad when GPIO6_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO6_A	9	0x0	Output value for PWM_GPIO6 pad when GPIO6_OR is set
GPIO6_OR	10	0x0	When set, converts the PWM_GPIO6 pad to a software controllable GPIO pad
GPIO6_PU	11	0x1	Weak pull up control for the PWM_GPIO6 pad when GPIO6_OR is set 1 - Weak pull up disabled 0 - Weak pull up enabled
GPIO6_PD	12	0x0	Weak pull down control for the PWM_GPIO6 pad when GPIO6_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled
GPIO6_SCHMEN	13	0x1	Schmidt trigger enable control for the PWM_GPIO6 pad receiver when GPIO6_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO6_Y (R)	14	0x0	Input value sampled by PWM_GPIO6
GPIO7_OE	16	0x0	Output enable control for the DFT_GPIO0 pad when GPIO7_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO7_A	17	0x0	Output value for DFT_GPIO0 pad when GPIO7_OR is set
GPIO7_OR	18	0x0	When set, converts the DFT_GPIO0 pad to a software controllable GPIO pad
GPIO7_PU	19	0x1	GPIO_DFT_GPIO0_PU
GPIO7_PD	20	0x0	Weak pull down control for the DFT_GPIO0 pad when GPIO7_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled
GPIO7_SCHMEN	21	0x1	Schmidt trigger enable control for the DFT_GPIO0 pad receiver when GPIO7_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO7_Y (R)	22	0x0	Input value sampled by DFT_GPIO0
GPIO8_OE	24	0x0	Output enable control for the DFT_GPIO1 pad when GPIO8_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO8_A	25	0x0	Output value for DFT_GPIO1 pad when GPIO8_OR is set
GPIO8_OR	26	0x0	When set, converts the DFT_GPIO1 pad to a software controllable GPIO pad

GPIO8_PU	27	0x1	Weak pull up control for the DFT_GPIO1 pad when GPIO8_OR is set 1 - Weak pull up disabled 0 - Weak pull up enabled
GPIO8_PD	28	0x0	Weak pull down control for the DFT_GPIO1 pad when GPIO8_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled
GPIO8_SCHMEN	29	0x1	Schmidt trigger enable control for the DFT_GPIO1 pad receiver when GPIO8_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO8_Y (R)	30	0x0	Input value sampled by DFT_GPIO1
GPIO_PWM_GPIO5_6_DFT_0_1			

GPIO_9_12 - RW - 32 bits - HTIUNBIND:0xA6			
Field Name	**Bits**	**Default**	**Description**
GPIO9_OE	0	0x0	Output enable control for the DFT_GPIO2 pad when GPIO9_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO9_A	1	0x0	Output value for DFT_GPIO2 pad when GPIO9_OR is set
GPIO9_OR	2	0x0	When set, converts the DFT_GPIO2 pad to a software controllable GPIO pad
GPIO9_PU	3	0x1	Weak pull up control for the DFT_GPIO2 pad when GPIO9_OR is set 1 - Weak pull up disabled 0 - Weak pull up enabled
GPIO9_PD	4	0x0	Weak pull down control for the DFT_GPIO2 pad when GPIO9_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled
GPIO9_SCHMEN	5	0x1	Schmidt trigger enable control for the DFT_GPIO2 pad receiver when GPIO9_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO9_Y (R)	6	0x0	Input value sampled by DFT_GPIO2
GPIO10_OE	8	0x0	Output enable control for the DFT_GPIO3 pad when GPIO10_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO10_A	9	0x0	Output value for DFT_GPIO3 pad when GPIO10_OR is set
GPIO10_OR	10	0x0	When set, converts the DFT_GPIO3 pad to a software controllable GPIO pad
GPIO10_PU	11	0x1	Weak pull up control for the DFT_GPIO3 pad when GPIO10_OR is set 1 - Weak pull up disabled 0 - Weak pull up enabled
GPIO10_PD	12	0x0	Weak pull down control for the DFT_GPIO3 pad when GPIO10_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled
GPIO10_SCHMEN	13	0x1	Schmidt trigger enable control for the DFT_GPIO3 pad receiver when GPIO10_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO10_Y (R)	14	0x0	Input value sampled by DFT_GPIO3

GPIO11_OE	16	0x0	Output enable control for the DFT_GPIO4 pad when GPIO11_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO11_A	17	0x0	Output value for DFT_GPIO4 pad when GPIO11_OR is set
GPIO11_OR	18	0x0	When set, converts the DFT_GPIO4 pad to a software controllable GPIO pad
GPIO11_PU	19	0x1	Weak pull up control for the DFT_GPIO4 pad when GPIO11_OR is set 1 - Weak pull up disabled 0 - Weak pull up enabled
GPIO11_PD	20	0x0	Weak pull down control for the DFT_GPIO4 pad when GPIO11_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled
GPIO11_SCHMEN	21	0x1	Schmidt trigger enable control for the DFT_GPIO4 pad receiver when GPIO11_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO11_Y (R)	22	0x0	Input value sampled by DFT_GPIO4
GPIO12_OE	24	0x0	Output enable control for the DFT_GPIO5 pad when GPIO12_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO12_A	25	0x0	Output value for DFT_GPIO5 pad when GPIO12_OR is set
GPIO12_OR	26	0x0	When set, converts the DFT_GPIO5 pad to a software controllable GPIO pad
GPIO12_PU	27	0x1	Weak pull up control for the DFT_GPIO5 pad when GPIO12_OR is set 1 - Weak pull up disabled 0 - Weak pull up enabled
GPIO12_PD	28	0x0	Weak pull down control for the DFT_GPIO5 pad when GPIO12_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled
GPIO12_SCHMEN	29	0x1	Schmidt trigger enable control for the DFT_GPIO5 pad receiver when GPIO12_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO12_Y (R)	30	0x0	Input value sampled by DFT_GPIO5
GPIO_DFT_GPIO2_5			

GPIO_13_16 - RW - 32 bits - HTIUNBIND:0xA7			
Field Name	**Bits**	**Default**	**Description**
GPIO13_OE	0	0x0	Output enable control for the DBG_GPIO0 pad when GPIO13_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO13_A	1	0x0	Output value for DBG_GPIO0 pad when GPIO13_OR is set
GPIO13_OR	2	0x0	When set, converts the DBG_GPIO0 pad to a software controllable GPIO pad
GPIO13_PU	3	0x1	Weak pull up control for the DBG_GPIO0 pad when GPIO13_OR is set 1 - Weak pull up disabled 0 - Weak pull up enabled
GPIO13_PD	4	0x0	Weak pull down control for the DBG_GPIO0 pad when GPIO13_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled

GPIO13_SCHMEN	5	0x1	Schmidt trigger enable control for the DBG_GPIO0 pad receiver when GPIO13_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO13_Y (R)	6	0x0	Input value sampled by DBG_DGPIO0
GPIO14_OE	8	0x0	Output enable control for the DBG_GPIO1 pad when GPIO14_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO14_A	9	0x0	Output value for DBG_GPIO1 pad when GPIO14_OR is set
GPIO14_OR	10	0x0	When set, converts the DBG_GPIO1 pad to a software controllable GPIO pad
GPIO14_PU	11	0x1	Weak pull up control for the DBG_GPIO1 pad when GPIO14_OR is set 1 - Weak pull up disabled 0 - Weak pull up enabled
GPIO14_PD	12	0x0	Weak pull down control for the DBG_GPIO1 pad when GPIO14_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled
GPIO14_SCHMEN	13	0x1	Schmidt trigger enable control for the DBG_GPIO1 pad receiver when GPIO14_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO14_Y (R)	14	0x0	Input value sampled by DBG_DGPIO1
GPIO15_OE	16	0x0	Output enable control for the DBG_GPIO2 pad when GPIO15_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO15_A	17	0x0	Output value for DBG_GPIO2 pad when GPIO15_OR is set
GPIO15_OR	18	0x0	When set, converts the DBG_GPIO2 pad to a software controllable GPIO pad
GPIO15_PU	19	0x1	Weak pull up control for the DBG_GPIO2 pad when GPIO15_OR is set 1 - Weak pull up disabled 0 - Weak pull up enabled
GPIO15_PD	20	0x0	Weak pull down control for the DBG_GPIO2 pad when GPIO15_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled
GPIO15_SCHMEN	21	0x1	Schmidt trigger enable control for the DBG_GPIO2 pad receiver when GPIO15_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO15_Y (R)	22	0x0	Input value sampled by DBG_DGPIO2
GPIO16_OE	24	0x0	Output enable control for the DBG_GPIO3 pad when GPIO16_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO16_A	25	0x0	Output value for DBG_GPIO3 pad when GPIO16_OR is set
GPIO16_OR	26	0x0	When set, converts the DBG_GPIO3 pad to a software controllable GPIO pad
GPIO16_PU	27	0x1	Weak pull up control for the DBG_GPIO3 pad when GPIO16_OR is set 1 - Weak pull up disabled 0 - Weak pull up enabled
GPIO16_PD	28	0x0	Weak pull down control for the DBG_GPIO3 pad when GPIO16_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled

GPIO16_SCHMEN	29	0x1	Schmidt trigger enable control for the DBG_GPIO3 pad receiver when GPIO16_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO16_Y (R)	30	0x0	Input value sampled by DBG_DGPIO3
GPIO_DBG_GPIO0_3			

GPIO_17_20 - RW - 32 bits - HTIUNBIND:0xA8			
Field Name	**Bits**	**Default**	**Description**
GPIO17_OE	0	0x0	Output enable control for the PCIE_RESET_GPIO1 pad when GPIO17_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO17_A	1	0x0	Output value for PCIE_RESET_GPIO1 pad when GPIO17_OR is set
GPIO17_OR	2	0x0	When set, converts the PCIE_RESET_GPIO1 pad to a software controllable GPIO pad
GPIO17_PU	3	0x1	Weak pull up control for the PCIE_RESET_GPIO1 pad when GPIO17_OR is set 1 - Weak pull up disabled 0 - Weak pull up enabled
GPIO17_PD	4	0x0	Weak pull down control for the PCIE_RESET_GPIO1 pad when GPIO17_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled
GPIO17_SCHMEN	5	0x1	Schmidt trigger enable control for the PCIE_RESET_GPIO1 pad receiver when GPIO17_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO17_Y (R)	6	0x0	Input value sampled by PCIE_RESET_GPIO1
GPIO18_OE	8	0x0	Output enable control for the PCIE_RESET_GPIO2 pad when GPIO18_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO18_A	9	0x0	Output value for PCIE_RESET_GPIO2 pad when GPIO18_OR is set
GPIO18_OR	10	0x0	When set, converts the PCIE_RESET_GPIO2 pad to a software controllable GPIO pad
GPIO18_PU	11	0x1	Weak pull up control for the PCIE_RESET_GPIO2 pad when GPIO18_OR is set 1 - Weak pull up disabled 0 - Weak pull up enabled
GPIO18_PD	12	0x0	Weak pull down control for the PCIE_RESET_GPIO2 pad when GPIO18_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled
GPIO18_SCHMEN	13	0x1	Schmidt trigger enable control for the PCIE_RESET_GPIO2 pad receiver when GPIO18_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO18_Y (R)	14	0x0	Input value sampled by PCIE_RESET_GPIO2
GPIO19_OE	16	0x0	Output enable control for the PCIE_RESET_GPIO3 pad when GPIO19_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO19_A	17	0x0	Output value for PCIE_RESET_GPIO3 pad when GPIO19_OR is set

GPIO19_OR	18	0x0	When set, converts the PCIE_RESET_GPIO3 pad to a software controllable GPIO pad
GPIO19_PU	19	0x1	Weak pull up control for the PCIE_RESET_GPIO3 pad when GPIO19_OR is set 1 - Weak pull up disabled 0 - Weak pull up enabled
GPIO19_PD	20	0x0	Weak pull down control for the PCIE_RESET_GPIO3 pad when GPIO19_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled
GPIO19_SCHMEN	21	0x1	Schmidt trigger enable control for the PCIE_RESET_GPIO3 pad receiver when GPIO19_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO19_Y (R)	22	0x0	Input value sampled by PCIE_RESET_GPIO3
GPIO20_OE	24	0x0	Output enable control for the PCIE_RESET_GPIO4 pad when GPIO20_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO20_A	25	0x0	Output value for PCIE_RESET_GPIO4 pad when GPIO20_OR is set
GPIO20_OR	26	0x0	When set, converts the PCIE_RESET_GPIO4 pad to a software controllable GPIO pad
GPIO20_PU	27	0x1	Weak pull up control for the PCIE_RESET_GPIO4 pad when GPIO20_OR is set 1 - Weak pull up disabled 0 - Weak pull up enabled
GPIO20_PD	28	0x0	Weak pull down control for the PCIE_RESET_GPIO4 pad when GPIO20_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled
GPIO20_SCHMEN	29	0x1	Schmidt trigger enable control for the PCIE_RESET_GPIO4 pad receiver when GPIO20_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO20_Y (R)	30	0x0	Input value sampled by PCIE_RESET_GPIO4
GPIO_PCIE_RESET_GPIO1_4			

GPIO_21_24 - RW - 32 bits - HTIUNBIND:0xA9			
Field Name	**Bits**	**Default**	**Description**
GPIO21_OE	0	0x0	Output enable control for the PCIE_RESET_GPIO5 pad when GPIO21_OR is set 1 - Output driver enabled 0 - Output driver disabled
GPIO21_A	1	0x0	Output value for PCIE_RESET_GPIO5 pad when GPIO21_OR is set
GPIO21_OR	2	0x0	When set, converts the PCIE_RESET_GPIO5 pad to a software controllable GPIO pad
GPIO21_PU	3	0x1	Weak pull up control for the PCIE_RESET_GPIO5 pad when GPIO21_OR is set 1 - Weak pull up disabled 0 - Weak pull up enabled
GPIO21_PD	4	0x0	Weak pull down control for the PCIE_RESET_GPIO5 pad when GPIO21_OR is set 1 - Weak pull up enabled 0 - Weak pull up disabled

GPIO21_SCHMEN	5	0x1	Schmidt trigger enable control for the PCIE_RESET_GPIO5 pad receiver when GPIO21_OR is set 1 - Schmidt trigger input enabled 0 - Schmidt trigger input disabled
GPIO21_Y (R)	6	0x0	Input value sampled by PCIE_RESET_GPIO5
GPIO22_OE	8	0x0	Reserved for future use. This register controls no hardware
GPIO22_A	9	0x0	Reserved for future use. This register controls no hardware
GPIO22_OR	10	0x0	Reserved for future use. This register controls no hardware
GPIO22_PU	11	0x1	Reserved for future use. This register controls no hardware
GPIO22_PD	12	0x0	Reserved for future use. This register controls no hardware
GPIO22_SCHMEN	13	0x1	Reserved for future use. This register controls no hardware
GPIO22_Y (R)	14	0x0	Reserved for future use. This register controls no hardware
GPIO23_OE	16	0x0	Reserved for future use. This register controls no hardware
GPIO23_A	17	0x0	Reserved for future use. This register controls no hardware
GPIO23_OR	18	0x0	Reserved for future use. This register controls no hardware
GPIO23_PU	19	0x1	Reserved for future use. This register controls no hardware
GPIO23_PD	20	0x0	Reserved for future use. This register controls no hardware
GPIO23_SCHMEN	21	0x1	Reserved for future use. This register controls no hardware
GPIO23_Y (R)	22	0x0	Reserved for future use. This register controls no hardware
GPIO24_OE	24	0x0	Reserved for future use. This register controls no hardware
GPIO24_A	25	0x0	Reserved for future use. This register controls no hardware
GPIO24_OR	26	0x0	Reserved for future use. This register controls no hardware
GPIO24_PU	27	0x1	Reserved for future use. This register controls no hardware
GPIO24_PD	28	0x0	Reserved for future use. This register controls no hardware
GPIO24_SCHMEN	29	0x1	Reserved for future use. This register controls no hardware
GPIO24_Y (R)	30	0x0	Reserved for future use. This register controls no hardware
GPIO_PCIE_RESET_GPIO5			

GPIO_CNTL_1_24 - RW - 32 bits - HTIUNBIND:0xAA			
Field Name	**Bits**	**Default**	**Description**
TERM_EN	23:0	0x0	This register enables integrated termination for the GPIO pads when the corresponding bit is set to 1 Bit 0 - DFT_GPIO0 termination enable/disable Bit 1 - DFT_GPIO1 termination enable/disable Bit 2 - DFT_GPIO2 termination enable/disable Bit 3 - DFT_GPIO3 termination enable/disable Bit 4 - DFT_GPIO4 termination enable/disable Bit 5 - DFT_GPIO5 termination enable/disable Bit 6 - DBG_GPIO0 termination enable/disable Bit 7 - DBG_GPIO1 termination enable/disable Bit 8 - DBG_GPIO2 termination enable/disable Bit 9 - DBG_GPIO3 termination enable/disable Bit 10 - PCIE_RESET_GPIO1 termination enable/disable Bit 11 - PCIE_RESET_GPIO2 termination enable/disable Bit 12 - PCIE_RESET_GPIO3 termination enable/disable Bit 13 - PCIE_RESET_GPIO4 termination enable/disable Bit 14 - PCIE_RESET_GPIO5 termination enable/disable Bit 15 - PWM_GPIO1 termination enable/disable Bit 16 - PWM_GPIO2 termination enable/disable Bit 17 - PWM_GPIO3 termination enable/disable Bit 18 - PWM_GPIO4 termination enable/disable Bit 19 - PWM_GPIO5 termination enable/disable Bit 20 - PWM_GPIO6 termination enable/disable Bit 21 - I2C_CLK termination enable/disable Bit 22 - I2C_DATA termination enable/disable Bit 23 - STRP_DATA termination enable/disable

Appendix A
Cross-Referenced Index

A.1 Quick Cross-Referenced Index

For users of the PDF version of this document: in the tables below, click on the *name* of a register to go to the description of that register found in *Chapter 2*.

A.2 Registers Sorted By Name

Table 2-1 Registers Sorted by Name

Register Name	Address	Page
CFG_CT_CLKGATE_HTIU	clkconfig:0xF8	2-78
CFG_HT_DIV_CTRL	HTIUNBIND:0x2C	2-220
CFG_IOC_TOM3	NBMISCIND:0x4E	2-168
CLK_ADAPTER_ID	clkconfig:0x2C	2-66
CLK_BAR1_RCRB	clkconfig:0x14	2-66
CLK_BASE_CODE	clkconfig:0xB	2-65
CLK_BIST	clkconfig:0xF	2-66
CLK_CACHE_LINE	clkconfig:0xC	2-65
CLK_CAPABILITIES_PTR	clkconfig:0x34	2-66
CLK_CFG_HTPLL_CNTL	clkconfig:0xD4	2-76
CLK_COMMAND	clkconfig:0x4	2-64
CLK_DEVICE_ID	clkconfig:0x2	2-64
CLK_HEADER	clkconfig:0xE	2-66
CLK_HTPLL_CONTROL	clkconfig:0xD8	2-76
CLK_INTERRUPT_LINE	clkconfig:0x3C	2-66
CLK_INTERRUPT_PIN	clkconfig:0x3D	2-67
CLK_LATENCY	clkconfig:0xD	2-66
CLK_REGPROG_INF	clkconfig:0x9	2-65
CLK_REVISION_ID	clkconfig:0x8	2-65
CLK_STATUS	clkconfig:0x6	2-64
CLK_SUB_CLASS	clkconfig:0xA	2-65
clk_top_pwm1_ctrl	clkconfig:0xB0	2-74
clk_top_pwm2_ctrl	clkconfig:0xB4	2-74
clk_top_pwm3_ctrl	clkconfig:0xCC	2-75
clk_top_pwm4_ctrl	clkconfig:0x4C	2-68
clk_top_pwm5_ctrl	clkconfig:0x50	2-68
clk_top_pwm6_ctrl	clkconfig:0x54	2-68
CLK_TOP_SPARE_A	clkconfig:0xE0	2-77
CLK_TOP_SPARE_B	clkconfig:0xE4	2-77
CLK_TOP_SPARE_C	clkconfig:0xE8	2-77
CLK_TOP_SPARE_D	clkconfig:0xEC	2-78
clk_top_spare_pll	clkconfig:0xD0	2-75
clk_top_test_ctrl	clkconfig:0xB8	2-74
CLK_TOP_THERMAL_ALERT_INTR_EN	clkconfig:0xC0	2-75
CLK_TOP_THERMAL_ALERT_STATUS	clkconfig:0xC4	2-75
CLK_TOP_THERMAL_ALERT_WAIT_WINDOW	clkconfig:0xC8	2-75
CLK_VENDOR_ID	clkconfig:0x0	2-64
CLKGATE_DISABLE	clkconfig:0x94	2-71
CLKGATE_DISABLE2	clkconfig:0x8C	2-71
CORR_PIN_CONTROL	NBMISCIND:0x7A	2-187
CPLL_CONTROL	clkconfig:0x44	2-67
CPLL_CONTROL2	clkconfig:0x98	2-73
CPLL_CONTROL3	clkconfig:0x70	2-69
CT_DISABLE_BIU	clkconfig:0x68	2-69
DELAY_SET_IOC_CCLK	clkconfig:0x5C	2-68
DFT_CNTL0	NBMISCIND:0x5	2-133
DFT_CNTL1	NBMISCIND:0x6	2-133
DFT_CNTL2	NBMISCIND:0x10	2-139
DFT_CNTL3	NBMISCIND:0x7B	2-188
DFT_CNTL4	NBMISCIND:0x1C	2-142
DFT_CNTL5	NBMISCIND:0x1D	2-143
DFT_SPARE	NBMISCIND:0x7F	2-188
EFUSE_CFG_HW_CONFIG_4	NBMISCIND:0x4A	2-168

Table 2-1 Registers Sorted by Name (Continued)

Register Name	Address	Page
EOI_REGISTER	ioapicmmreg\:0x40	2-88
FATAL_PIN_CONTROL	NBMISCIND:0x78	2-186
FEATURES_ENABLE	IOAPICCMISCIND\:0x0	2-89
GC_CLK_CNTRL	clkconfig:0x74	2-70
GPIO_1_4	HTIUNBIND\:0xA4	2-233
GPIO_13_16	HTIUNBIND\:0xA7	2-237
GPIO_17_20	HTIUNBIND\:0xA8	2-239
GPIO_21_24	HTIUNBIND\:0xA9	2-240
GPIO_5_8	HTIUNBIND\:0xA5	2-234
GPIO_9_12	HTIUNBIND\:0xA6	2-236
GPIO_CNTL_1_24	HTIUNBIND\:0xAA	2-241
GPIO_ctrl	clkconfig:0xDC	2-76
GPIO_PAD	NBMISCIND:0x46	2-167
GPIO_PAD_CNTL_PU_PD	NBMISCIND:0x41	2-164
GPIO_PAD_SCHMEM_OE	NBMISCIND:0x42	2-165
GPIO_PAD_SP_SN	NBMISCIND\:0x43	2-166
HOTPLUG_BLINK_RATE	clkconfig\:0x90	2-71
HOTPLUG_SPARE_0	clkconfig\:0xF0	2-78
HOTPLUG_SPARE_1	clkconfig\:0xF4	2-78
HT_BIST_Extended_Control_0	HTIUNBIND:0x21	2-216
HT_BIST_Extended_Control_1	HTIUNBIND:0x22	2-216
HT_ERROR_INJECTION_CNTL	HTIUNBIND\:0x7E	2-228
HT_PARITY_ERR_CONTROL_STATUS	nbconfig:0x68	2-12
HT3PHY_CNTL_1	HTIUNBIND:0x26	2-217
HT3PHY_CNTL_10	HTIUNBIND\:0x49	2-225
HT3PHY_CNTL_11	HTIUNBIND\:0x4A	2-225
HT3PHY_CNTL_12	HTIUNBIND\:0x4B	2-225
HT3PHY_CNTL_13	HTIUNBIND\:0x4C	2-225
HT3PHY_CNTL_14	HTIUNBIND\:0x4D	2-226
HT3PHY_CNTL_15	HTIUNBIND:0x33	2-221
HT3PHY_CNTL_15	HTIUNBIND\:0x33	2-226
HT3PHY_CNTL_2	HTIUNBIND:0x27	2-218
HT3PHY_CNTL_3	HTIUNBIND:0x28	2-218
HT3PHY_CNTL_4	HTIUNBIND:0x29	2-219
HT3PHY_CNTL_5	HTIUNBIND:0x2A	2-219
HT3PHY_CNTL_6	HTIUNBIND:0x2B	2-219
HT3PHY_CNTL_8	HTIUNBIND\:0x47	2-224
HT3PHY_CNTL_9	HTIUNBIND\:0x48	2-224
HTIU_DEBUG	HTIUNBIND:0x5	2-207
HTIU_DOWNSTREAM_CONFIG	HTIUNBIND:0x6	2-207
HTIU_ILA_CONTROL_0	HTIUNBIND:0x78	2-227
HTIU_ILA_CONTROL_1	HTIUNBIND:0x79	2-228
HTIU_ILA_CONTROL_2	HTIUNBIND:0x7A	2-228
HTIU_ILA_CONTROL_3	HTIUNBIND:0x7B	2-228
HTIU_ILA_CONTROL_4	HTIUNBIND:0x7C	2-228
HTIU_ILA_CONTROL_5	HTIUNBIND:0x7D	2-228
HTIU_IOMMU_CONTROL_0	HTIUNBIND:0x2E	2-220
HTIU_IOMMU_CONTROL_1	HTIUNBIND:0x2F	2-220
HTIU_NB_DATA	nbconfig:0x98	2-17
HTIU_NB_INDEX	nbconfig:0x94	2-17
HTIU_PCIE_ERR_FLOOD_CONTROL_0	HTIUNBIND:0x3A	2-221
HTIU_PCIE_ERR_FLOOD_CONTROL_1	HTIUNBIND:0x3B	2-222
HTIU_SCRATCH_0	HTIUNBIND:0xF	2-210
HTIU_SCRATCH_2	HTIUNBIND:0x11	2-210
HTIU_SCRATCH_3	HTIUNBIND:0x12	2-210
HTIU_SCRATCH_4	HTIUNBIND:0x13	2-210
HTIU_SCRATCH_5	HTIUNBIND:0x14	2-210

Table 2-1 Registers Sorted by Name (Continued)

Register Name	Address	Page
HTIU_STATUS_0	HTIUNBIND:0x10	2-210
HTIU_TAG_XTL_CONTROL_0	HTIUNBIND:0x38	2-221
HTIU_TAG_XTL_CONTROL_1	HTIUNBIND:0x39	2-221
HTIU_UPSTREAM_ARB_CONTROL_0	HTIUNBIND\:0x7	2-208
HTIU_UPSTREAM_ARB_CONTROL_1	HTIUNBIND\:0x8	2-209
HTIU_UPSTREAM_ARB_CONTROL_2	HTIUNBIND\:0x9	2-209
HTIU_UPSTREAM_ARB_CONTROL_3	HTIUNBIND\:0xA	2-209
HTIU_UPSTREAM_ARB_CONTROL_4	HTIUNBIND\:0xB	2-209
HTIU_UPSTREAM_ARB_CONTROL_5	HTIUNBIND\:0xC	2-209
HTIU_UPSTREAM_ARB_CONTROL_6	HTIUNBIND\:0xD	2-209
HTIU_UPSTREAM_ARB_CONTROL_8	HTIUNBIND:0x77	2-227
IO_REGISTER_SELECT_INDEX	ioapicmmreg\:0x0	2-88
IO_WINDOW_REGISTER_DATA	ioapicmmreg\:0x10	2-88
IOAPIC_ARBITRATION_REGISTER	IOAPICMMISCIND\:0x2	2-93
IOAPIC_CONF_LOWER	IOAPICCMISCIND\:0x1	2-89
IOAPIC_CONF_UPPER	IOAPICCMISCIND\:0x2	2-89
IOAPIC_DATA	nbconfig\:0xFC	2-30
IOAPIC_ID_REGISTER	IOAPICMMISCIND\:0x0	2-93
IOAPIC_INDEX	nbconfig\:0xF8	2-30
IOAPIC_INT_ROUTING_REGISTER1	IOAPICCMISCIND\:0x3	2-89
IOAPIC_INT_ROUTING_REGISTER2	IOAPICCMISCIND\:0x4	2-90
IOAPIC_INT_ROUTING_REGISTER3	IOAPICCMISCIND\:0x5	2-90
IOAPIC_INT_ROUTING_REGISTER4	IOAPICCMISCIND\:0x6	2-90
IOAPIC_INT_ROUTING_REGISTER5	IOAPICCMISCIND\:0x7	2-91
IOAPIC_INT_ROUTING_REGISTER6	IOAPICCMISCIND\:0x8	2-91
IOAPIC_INT_ROUTING_REGISTER7	IOAPICCMISCIND\:0x9	2-91
IOAPIC_SERIAL_IRQ_STATUS	IOAPICCMISCIND\:0xA	2-92
IOAPIC_VERSION_REGISTER	IOAPICMMISCIND\:0x1	2-93
IOC_DMA_ARBITER	NBMISCIND:0x9	2-136
IOC_FEATURE_CNTL	NBMISCIND\:0x75	2-184
IOC_JTAG_CNTL	NBMISCIND:0x47	2-167
IOC_P2P_CNTL	NBMISCIND:0xC	2-137
IOC_PCIE_CNTL	NBMISCIND:0xB	2-136
IOC_PCIE_CSR_Count	NBMISCIND:0xA	2-136
IOC_PCIE_D10_CNTL	NBMISCIND:0x5F	2-175
IOC_PCIE_D10_CSR_Count	NBMISCIND:0x5E	2-175
IOC_PCIE_D11_CNTL	NBMISCIND:0x61	2-176
IOC_PCIE_D11_CSR_Count	NBMISCIND:0x60	2-176
IOC_PCIE_D12_CNTL	NBMISCIND:0x63	2-177
IOC_PCIE_D12_CSR_Count	NBMISCIND:0x62	2-177
IOC_PCIE_D13_CNTL	NBMISCIND:0x1F	2-143
IOC_PCIE_D13_CSR_Count	NBMISCIND:0x1E	2-143
IOC_PCIE_D2_CNTL	NBMISCIND:0x51	2-169
IOC_PCIE_D2_CSR_Count	NBMISCIND:0x50	2-169
IOC_PCIE_D3_CNTL	NBMISCIND:0x53	2-170
IOC_PCIE_D3_CSR_Count	NBMISCIND:0x52	2-169
IOC_PCIE_D4_CNTL	NBMISCIND:0x55	2-171
IOC_PCIE_D4_CSR_Count	NBMISCIND:0x54	2-170
IOC_PCIE_D5_CNTL	NBMISCIND:0x57	2-171
IOC_PCIE_D5_CSR_Count	NBMISCIND:0x56	2-171
IOC_PCIE_D6_CNTL	NBMISCIND:0x59	2-172
IOC_PCIE_D6_CSR_Count	NBMISCIND:0x58	2-172
IOC_PCIE_D7_CNTL	NBMISCIND:0x5B	2-173
IOC_PCIE_D7_CSR_Count	NBMISCIND:0x5A	2-173
IOC_PCIE_D9_CNTL	NBMISCIND:0x5D	2-174
IOC_PCIE_D9_CSR_Count	NBMISCIND:0x5C	2-174
IOCIsocMapAddr_HI	NBMISCIND:0xF	2-139

Table 2-1 Registers Sorted by Name (Continued)

Register Name	Address	Page
IOCIsocMapAddr_LO	NBMISCIND:0xE	2-139
IOMMU_ADAPTER_ID	nbconfigfunc2:0x2C	2-34
IOMMU_ADAPTER_ID_W	nbconfigfunc2:0x68	2-37
IOMMU_BASE_CODE	nbconfigfunc2:0xB	2-33
IOMMU_BIST	nbconfigfunc2:0xF	2-34
IOMMU_CACHE_LINE	nbconfigfunc2:0xC	2-33
IOMMU_CAP_BASE_HI	nbconfigfunc2:0x48	2-35
IOMMU_CAP_BASE_LO	nbconfigfunc2:0x44	2-35
IOMMU_CAP_HEADER	nbconfigfunc2:0x40	2-34
IOMMU_CAP_MISC	nbconfigfunc2:0x50	2-35
IOMMU_CAP_RANGE	nbconfigfunc2:0x4C	2-35
IOMMU_CAPABILITIES_PTR	nbconfigfunc2:0x34	2-34
IOMMU_COMMAND	nbconfigfunc2:0x4	2-31
IOMMU_CONTROL_W	nbconfigfunc2:0x6C	2-37
IOMMU_DEVICE_ID	nbconfigfunc2:0x2	2-31
IOMMU_HEADER	nbconfigfunc2:0xE	2-33
IOMMU_INTERRUPT_LINE	nbconfigfunc2:0x3C	2-34
IOMMU_INTERRUPT_PIN	nbconfigfunc2:0x3D	2-34
IOMMU_LATENCY	nbconfigfunc2:0xD	2-33
IOMMU_MMIO_CMD_BASE_0	iommummreg:0x8	2-81
IOMMU_MMIO_CMD_BASE_1	iommummreg:0xC	2-81
IOMMU_MMIO_CMD_BUF_HDPTR_0	iommummreg:0x2000	2-85
IOMMU_MMIO_CMD_BUF_HDPTR_1	iommummreg:0x2004	2-85
IOMMU_MMIO_CMD_BUF_TAILPTR_0	iommummreg:0x2008	2-85
IOMMU_MMIO_CMD_BUF_TAILPTR_1	iommummreg:0x200C	2-86
IOMMU_MMIO_CNTRL_0	iommummreg:0x18	2-82
IOMMU_MMIO_CNTRL_1	iommummreg:0x1C	2-84
IOMMU_MMIO_DEVTBL_BASE_0	iommummreg:0x0	2-81
IOMMU_MMIO_DEVTBL_BASE_1	iommummreg:0x4	2-81
IOMMU_MMIO_EVENT_BASE_0	iommummreg:0x10	2-82
IOMMU_MMIO_EVENT_BASE_1	iommummreg:0x14	2-82
IOMMU_MMIO_EVENT_BUF_HDPTR_0	iommummreg:0x2010	2-86
IOMMU_MMIO_EVENT_BUF_HDPTR_1	iommummreg:0x2014	2-86
IOMMU_MMIO_EVENT_BUF_TAILPTR_0	iommummreg:0x2018	2-86
IOMMU_MMIO_EVENT_BUF_TAILPTR_1	iommummreg:0x201C	2-87
IOMMU_MMIO_EXCL_BASE_0	iommummreg:0x20	2-84
IOMMU_MMIO_EXCL_BASE_1	iommummreg:0x24	2-84
IOMMU_MMIO_EXCL_LIM_0	iommummreg:0x28	2-85
IOMMU_MMIO_EXCL_LIM_1	iommummreg:0x2C	2-85
IOMMU_MMIO_STATUS_0	iommummreg:0x2020	2-87
IOMMU_MMIO_STATUS_1	iommummreg:0x2024	2-87
IOMMU_MSI_ADDR_HI	nbconfigfunc2:0x5C	2-36
IOMMU_MSI_ADDR_LO	nbconfigfunc2:0x58	2-36
IOMMU_MSI_CAP	nbconfigfunc2:0x54	2-36
IOMMU_MSI_DATA	nbconfigfunc2:0x60	2-36
IOMMU_MSI_MAPPING_CAP	nbconfigfunc2:0x64	2-37
IOMMU_REGPROG_INF	nbconfigfunc2:0x9	2-33
IOMMU_REVISION_ID	nbconfigfunc2:0x8	2-33
IOMMU_STATUS	nbconfigfunc2:0x6	2-32
IOMMU_SUB_CLASS	nbconfigfunc2:0xA	2-33
IOMMU_VENDOR_ID	nbconfigfunc2:0x0	2-31
IRQ_PIN_ASSERTION_REGISTER	ioapicmmreg\:0x20	2-88
L1_BANK_DISABLE_0	L1CFGIND:0x11	2-191
L1_BANK_SEL_0	L1CFGIND:0x10	2-191
L1_CNTRL_0	L1CFGIND:0xC	2-189
L1_CNTRL_1	L1CFGIND\:0xD	2-190
L1_CNTRL_2	L1CFGIND\:0xE	2-190

Table 2-1 Registers Sorted by Name (Continued)

Register Name	Address	Page
L1_CNTRL_3	L1CFGIND\:0xF	2-191
L1_DEBUG_0	L1CFGIND:0x6	2-189
L1_DEBUG_1	L1CFGIND:0x7	2-189
L1_DEBUG_STATUS	L1CFGIND:0x8	2-189
L1_WQ_STATUS_0	L1CFGIND:0x20	2-191
L1_WQ_STATUS_1	L1CFGIND:0x21	2-191
L1_WQ_STATUS_2	L1CFGIND:0x22	2-192
L1_WQ_STATUS_3	L1CFGIND:0x23	2-192
L1CFG_DATA	nbconfigfunc2:0xFC	2-38
L1CFG_INDEX	nbconfigfunc2:0xF8	2-38
L2_CONTROL_0	L2CFGIND\:0xC	2-193
L2_CONTROL_0	L2CFGIND:0xC	2-194
L2_CONTROL_1	L2CFGIND\:0xD	2-195
L2_CONTROL_5	L2CFGIND\:0x4C	2-200
L2_CONTROL_6	L2CFGIND\:0x4D	2-201
L2_CP_CONTROL	L2CFGIND\:0x56	2-202
L2_CREDIT_CONTROL_0	L2CFGIND\:0x70	2-203
L2_CREDIT_CONTROL_1	L2CFGIND\:0x71	2-204
L2_CREDIT_CONTROL_2	L2CFGIND\:0x20	2-199
L2_DEBUG_0	L2CFGIND:0x6	2-193
L2_DEBUG_1	L2CFGIND:0x7	2-193
L2_DEBUG_2	L2CFGIND:0x43	2-199
L2_DEBUG_3	L2CFGIND:0x44	2-200
L2_DTC_CONTROL	L2CFGIND:0x10	2-195
L2_DTC_HASH_CONTROL	L2CFGIND:0x11	2-195
L2_DTC_WAY_CONTROL	L2CFGIND:0x12	2-196
L2_ERR_RULE_CONTROL_0	L2CFGIND\:0x80	2-204
L2_ERR_RULE_CONTROL_1	L2CFGIND\:0x81	2-204
L2_ERR_RULE_CONTROL_2	L2CFGIND\:0x82	2-205
L2_ERR_RULE_CONTROL_3	L2CFGIND\:0x30	2-199
L2_ERR_RULE_CONTROL_4	L2CFGIND\:0x31	2-199
L2_ERR_RULE_CONTROL_5	L2CFGIND\:0x32	2-199
L2_INT_CONTROL	L2CFGIND\:0x6A	2-203
L2_ITC_CONTROL	L2CFGIND:0x14	2-196
L2_ITC_HASH_CONTROL	L2CFGIND:0x15	2-196
L2_ITC_WAY_CONTROL	L2CFGIND:0x16	2-197
L2_MCIF_CONTROL	L2CFGIND\:0x78	2-204
L2_PDC_CONTROL	L2CFGIND:0x50	2-201
L2_PDC_HASH_CONTROL	L2CFGIND:0x51	2-202
L2_PDC_WAY_CONTROL	L2CFGIND:0x52	2-202
L2_PTC_A_CONTROL	L2CFGIND:0x18	2-197
L2_PTC_A_HASH_CONTROL	L2CFGIND:0x19	2-197
L2_PTC_A_WAY_CONTROL	L2CFGIND:0x1A	2-198
L2_PTC_B_CONTROL	L2CFGIND:0x1C	2-198
L2_PTC_B_HASH_CONTROL	L2CFGIND:0x1D	2-198
L2_PTC_B_WAY_CONTROL	L2CFGIND:0x1E	2-199
L2_STATUS_0	L2CFGIND:0x8	2-193
L2_STATUS_1	L2CFGIND:0x45	2-200
L2_TW_CONTROL	L2CFGIND:0x54	2-202
L2_TW_CONTROL_1	L2CFGIND\:0x60	2-203
L2_TW_CONTROL_2	L2CFGIND\:0x61	2-203
L2_TW_CONTROL_3	L2CFGIND\:0x62	2-203
L2CFG_DATA	nbconfigfunc2:0xF4	2-37
L2CFG_INDEX	nbconfigfunc2:0xF0	2-37
Link_State_Control_0	HTIUNBIND:0x15	2-210
Link_State_Control_1	HTIUNBIND:0x16	2-211
Link_State_Control_2	HTIUNBIND:0x17	2-212

Table 2-1 Registers Sorted by Name (Continued)

Register Name	Address	Page
Link_State_Control_3	HTIUNBIND:0x18	2-212
Link_State_Control_4	HTIUNBIND:0x19	2-212
Link_State_Control_5	HTIUNBIND:0x1A	2-212
Link_State_Control_6	HTIUNBIND:0x1B	2-212
Link_State_Control_7	HTIUNBIND:0x1C	2-213
LS_History0	HTIUNBIND:0x40	2-222
LS_History1	HTIUNBIND:0x41	2-223
LS_History2	HTIUNBIND:0x42	2-223
LS_History3	HTIUNBIND:0x43	2-223
LS_History4	HTIUNBIND:0x44	2-223
LS_History5	HTIUNBIND:0x45	2-224
MC_ACMD_DLL_CNTRL_A	clkconfig:0x88	2-71
MC_ACMD_DLL_CNTRL_B	clkconfig:0x89	2-71
MC_CLK_CNTRL	clkconfig:0x58	2-68
MC_CLK_DATA	clkconfig:0x64	2-69
MC_CLK_INDEX	clkconfig:0x60	2-68
MC_DATA_DLL_CNTRL_A	clkconfig:0x80	2-70
MMIO_BASE_LIMIT_UPPER	NBMISCIND:0x76	2-185
MSI_CAPABILITY_POINTER_0	nbconfig:0x70	2-14
MSI_CAPABILITY_POINTER_1	nbconfig:0x74	2-14
MSI_CAPABILITY_POINTER_2	nbconfig:0x78	2-14
MSI_MAPPING_CAPABILITY	nbconfig:0xF0	2-30
NB_ADAPTER_ID	nbconfig:0x2C	1-1
NB_ADAPTER_ID	nbconfig:0x2C	2-8
NB_ADAPTER_ID_W	nbconfig:0x50	2-11
NB_APIC_P2P_CNTL	NBMISCIND:0x3D	2-162
NB_APIC_P2P_RANGE_0	NBMISCIND:0x3E	2-164
NB_APIC_P2P_RANGE_1	NBMISCIND:0x3F	2-164
NB_APIC_P2P_RANGE_2	NBMISCIND:0x40	2-164
NB_BAR1_RCRB	nbconfig:0x14	2-7
NB_BAR2_PM2	nbconfig:0x18	2-7
NB_BAR3_PCIEXP_MMCFG	nbconfig:0x1C	2-8
NB_BAR3_UPPER_PCIEXP_MMCFG	nbconfig:0x20	2-8
NB_BASE_CODE	nbconfig:0xB	2-6
NB_BIST	nbconfig:0xF	2-7
NB_BROADCAST_BASE_HI	NBMISCIND:0x3B	2-162
NB_BROADCAST_BASE_LO	NBMISCIND:0x3A	2-162
NB_BROADCAST_CNTL	NBMISCIND:0x3C	2-162
NB_BUS_NUM_CNTL	NBMISCIND:0x11	2-139
NB_CACHE_LINE	nbconfig:0xC	2-6
NB_CAPABILITIES_PTR	nbconfig:0x34	2-8
NB_CFG_STAT	nbconfig:0x88	2-16
NB_CNTL	NBMISCIND:0x0	2-132
NB_COMMAND	nbconfig:0x4	2-4
NB_DEVICE_ID	nbconfig:0x2	2-4
NB_HEADER	nbconfig:0xE	2-6
NB_HT_CLK_CNTL_RECEIVER_COMP_CNTL	HTIUNBIND:0x0	2-206
NB_HT_ENUMERATION_SCRATCHPAD	nbconfig:0xD8	2-29
NB_HT_ERROR_RETRY_CAPABILITY	nbconfig:0x40	2-9
NB_HT_ERROR_RETRY_CONTROL_STATUS	nbconfig:0x44	2-9
NB_HT_ERROR_RETRY_COUNT	nbconfig:0x48	2-9
NB_HT_LINK_COMMAND	nbconfig:0xC4	2-25
NB_HT_LINK_CONF_CNTL	nbconfig\:0xC8	2-26
NB_HT_LINK_END	nbconfig:0xCC	2-27
NB_HT_LINK_FREQ_CAP_A	nbconfig:0xD0	2-27
NB_HT_LINK_FREQ_CAP_B	nbconfig:0xD4	2-28
NB_HT_MEMORY_BASE_UPPER	nbconfig:0xDC	2-29

Table 2-1 Registers Sorted by Name (Continued)

Register Name	Address	Page
NB_HT_TRANS_COMP_CNTL	HTIUNBIND:0x1	2-206
NB_HT3_BIST_CONTROL	nbconfig:0xC0	2-25
NB_HT3_CAPABILITY	nbconfig:0x9C	2-17
NB_HT3_GLOBAL_LINK_TRAIN	nbconfig:0xA0	2-17
NB_HT3_LINK_FREQUENCY_EXTENSION	nbconfig:0xB0	2-22
NB_HT3_LINK_RECEIVER_CONF_0	nbconfig:0xA8	2-20
NB_HT3_LINK_RECEIVER_CONF_1	nbconfig:0xB8	2-23
NB_HT3_LINK_TRAINING_0	nbconfig:0xAC	2-21
NB_HT3_LINK_TRAINING_1	nbconfig:0xBC	2-24
NB_HT3_LINK_TRANSMITTER_CONF_0	nbconfig:0xA4	2-19
NB_HT3_LINK_TRANSMITTER_CONF_1	nbconfig:0xB4	2-23
NB_HTIU_CFG	HTIUNBIND:0x32	2-221
NB_INTERRUPT_LINE	nbconfig:0x3C	2-8
NB_INTERRUPT_PIN	nbconfig:0x3D	2-9
NB_IOC_CFG_CNTL	nbconfig:0x7C	2-14
NB_IOC_DEBUG	NBMISCIND:0x1	2-132
NB_LATENCY	nbconfig:0xD	2-6
NB_LOWER_TOP_OF_DRAM2	HTIUNBIND:0x30	2-220
NB_MISC_DATA	nbconfig:0x64	2-12
NB_MISC_INDEX	nbconfig:0x60	2-12
NB_MMIOBASE	NBMISCIND:0x17	2-140
NB_MMIOLIMIT	NBMISCIND:0x18	2-140
NB_PCI_ARB	nbconfig:0x84	2-15
NB_PCI_CTRL	nbconfig:0x4C	2-10
NB_PCIE_INDX_ADDR	nbconfig:0xE0	2-29
NB_PCIE_INDX_DATA	nbconfig:0xE4	2-30
NB_PROG_DEVICE_REMAP_0	NBMISCIND:0x20	2-144
NB_PROG_DEVICE_REMAP_1	NBMISCIND:0x21	2-144
NB_REGPROG_INF	nbconfig:0x9	2-6
NB_REVISION_ID	nbconfig:0x8	2-6
NB_SPARE1	NBMISCIND:0x2	2-133
NB_STATUS	nbconfig:0x6	2-5
NB_STRAPS_READBACK_DATA	NBMISCIND:0x4	2-133
NB_STRAPS_READBACK_MUX	NBMISCIND:0x3	2-133
NB_SUB_CLASS	nbconfig:0xA	2-6
NB_TOM_PCI	NBMISCIND:0x16	2-140
NB_TOP_OF_DRAM_SLOT1	nbconfig:0x90	2-17
NB_UNITID_CLUMPING_CAPABILITY	nbconfig:0x54	2-11
NB_UNITID_CLUMPING_ENABLE	nbconfig:0x5C	2-12
NB_UNITID_CLUMPING_SUPPORT	nbconfig:0x58	2-12
NB_UPPER_TOP_OF_DRAM2	HTIUNBIND:0x31	2-220
NB_VENDOR_ID	nbconfig:0x0	2-4
NBCLK_IO_CONTROL	clkconfig:0xBC	2-74
NON_FATAL_PIN_CONTROL	NBMISCIND:0x79	2-187
OSC_CONTROL	clkconfig:0x40	2-67
PARITY_ERROR_INJECTION_CNTL	HTIUNBIND\:0x80	2-229
PARITY_ERROR_STATUS_0	HTIUNBIND:0x81	2-229
PARITY_ERROR_STATUS_1	HTIUNBIND:0x82	2-229
PARITY_ERROR_STATUS_10	HTIUNBIND:0x8B	2-231
PARITY_ERROR_STATUS_11	HTIUNBIND:0x8C	2-231
PARITY_ERROR_STATUS_12	HTIUNBIND:0x8D	2-231
PARITY_ERROR_STATUS_13	HTIUNBIND:0x8E	2-231
PARITY_ERROR_STATUS_14	HTIUNBIND:0x8F	2-231
PARITY_ERROR_STATUS_15	HTIUNBIND:0x90	2-231
PARITY_ERROR_STATUS_16	HTIUNBIND:0x91	2-232
PARITY_ERROR_STATUS_17	HTIUNBIND:0x92	2-232
PARITY_ERROR_STATUS_18	HTIUNBIND:0x93	2-232

Table 2-1 Registers Sorted by Name (Continued)

Register Name	Address	Page
PARITY_ERROR_STATUS_19	HTIUNBIND:0x94	2-232
PARITY_ERROR_STATUS_2	HTIUNBIND:0x83	2-230
PARITY_ERROR_STATUS_20	HTIUNBIND:0x95	2-232
PARITY_ERROR_STATUS_21	HTIUNBIND:0x96	2-232
PARITY_ERROR_STATUS_22	HTIUNBIND:0x97	2-232
PARITY_ERROR_STATUS_23	HTIUNBIND:0x98	2-233
PARITY_ERROR_STATUS_24	HTIUNBIND:0x99	2-233
PARITY_ERROR_STATUS_25	HTIUNBIND:0x9A	2-233
PARITY_ERROR_STATUS_3	HTIUNBIND:0x84	2-230
PARITY_ERROR_STATUS_4	HTIUNBIND:0x85	2-230
PARITY_ERROR_STATUS_5	HTIUNBIND:0x86	2-230
PARITY_ERROR_STATUS_6	HTIUNBIND:0x87	2-230
PARITY_ERROR_STATUS_7	HTIUNBIND:0x88	2-230
PARITY_ERROR_STATUS_8	HTIUNBIND:0x89	2-230
PARITY_ERROR_STATUS_9	HTIUNBIND:0x8A	2-231
PCIE_ACS_CAP	pcieConfigDev[13:2]:0x194	2-62
PCIE_ACS_CNTL	pcieConfigDev[13:2]:0x196	2-63
PCIE_ACS_ENH_CAP_LIST	pcieConfigDev[13:2]:0x190	2-62
PCIE_ADV_ERR_CAP_CNTL	pcieConfigDev[13:2]:0x168	2-60
PCIE_ADV_ERR_RPT_ENH_CAP_LIST	pcieConfigDev[13:2]:0x150	2-59
PCIE_B_P90_CNTL	PCIEIND:0xC3	2-107
PCIE_BASE_CLASS	pcieConfigDev[13:2]:0xB	2-41
PCIE_BIST	pcieConfigDev[13:2]:0xF	2-41
PCIE_BUS_CNTL	PCIEIND:0x21	2-100
PCIE_CACHE_LINE	pcieConfigDev[13:2]:0xC	2-41
PCIE_CAP	pcieConfigDev[13:2]:0x5A	2-46
PCIE_CAP_LIST	pcieConfigDev[13:2]:0x58	2-46
PCIE_CAP_PTR	pcieConfigDev[13:2]:0x34	2-44
PCIE_CFG_CNTL	PCIEIND:0x3C	2-103
PCIE_CI_CNTL	PCIEIND:0x20	2-99
PCIE_CI_MST_C_RTR_TIMEOUT_CNTL	PCIEIND:0x16	2-98
PCIE_CI_MST_R_RTR_TIMEOUT_CNTL	PCIEIND:0x15	2-98
PCIE_CI_SLV_R_RTR_TIMEOUT_CNTL	PCIEIND:0x14	2-97
PCIE_CNTL	PCIEIND:0x10	2-96
PCIE_CNTL2	PCIEIND:0x1C	2-99
PCIE_COMMAND	pcieConfigDev[13:2]:0x4	2-39
PCIE_CONFIG_CNTL	PCIEIND:0x11	2-96
PCIE_CORE_ARB	NBMISCIND:0x12	2-139
PCIE_CORE_ARB_2	NBMISCIND:0x74	2-184
PCIE_CORR_ERR_MASK	pcieConfigDev[13:2]:0x164	2-60
PCIE_CORR_ERR_STATUS	pcieConfigDev[13:2]:0x160	2-60
PCIE_DEBUG_CNTL	PCIEIND:0x12	2-96
PCIE_DEV_SERIAL_NUM_DW1	pcieConfigDev[13:2]:0x144	2-59
PCIE_DEV_SERIAL_NUM_DW2	pcieConfigDev[13:2]:0x148	2-59
PCIE_DEV_SERIAL_NUM_ENH_CAP_LIST	pcieConfigDev[13:2]:0x140	2-58
PCIE_DEVICE_CAP	pcieConfigDev[13:2]:0x5C	2-46
PCIE_DEVICE_CAP2	pcieConfigDev[13:2]:0x7C	2-52
PCIE_DEVICE_CNTL	pcieConfigDev[13:2]:0x60	2-47
PCIE_DEVICE_CNTL2	pcieConfigDev[13:2]:0x80	2-52
PCIE_DEVICE_ID	pcieConfigDev[13:2]:0x2	2-39
PCIE_DEVICE_SERIAL_NO_0	clkconfig\:0x9C	2-74
PCIE_DEVICE_SERIAL_NO_1	clkconfig\:0xA0	2-74
PCIE_DEVICE_STATUS	pcieConfigDev[13:2]:0x62	2-48
PCIE_DEVICE_STATUS2	pcieConfigDev[13:2]:0x82	2-53
PCIE_ERR_CNTL	PCIEIND_P:0x6A	2-119
PCIE_ERR_SRC_ID	pcieConfigDev[13:2]:0x184	2-62
PCIE_EXT_BRIDGE_CNTL	pcieConfigDev[13:2]\:0x40	2-45

Table 2-1 Registers Sorted by Name (Continued)

Register Name	Address	Page
PCIE_FC_CPL	PCIEIND_P:0x62	2-119
PCIE_FC_NP	PCIEIND_P:0x61	2-118
PCIE_FC_P	PCIEIND_P:0x60	2-118
PCIE_GFX_P2P_ARBITRER_CONTROL	NBMISCIND:0x49	2-168
PCIE_GFX_P2P_CONTROL	NBMISCIND:0x48	2-167
PCIE_GFX2_P2P_ARBITRER_CONTROL	NBMISCIND:0x2F	2-155
PCIE_HDR_LOG0	pcieConfigDev[13:2]:0x16C	2-61
PCIE_HDR_LOG1	pcieConfigDev[13:2]:0x170	2-61
PCIE_HDR_LOG2	pcieConfigDev[13:2]:0x174	2-61
PCIE_HDR_LOG3	pcieConfigDev[13:2]:0x178	2-61
PCIE_HEADER	pcieConfigDev[13:2]:0xE	2-41
PCIE_HW_DEBUG	PCIEIND:0x2	2-95
PCIE_I2C_DEBUG_BUS	PCIEIND:0x39	2-102
PCIE_I2C_REG_ADDR_EXPAND	PCIEIND:0x3A	2-103
PCIE_I2C_REG_DATA	PCIEIND:0x3B	2-103
PCIE_INTERRUPT_LINE	pcieConfigDev[13:2]:0x3C	2-44
PCIE_INTERRUPT_PIN	pcieConfigDev[13:2]:0x3D	2-45
PCIE_IO_BASE_LIMIT	pcieConfigDev[13:2]:0x1C	2-42
PCIE_IO_BASE_LIMIT_HI	pcieConfigDev[13:2]:0x30	2-44
PCIE_IRQ_BRIDGE_CNTL	pcieConfigDev[13:2]:0x3E	2-44
PCIE_LATENCY	pcieConfigDev[13:2]:0xD	2-41
PCIE_LC_BW_CHANGE_CNTL	PCIEIND_P:0xB2	2-129
PCIE_LC_CDR_CNTL	PCIEIND_P:0xB3	2-129
PCIE_LC_CNTL	PCIEIND_P:0xA0	2-121
PCIE_LC_CNTL2	PCIEIND_P:0xB1	2-128
PCIE_LC_CNTL3	PCIEIND_P:0xB5	2-130
PCIE_LC_LANE_CNTL	PCIEIND_P:0xB4	2-129
PCIE_LC_LINK_WIDTH_CNTL	PCIEIND_P:0xA2	2-123
PCIE_LC_N_FTS_CNTL	PCIEIND_P:0xA3	2-124
PCIE_LC_SPEED_CNTL	PCIEIND_P:0xA4	2-124
PCIE_LC_STATE0	PCIEIND_P:0xA5	2-127
PCIE_LC_STATE1	PCIEIND_P:0xA6	2-127
PCIE_LC_STATE10	PCIEIND:0x26	2-100
PCIE_LC_STATE11	PCIEIND:0x27	2-101
PCIE_LC_STATE2	PCIEIND_P:0xA7	2-127
PCIE_LC_STATE3	PCIEIND_P:0xA8	2-127
PCIE_LC_STATE4	PCIEIND_P:0xA9	2-127
PCIE_LC_STATE5	PCIEIND_P:0xAA	2-128
PCIE_LC_STATE6	PCIEIND:0x22	2-100
PCIE_LC_STATE7	PCIEIND:0x23	2-100
PCIE_LC_STATE8	PCIEIND:0x24	2-100
PCIE_LC_STATE9	PCIEIND:0x25	2-100
PCIE_LC_STATUS1	PCIEIND:0x28	2-101
PCIE_LC_STATUS2	PCIEIND:0x29	2-101
PCIE_LC_TRAINING_CNTL	PCIEIND_P:0xA1	2-122
PCIE_LINK_CAP	pcieConfigDev[13:2]:0x64	2-48
PCIE_LINK_CAP2	pcieConfigDev[13:2]:0x84	2-53
PCIE_LINK_CFG	NBMISCIND:0x8	2-134
PCIE_LINK_CNTL	pcieConfigDev[13:2]:0x68	2-49
PCIE_LINK_CNTL2	pcieConfigDev[13:2]:0x88	2-53
PCIE_LINK_DISABLE_CONTROL1	NBMISCIND\:0xD	2-138
PCIE_LINK_DISABLE_CONTROL2	NBMISCIND\:0x4F	2-168
PCIE_LINK_STATUS	pcieConfigDev[13:2]:0x6A	2-49
PCIE_LINK_STATUS2	pcieConfigDev[13:2]:0x8A	2-53
PCIE_MEM_BASE_LIMIT	pcieConfigDev[13:2]:0x20	2-43
PCIE_MSI_CAP_LIST	pcieConfigDev[13:2]:0xA0	2-54
PCIE_MSI_MAP_CAP_LIST	pcieConfigDev[13:2]:0xB8	2-55

Table 2-1 Registers Sorted by Name (Continued)

Register Name	Address	Page
PCIE_MSI_MSG_ADDR_HI	pcieConfigDev[13:2]:0xA8	2-55
PCIE_MSI_MSG_ADDR_LO	pcieConfigDev[13:2]:0xA4	2-54
PCIE_MSI_MSG_CNTL	pcieConfigDev[13:2]:0xA2	2-54
PCIE_MSI_MSG_DATA	pcieConfigDev[13:2]:0xA8	2-55
PCIE_MSI_MSG_DATA_64	pcieConfigDev[13:2]:0xAC	2-55
PCIE_NBCFG_REG10	NBMISCIND:0x28	2-149
PCIE_NBCFG_REG11	NBMISCIND:0x29	2-151
PCIE_NBCFG_REG12	NBMISCIND:0x2A	2-151
PCIE_NBCFG_REG13	NBMISCIND:0x2B	2-152
PCIE_NBCFG_REG14	NBMISCIND:0x2C	2-153
PCIE_NBCFG_REG15	NBMISCIND:0x2D	2-154
PCIE_NBCFG_REG16	NBMISCIND:0x2E	2-154
PCIE_NBCFG_REG17	NBMISCIND:0x19	2-140
PCIE_NBCFG_REG18	NBMISCIND:0x1A	2-141
PCIE_NBCFG_REG19	NBMISCIND:0x1B	2-142
PCIE_NBCFG_REG2	NBMISCIND:0x32	2-156
PCIE_NBCFG_REG3	NBMISCIND:0x33	2-156
PCIE_NBCFG_REG4	NBMISCIND:0x34	2-158
PCIE_NBCFG_REG5	NBMISCIND:0x35	2-159
PCIE_NBCFG_REG6	NBMISCIND:0x36	2-160
PCIE_NBCFG_REG7	NBMISCIND:0x37	2-160
PCIE_NBCFG_REG8	NBMISCIND:0x38	2-161
PCIE_NBCFG_REG9	NBMISCIND:0x39	2-161
PCIE_NBCFG_REGA	NBMISCIND:0x22	2-144
PCIE_NBCFG_REGB	NBMISCIND:0x23	2-144
PCIE_NBCFG_REGC	NBMISCIND:0x24	2-145
PCIE_NBCFG_REGD	NBMISCIND:0x25	2-146
PCIE_NBCFG_REGE	NBMISCIND:0x26	2-147
PCIE_NBCFG_REGF	NBMISCIND:0x27	2-148
PCIE_P_BUF_STATUS	PCIEIND:0x41	2-104
PCIE_P_CNTL	PCIEIND:0x40	2-103
PCIE_P_DECODER_STATUS	PCIEIND:0x42	2-104
PCIE_P_IMP_CNTL_STRENGTH	PCIEIND:0x60	2-105
PCIE_P_IMP_CNTL_UPDATE	PCIEIND:0x61	2-105
PCIE_P_MISC_STATUS	PCIEIND:0x43	2-105
PCIE_P_PAD_FORCE_DIS	PCIEIND:0x65	2-106
PCIE_P_PAD_FORCE_EN	PCIEIND:0x64	2-106
PCIE_P_PAD_MISC_CNTL	PCIEIND:0x63	2-106
PCIE_P_PLL_CNTL	PCIEIND:0x44	2-105
PCIE_P_PORT_LANE_STATUS	PCIEIND_P:0x50	2-118
PCIE_P_RCV_L0S_FTS_DET	PCIEIND:0x50	2-105
PCIE_P_STR_CNTL_UPDATE	PCIEIND:0x62	2-106
PCIE_P90_BRX_PRBS10_ER	PCIEIND:0xC7	2-108
PCIE_P90RX_PRBS10_CNTL	PCIEIND:0xC6	2-108
PCIE_PDNB_CNTL	NBMISCIND:0x7	2-134
PCIE_PMI_CAP	pcieConfigDev[13:2]:0x52	2-45
PCIE_PMI_CAP_LIST	pcieConfigDev[13:2]:0x50	2-45
PCIE_PMI_STATUS_CNTL	pcieConfigDev[13:2]:0x54	2-45
PCIE_PORT_DATA	pcieConfigDev[13:2]:0xE4	2-55
PCIE_PORT_INDEX	pcieConfigDev[13:2]:0xE0	2-55
PCIE_PORT_VC_CAP_REG1	pcieConfigDev[13:2]:0x114	2-56
PCIE_PORT_VC_CAP_REG2	pcieConfigDev[13:2]:0x118	2-57
PCIE_PORT_VC_CNTL	pcieConfigDev[13:2]:0x11C	2-57
PCIE_PORT_VC_STATUS	pcieConfigDev[13:2]:0x11E	2-57
PCIE_PRBS_CLR	PCIEIND:0xC8	2-108
PCIE_PRBS_ERRCNT_0	PCIEIND:0xD0	2-110
PCIE_PRBS_ERRCNT_1	PCIEIND:0xD1	2-110

Table 2-1 Registers Sorted by Name (Continued)

Register Name	Address	Page
PCIE_PRBS_ERRCNT_10	PCIEIND:0xDA	2-111
PCIE_PRBS_ERRCNT_11	PCIEIND:0xDB	2-111
PCIE_PRBS_ERRCNT_12	PCIEIND:0xDC	2-111
PCIE_PRBS_ERRCNT_13	PCIEIND:0xDD	2-111
PCIE_PRBS_ERRCNT_14	PCIEIND:0xDE	2-111
PCIE_PRBS_ERRCNT_15	PCIEIND:0xDF	2-111
PCIE_PRBS_ERRCNT_2	PCIEIND:0xD2	2-110
PCIE_PRBS_ERRCNT_3	PCIEIND:0xD3	2-110
PCIE_PRBS_ERRCNT_4	PCIEIND:0xD4	2-110
PCIE_PRBS_ERRCNT_5	PCIEIND:0xD5	2-110
PCIE_PRBS_ERRCNT_6	PCIEIND:0xD6	2-110
PCIE_PRBS_ERRCNT_7	PCIEIND:0xD7	2-110
PCIE_PRBS_ERRCNT_8	PCIEIND:0xD8	2-111
PCIE_PRBS_ERRCNT_9	PCIEIND:0xD9	2-111
PCIE_PRBS_FREERUN	PCIEIND:0xCB	2-109
PCIE_PRBS_HI_BITCNT	PCIEIND:0xCF	2-109
PCIE_PRBS_LO_BITCNT	PCIEIND:0xCE	2-109
PCIE_PRBS_MISC	PCIEIND:0xCC	2-109
PCIE_PRBS_STATUS1	PCIEIND:0xC9	2-108
PCIE_PRBS_STATUS2	PCIEIND:0xCA	2-108
PCIE_PRBS_USER_PATTERN	PCIEIND:0xCD	2-109
PCIE_PREF_BASE_LIMIT	pcieConfigDev[13:2]:0x24	2-43
PCIE_PREF_BASE_UPPER	pcieConfigDev[13:2]:0x28	2-43
PCIE_PREF_LIMIT_UPPER	pcieConfigDev[13:2]:0x2C	2-43
PCIE_PROG_INTERFACE	pcieConfigDev[13:2]:0x9	2-41
PCIE_REG_R_RTR_TIMEOUT_CNTL	PCIEIND:0x17	2-98
PCIE_RESERVED	PCIEIND:0x0	2-95
PCIE_REVISION_ID	pcieConfigDev[13:2]:0x8	2-40
PCIE_ROOT_CAP	pcieConfigDev[13:2]:0x76	2-52
PCIE_ROOT_CNTL	pcieConfigDev[13:2]:0x74	2-52
PCIE_ROOT_ERR_CMD	pcieConfigDev[13:2]:0x17C	2-61
PCIE_ROOT_ERR_STATUS	pcieConfigDev[13:2]:0x180	2-61
PCIE_ROOT_STATUS	pcieConfigDev[13:2]:0x78	2-52
PCIE_RTR_CPL_TIMEOUT_STATUS	PCIEIND:0x13	2-97
PCIE_RX_CNTL	PCIEIND_P:0x70	2-119
PCIE_RX_CREDITS_ALLOCATED_CPL	PCIEIND_P:0x82	2-120
PCIE_RX_CREDITS_ALLOCATED_NP	PCIEIND_P:0x81	2-120
PCIE_RX_CREDITS_ALLOCATED_P	PCIEIND_P:0x80	2-120
PCIE_RX_CREDITS_RECEIVED_CPL	PCIEIND_P:0x85	2-121
PCIE_RX_CREDITS_RECEIVED_NP	PCIEIND_P:0x84	2-120
PCIE_RX_CREDITS_RECEIVED_P	PCIEIND_P:0x83	2-120
PCIE_RX_EXPECTED_SEQNUM	PCIEIND_P:0x71	2-119
PCIE_RX_LAST_TLP0	PCIEIND:0x31	2-101
PCIE_RX_LAST_TLP1	PCIEIND:0x32	2-102
PCIE_RX_LAST_TLP2	PCIEIND:0x33	2-102
PCIE_RX_LAST_TLP3	PCIEIND:0x34	2-102
PCIE_RX_NUM_NAK	PCIEIND:0xE	2-95
PCIE_RX_NUM_NAK_GENERATED	PCIEIND:0xF	2-95
PCIE_RX_VENDOR_SPECIFIC	PCIEIND_P:0x72	2-120
PCIE_SCRATCH	PCIEIND:0x1	2-95
PCIE_SECONDARY_STATUS	pcieConfigDev[13:2]:0x1E	2-42
PCIE_SLOT_CAP	pcieConfigDev[13:2]:0x6C	2-50
PCIE_SLOT_CAP2	pcieConfigDev[13:2]:0x8C	2-53
PCIE_SLOT_CNTL	pcieConfigDev[13:2]:0x70	2-51
PCIE_SLOT_CNTL2	pcieConfigDev[13:2]:0x90	2-53
PCIE_SLOT_STATUS	pcieConfigDev[13:2]:0x72	2-51
PCIE_SLOT_STATUS2	pcieConfigDev[13:2]:0x92	2-54

Table 2-1 Registers Sorted by Name (Continued)

Register Name	Address	Page
PCIE_SSID_CAP_LIST	pcieConfigDev[13:2]:0xB0	2-55
PCIE_SSID_ID	pcieConfigDev[13:2]:0xB4	2-55
PCIE_STATUS	pcieConfigDev[13:2]:0x6	2-40
PCIE_STRAP_I2C_BD	PCIEIND:0xC4	2-108
PCIE_STRAP_MISC	PCIEIND:0xC0	2-107
PCIE_STRAP_MISC2	PCIEIND:0xC1	2-107
PCIE_STRAP_PI	PCIEIND:0xC2	2-107
PCIE_SUB_BUS_NUMBER_LATENCY	pcieConfigDev[13:2]:0x18	2-42
PCIE_SUB_CLASS	pcieConfigDev[13:2]:0xA	2-41
PCIE_TX_ACK_LATENCY_LIMIT	PCIEIND_P:0x26	2-115
PCIE_TX_CNTL	PCIEIND_P:0x20	2-114
PCIE_TX_CREDITS_ADVT_CPL	PCIEIND_P:0x32	2-116
PCIE_TX_CREDITS_ADVT_NP	PCIEIND_P:0x31	2-116
PCIE_TX_CREDITS_ADVT_P	PCIEIND_P:0x30	2-116
PCIE_TX_CREDITS_FCU_THRESHOLD	PCIEIND_P:0x37	2-117
PCIE_TX_CREDITS_INIT_CPL	PCIEIND_P:0x35	2-116
PCIE_TX_CREDITS_INIT_NP	PCIEIND_P:0x34	2-116
PCIE_TX_CREDITS_INIT_P	PCIEIND_P:0x33	2-116
PCIE_TX_CREDITS_STATUS	PCIEIND_P:0x36	2-116
PCIE_TX_LAST_TLP0	PCIEIND:0x35	2-102
PCIE_TX_LAST_TLP1	PCIEIND:0x36	2-102
PCIE_TX_LAST_TLP2	PCIEIND:0x37	2-102
PCIE_TX_LAST_TLP3	PCIEIND:0x38	2-102
PCIE_TX_REPLAY	PCIEIND_P:0x25	2-115
PCIE_TX_REQUEST_NUM_CNTL	PCIEIND_P:0x23	2-115
PCIE_TX_REQUESTER_ID	PCIEIND_P:0x21	2-115
PCIE_TX_SEQ	PCIEIND_P:0x24	2-115
PCIE_TX_SLVCPL_NS_TIMEOUT_CNTL	PCIEIND:0x19	2-98
PCIE_TX_SLVCPL_TIMEOUT_CNTL	PCIEIND:0x18	2-98
PCIE_TX_VENDOR_SPECIFIC	PCIEIND_P:0x22	2-115
PCIE_UNCORR_ERR_MASK	pcieConfigDev[13:2]:0x158	2-59
PCIE_UNCORR_ERR_SEVERITY	pcieConfigDev[13:2]:0x15C	2-60
PCIE_UNCORR_ERR_STATUS	pcieConfigDev[13:2]:0x154	2-59
PCIE_VC_ENH_CAP_LIST	pcieConfigDev[13:2]:0x110	2-56
PCIE_VC0_RESOURCE_CAP	pcieConfigDev[13:2]:0x120	2-57
PCIE_VC0_RESOURCE_CNTL	pcieConfigDev[13:2]:0x124	2-57
PCIE_VC0_RESOURCE_STATUS	pcieConfigDev[13:2]:0x12A	2-58
PCIE_VC1_RESOURCE_CAP	pcieConfigDev[13:2]:0x12C	2-58
PCIE_VC1_RESOURCE_CNTL	pcieConfigDev[13:2]:0x130	2-58
PCIE_VC1_RESOURCE_STATUS	pcieConfigDev[13:2]:0x136	2-58
PCIE_VENDOR_ID	pcieConfigDev[13:2]:0x0	2-39
PCIE_VENDOR_SPECIFIC_ENH_CAP_LIST	pcieConfigDev[13:2]:0x100	2-56
PCIE_VENDOR_SPECIFIC_HDR	pcieConfigDev[13:2]:0x104	2-56
PCIE_VENDOR_SPECIFIC1	pcieConfigDev[13:2]:0x108	2-56
PCIE_VENDOR_SPECIFIC2	pcieConfigDev[13:2]:0x10C	2-56
PCIE_WPR_CNTL	PCIEIND:0x30	2-101
PCIEP_HW_DEBUG	PCIEIND_P:0x2	2-113
PCIEP_PORT_CNTL	PCIEIND_P:0x10	2-113
PCIEP_RESERVED	PCIEIND_P:0x0	2-113
PCIEP_SCRATCH	PCIEIND_P:0x1	2-113
PCIEP_STRAP_LC	PCIEIND_P:0xC0	2-130
PCIEP_STRAP_MISC	PCIEIND_P:0xC1	2-131
PLL_VOLTAGE_REG_CNTL	clkconfig:0x6C	2-69
PM1_STATUS	pmm2reg:0x4	2-80
PM2_CNTRL	pmm2reg:0x0	2-80
Receiver_Control_0	HTIUNBIND:0x1D	2-213
Receiver_Control_1	HTIUNBIND\:0x1E	2-215

Table 2-1 Registers Sorted by Name (Continued)

Register Name	Address	Page
Receiver_Control_2	HTIUNBIND:0x1F	2-215
Receiver_Control_3	HTIUNBIND:0x20	2-215
REDIRECTION_TABLE_ENTRY_HIGH_[31:0]	IOAPICMMISCIND\:0x11-0x4F	2-94
REDIRECTION_TABLE_ENTRY_LOW_[31:0]	IOAPICMMISCIND\:0x10-0x4E	2-94
SCRATCH_1_CLKCFG	clkconfig:0x78	2-70
SCRATCH_2_CLKCFG	clkconfig:0x7C	2-70
SCRATCH_4	HTIUNBIND:0x50	2-226
SCRATCH_5	HTIUNBIND:0x51	2-226
SCRATCH_6	HTIUNBIND:0x52	2-227
SCRATCH_7	HTIUNBIND:0x53	2-227
SCRATCH_8	HTIUNBIND:0x54	2-227
SCRATCH_9	HTIUNBIND:0x55	2-227
SCRATCH_A	HTIUNBIND:0x56	2-227
SCRATCH_CLKCFG	clkconfig:0x84	2-70
SCRATCH_NBCFG	nbconfig:0x78	2-14
SERR_PIN_CONTROL	NBMISCIND:0x77	2-186
StrapsOutputMux_0	NBMISCIND:0x70	2-184
StrapsOutputMux_1	NBMISCIND:0x71	2-184
StrapsOutputMux_2	NBMISCIND:0x72	2-184
StrapsOutputMux_3	NBMISCIND:0x73	2-184
StrapsOutputMux_4	NBMISCIND:0x64	2-177
StrapsOutputMux_5	NBMISCIND:0x65	2-178
StrapsOutputMux_6	NBMISCIND\:0x66	2-178
StrapsOutputMux_7	NBMISCIND\:0x67	2-179
StrapsOutputMux_8	NBMISCIND\:0x68	2-180
StrapsOutputMux_9	NBMISCIND\:0x69	2-181
StrapsOutputMux_A	NBMISCIND\:0x6A	2-181
StrapsOutputMux_B	NBMISCIND\:0x6B	2-181
StrapsOutputMux_C	NBMISCIND\:0x6C	2-182
StrapsOutputMux_D	NBMISCIND:0x6D	2-183
StrapsOutputMux_E	NBMISCIND:0x6E	2-183
StrapsOutputMux_F	NBMISCIND:0x6F	2-183
Transmiter_Control_0	HTIUNBIND:0x23	2-216
Transmitter_Control_1	HTIUNBIND:0x24	2-217
Transmitter_Control_2	HTIUNBIND:0x25	2-217
TX_B_P90PLL_IBias	HTIUNBIND:0x46	2-224

A.3 Registers Sorted by Address

Table 2-2 Registers Sorted by Address

Address	Register Name	Page
clkconfig:0x0	CLK_VENDOR_ID	2-64
clkconfig:0x14	CLK_BAR1_RCRB	2-66
clkconfig:0x2	CLK_DEVICE_ID	2-64
clkconfig:0x2C	CLK_ADAPTER_ID	2-66
clkconfig:0x34	CLK_CAPABILITIES_PTR	2-66
clkconfig:0x3C	CLK_INTERRUPT_LINE	2-66
clkconfig:0x3D	CLK_INTERRUPT_PIN	2-67
clkconfig:0x4	CLK_COMMAND	2-64
clkconfig:0x40	OSC_CONTROL	2-67
clkconfig:0x44	CPLL_CONTROL	2-67
clkconfig:0x4C	clk_top_pwm4_ctrl	2-68
clkconfig:0x50	clk_top_pwm5_ctrl	2-68
clkconfig:0x54	clk_top_pwm6_ctrl	2-68
clkconfig:0x58	MC_CLK_CNTRL	2-68
clkconfig:0x5C	DELAY_SET_IOC_CCLK	2-68
clkconfig:0x6	CLK_STATUS	2-64
clkconfig:0x60	MC_CLK_INDEX	2-68
clkconfig:0x64	MC_CLK_DATA	2-69
clkconfig:0x68	CT_DISABLE_BIU	2-69
clkconfig:0x6C	PLL_VOLTAGE_REG_CNTL	2-69
clkconfig:0x70	CPLL_CONTROL3	2-69
clkconfig:0x74	GC_CLK_CNTRL	2-70
clkconfig:0x78	SCRATCH_1_CLKCFG	2-70
clkconfig:0x7C	SCRATCH_2_CLKCFG	2-70
clkconfig:0x8	CLK_REVISION_ID	2-65
clkconfig:0x80	MC_DATA_DLL_CNTRL_A	2-70
clkconfig:0x84	SCRATCH_CLKCFG	2-70
clkconfig:0x88	MC_ACMD_DLL_CNTRL_A	2-71
clkconfig:0x89	MC_ACMD_DLL_CNTRL_B	2-71
clkconfig:0x8C	CLKGATE_DISABLE2	2-71
clkconfig:0x9	CLK_REGPROG_INF	2-65
clkconfig:0x94	CLKGATE_DISABLE	2-71
clkconfig:0x98	CPLL_CONTROL2	2-73
clkconfig:0xA	CLK_SUB_CLASS	2-65
clkconfig:0xB	CLK_BASE_CODE	2-65
clkconfig:0xB0	clk_top_pwm1_ctrl	2-74
clkconfig:0xB4	clk_top_pwm2_ctrl	2-74
clkconfig:0xB8	clk_top_test_ctrl	2-74
clkconfig:0xBC	NBCLK_IO_CONTROL	2-74
clkconfig:0xC	CLK_CACHE_LINE	2-65
clkconfig:0xC0	CLK_TOP_THERMAL_ALERT_INTR_EN	2-75
clkconfig:0xC4	CLK_TOP_THERMAL_ALERT_STATUS	2-75
clkconfig:0xC8	CLK_TOP_THERMAL_ALERT_WAIT_WINDOW	2-75
clkconfig:0xCC	clk_top_pwm3_ctrl	2-75
clkconfig:0xD	CLK_LATENCY	2-66
clkconfig:0xD0	clk_top_spare_pll	2-75
clkconfig:0xD4	CLK_CFG_HTPLL_CNTL	2-76
clkconfig:0xD8	CLK_HTPLL_CONTROL	2-76
clkconfig:0xDC	GPIO_ctrl	2-76
clkconfig:0xE	CLK_HEADER	2-66
clkconfig:0xE0	CLK_TOP_SPARE_A	2-77
clkconfig:0xE4	CLK_TOP_SPARE_B	2-77
clkconfig:0xE8	CLK_TOP_SPARE_C	2-77
clkconfig:0xEC	CLK_TOP_SPARE_D	2-78

Table 2-2 Registers Sorted by Address (Continued)

Address	Register Name	Page
clkconfig:0xF	CLK_BIST	2-66
clkconfig:0xF8	CFG_CT_CLKGATE_HTIU	2-78
clkconfig\:0x90	HOTPLUG_BLINK_RATE	2-71
clkconfig\:0x9C	PCIE_DEVICE_SERIAL_NO_0	2-74
clkconfig\:0xA0	PCIE_DEVICE_SERIAL_NO_1	2-74
clkconfig\:0xF0	HOTPLUG_SPARE_0	2-78
clkconfig\:0xF4	HOTPLUG_SPARE_1	2-78
HTIUNBIND:0x0	NB_HT_CLK_CNTL_RECEIVER_COMP_CNTL	2-206
HTIUNBIND:0x1	NB_HT_TRANS_COMP_CNTL	2-206
HTIUNBIND:0x10	HTIU_STATUS_0	2-210
HTIUNBIND:0x11	HTIU_SCRATCH_2	2-210
HTIUNBIND:0x12	HTIU_SCRATCH_3	2-210
HTIUNBIND:0x13	HTIU_SCRATCH_4	2-210
HTIUNBIND:0x14	HTIU_SCRATCH_5	2-210
HTIUNBIND:0x15	Link_State_Control_0	2-210
HTIUNBIND:0x16	Link_State_Control_1	2-211
HTIUNBIND:0x17	Link_State_Control_2	2-212
HTIUNBIND:0x18	Link_State_Control_3	2-212
HTIUNBIND:0x19	Link_State_Control_4	2-212
HTIUNBIND:0x1A	Link_State_Control_5	2-212
HTIUNBIND:0x1B	Link_State_Control_6	2-212
HTIUNBIND:0x1C	Link_State_Control_7	2-213
HTIUNBIND:0x1D	Receiver_Control_0	2-213
HTIUNBIND:0x1F	Receiver_Control_2	2-215
HTIUNBIND:0x20	Receiver_Control_3	2-215
HTIUNBIND:0x21	HT_BIST_Extended_Control_0	2-216
HTIUNBIND:0x22	HT_BIST_Extended_Control_1	2-216
HTIUNBIND:0x23	Transmiter_Control_0	2-216
HTIUNBIND:0x24	Transmitter_Control_1	2-217
HTIUNBIND:0x25	Transmitter_Control_2	2-217
HTIUNBIND:0x26	HT3PHY_CNTL_1	2-217
HTIUNBIND:0x27	HT3PHY_CNTL_2	2-218
HTIUNBIND:0x28	HT3PHY_CNTL_3	2-218
HTIUNBIND:0x29	HT3PHY_CNTL_4	2-219
HTIUNBIND:0x2A	HT3PHY_CNTL_5	2-219
HTIUNBIND:0x2B	HT3PHY_CNTL_6	2-219
HTIUNBIND:0x2C	CFG_HT_DIV_CTRL	2-220
HTIUNBIND:0x2E	HTIU_IOMMU_CONTROL_0	2-220
HTIUNBIND:0x2F	HTIU_IOMMU_CONTROL_1	2-220
HTIUNBIND:0x30	NB_LOWER_TOP_OF_DRAM2	2-220
HTIUNBIND:0x31	NB_UPPER_TOP_OF_DRAM2	2-220
HTIUNBIND:0x32	NB_HTIU_CFG	2-221
HTIUNBIND:0x33	HT3PHY_CNTL_15	2-221
HTIUNBIND:0x38	HTIU_TAG_XTL_CONTROL_0	2-221
HTIUNBIND:0x39	HTIU_TAG_XTL_CONTROL_1	2-221
HTIUNBIND:0x3A	HTIU_PCIE_ERR_FLOOD_CONTROL_0	2-221
HTIUNBIND:0x3B	HTIU_PCIE_ERR_FLOOD_CONTROL_1	2-222
HTIUNBIND:0x40	LS_History0	2-222
HTIUNBIND:0x41	LS_History1	2-223
HTIUNBIND:0x42	LS_History2	2-223
HTIUNBIND:0x43	LS_History3	2-223
HTIUNBIND:0x44	LS_History4	2-223
HTIUNBIND:0x45	LS_History5	2-224
HTIUNBIND:0x46	TX_B_P90PLL_IBias	2-224
HTIUNBIND:0x5	HTIU_DEBUG	2-207
HTIUNBIND:0x50	SCRATCH_4	2-226
HTIUNBIND:0x51	SCRATCH_5	2-226

Table 2-2 Registers Sorted by Address (Continued)

Address	Register Name	Page
HTIUNBIND:0x52	SCRATCH_6	2-227
HTIUNBIND:0x53	SCRATCH_7	2-227
HTIUNBIND:0x54	SCRATCH_8	2-227
HTIUNBIND:0x55	SCRATCH_9	2-227
HTIUNBIND:0x56	SCRATCH_A	2-227
HTIUNBIND:0x6	HTIU_DOWNSTREAM_CONFIG	2-207
HTIUNBIND:0x77	HTIU_UPSTREAM_ARB_CONTROL_8	2-227
HTIUNBIND:0x78	HTIU_ILA_CONTROL_0	2-227
HTIUNBIND:0x79	HTIU_ILA_CONTROL_1	2-228
HTIUNBIND:0x7A	HTIU_ILA_CONTROL_2	2-228
HTIUNBIND:0x7B	HTIU_ILA_CONTROL_3	2-228
HTIUNBIND:0x7C	HTIU_ILA_CONTROL_4	2-228
HTIUNBIND:0x7D	HTIU_ILA_CONTROL_5	2-228
HTIUNBIND:0x81	PARITY_ERROR_STATUS_0	2-229
HTIUNBIND:0x82	PARITY_ERROR_STATUS_1	2-229
HTIUNBIND:0x83	PARITY_ERROR_STATUS_2	2-230
HTIUNBIND:0x84	PARITY_ERROR_STATUS_3	2-230
HTIUNBIND:0x85	PARITY_ERROR_STATUS_4	2-230
HTIUNBIND:0x86	PARITY_ERROR_STATUS_5	2-230
HTIUNBIND:0x87	PARITY_ERROR_STATUS_6	2-230
HTIUNBIND:0x88	PARITY_ERROR_STATUS_7	2-230
HTIUNBIND:0x89	PARITY_ERROR_STATUS_8	2-230
HTIUNBIND:0x8A	PARITY_ERROR_STATUS_9	2-231
HTIUNBIND:0x8B	PARITY_ERROR_STATUS_10	2-231
HTIUNBIND:0x8C	PARITY_ERROR_STATUS_11	2-231
HTIUNBIND:0x8D	PARITY_ERROR_STATUS_12	2-231
HTIUNBIND:0x8E	PARITY_ERROR_STATUS_13	2-231
HTIUNBIND:0x8F	PARITY_ERROR_STATUS_14	2-231
HTIUNBIND:0x90	PARITY_ERROR_STATUS_15	2-231
HTIUNBIND:0x91	PARITY_ERROR_STATUS_16	2-232
HTIUNBIND:0x92	PARITY_ERROR_STATUS_17	2-232
HTIUNBIND:0x93	PARITY_ERROR_STATUS_18	2-232
HTIUNBIND:0x94	PARITY_ERROR_STATUS_19	2-232
HTIUNBIND:0x95	PARITY_ERROR_STATUS_20	2-232
HTIUNBIND:0x96	PARITY_ERROR_STATUS_21	2-232
HTIUNBIND:0x97	PARITY_ERROR_STATUS_22	2-232
HTIUNBIND:0x98	PARITY_ERROR_STATUS_23	2-233
HTIUNBIND:0x99	PARITY_ERROR_STATUS_24	2-233
HTIUNBIND:0x9A	PARITY_ERROR_STATUS_25	2-233
HTIUNBIND:0xF	HTIU_SCRATCH_0	2-210
HTIUNBIND\:0x1E	Receiver_Control_1	2-215
HTIUNBIND\:0x33	HT3PHY_CNTL_15	2-226
HTIUNBIND\:0x47	HT3PHY_CNTL_8	2-224
HTIUNBIND\:0x48	HT3PHY_CNTL_9	2-224
HTIUNBIND\:0x49	HT3PHY_CNTL_10	2-225
HTIUNBIND\:0x4A	HT3PHY_CNTL_11	2-225
HTIUNBIND\:0x4B	HT3PHY_CNTL_12	2-225
HTIUNBIND\:0x4C	HT3PHY_CNTL_13	2-225
HTIUNBIND\:0x4D	HT3PHY_CNTL_14	2-226
HTIUNBIND\:0x7	HTIU_UPSTREAM_ARB_CONTROL_0	2-208
HTIUNBIND\:0x7E	HT_ERROR_INJECTION_CNTL	2-228
HTIUNBIND\:0x8	HTIU_UPSTREAM_ARB_CONTROL_1	2-209
HTIUNBIND\:0x80	PARITY_ERROR_INJECTION_CNTL	2-229
HTIUNBIND\:0x9	HTIU_UPSTREAM_ARB_CONTROL_2	2-209
HTIUNBIND\:0xA	HTIU_UPSTREAM_ARB_CONTROL_3	2-209
HTIUNBIND\:0xA4	GPIO_1_4	2-233
HTIUNBIND\:0xA5	GPIO_5_8	2-234

Table 2-2 Registers Sorted by Address (Continued)

Address	Register Name	Page
HTIUNBIND\:0xA6	GPIO_9_12	2-236
HTIUNBIND\:0xA7	GPIO_13_16	2-237
HTIUNBIND\:0xA8	GPIO_17_20	2-239
HTIUNBIND\:0xA9	GPIO_21_24	2-240
HTIUNBIND\:0xAA	GPIO_CNTL_1_24	2-241
HTIUNBIND\:0xB	HTIU_UPSTREAM_ARB_CONTROL_4	2-209
HTIUNBIND\:0xC	HTIU_UPSTREAM_ARB_CONTROL_5	2-209
HTIUNBIND\:0xD	HTIU_UPSTREAM_ARB_CONTROL_6	2-209
IOAPICCMISCIND\:0x0	FEATURES_ENABLE	2-89
IOAPICCMISCIND\:0x1	IOAPIC_CONF_LOWER	2-89
IOAPICCMISCIND\:0x2	IOAPIC_CONF_UPPER	2-89
IOAPICCMISCIND\:0x3	IOAPIC_INT_ROUTING_REGISTER1	2-89
IOAPICCMISCIND\:0x4	IOAPIC_INT_ROUTING_REGISTER2	2-90
IOAPICCMISCIND\:0x5	IOAPIC_INT_ROUTING_REGISTER3	2-90
IOAPICCMISCIND\:0x6	IOAPIC_INT_ROUTING_REGISTER4	2-90
IOAPICCMISCIND\:0x7	IOAPIC_INT_ROUTING_REGISTER5	2-91
IOAPICCMISCIND\:0x8	IOAPIC_INT_ROUTING_REGISTER6	2-91
IOAPICCMISCIND\:0x9	IOAPIC_INT_ROUTING_REGISTER7	2-91
IOAPICCMISCIND\:0xA	IOAPIC_SERIAL_IRQ_STATUS	2-92
IOAPICMMISCIND\:0x0	IOAPIC_ID_REGISTER	2-93
IOAPICMMISCIND\:0x1	IOAPIC_VERSION_REGISTER	2-93
IOAPICMMISCIND\:0x10-0x4E	REDIRECTION_TABLE_ENTRY_LOW_[31:0]	2-94
IOAPICMMISCIND\:0x11-0x4F	REDIRECTION_TABLE_ENTRY_HIGH_[31:0]	2-94
IOAPICMMISCIND\:0x2	IOAPIC_ARBITRATION_REGISTER	2-93
ioapicmmreg\:0x0	IO_REGISTER_SELECT_INDEX	2-88
ioapicmmreg\:0x10	IO_WINDOW_REGISTER_DATA	2-88
ioapicmmreg\:0x20	IRQ_PIN_ASSERTION_REGISTER	2-88
ioapicmmreg\:0x40	EOI_REGISTER	2-88
iommummreg:0x0	IOMMU_MMIO_DEVTBL_BASE_0	2-81
iommummreg:0x10	IOMMU_MMIO_EVENT_BASE_0	2-82
iommummreg:0x14	IOMMU_MMIO_EVENT_BASE_1	2-82
iommummreg:0x18	IOMMU_MMIO_CNTRL_0	2-82
iommummreg:0x1C	IOMMU_MMIO_CNTRL_1	2-84
iommummreg:0x20	IOMMU_MMIO_EXCL_BASE_0	2-84
iommummreg:0x2000	IOMMU_MMIO_CMD_BUF_HDPTR_0	2-85
iommummreg:0x2004	IOMMU_MMIO_CMD_BUF_HDPTR_1	2-85
iommummreg:0x2008	IOMMU_MMIO_CMD_BUF_TAILPTR_0	2-85
iommummreg:0x200C	IOMMU_MMIO_CMD_BUF_TAILPTR_1	2-86
iommummreg:0x2010	IOMMU_MMIO_EVENT_BUF_HDPTR_0	2-86
iommummreg:0x2014	IOMMU_MMIO_EVENT_BUF_HDPTR_1	2-86
iommummreg:0x2018	IOMMU_MMIO_EVENT_BUF_TAILPTR_0	2-86
iommummreg:0x201C	IOMMU_MMIO_EVENT_BUF_TAILPTR_1	2-87
iommummreg:0x2020	IOMMU_MMIO_STATUS_0	2-87
iommummreg:0x2024	IOMMU_MMIO_STATUS_1	2-87
iommummreg:0x24	IOMMU_MMIO_EXCL_BASE_1	2-84
iommummreg:0x28	IOMMU_MMIO_EXCL_LIM_0	2-85
iommummreg:0x2C	IOMMU_MMIO_EXCL_LIM_1	2-85
iommummreg:0x4	IOMMU_MMIO_DEVTBL_BASE_1	2-81
iommummreg:0x8	IOMMU_MMIO_CMD_BASE_0	2-81
iommummreg:0xC	IOMMU_MMIO_CMD_BASE_1	2-81
L1CFGIND:0x10	L1_BANK_SEL_0	2-191
L1CFGIND:0x11	L1_BANK_DISABLE_0	2-191
L1CFGIND:0x20	L1_WQ_STATUS_0	2-191
L1CFGIND:0x21	L1_WQ_STATUS_1	2-191
L1CFGIND:0x22	L1_WQ_STATUS_2	2-192
L1CFGIND:0x23	L1_WQ_STATUS_3	2-192
L1CFGIND:0x6	L1_DEBUG_0	2-189

Table 2-2 Registers Sorted by Address (Continued)

Address	Register Name	Page
L1CFGIND:0x7	L1_DEBUG_1	2-189
L1CFGIND:0x8	L1_DEBUG_STATUS	2-189
L1CFGIND:0xC	L1_CNTRL_0	2-189
L1CFGIND\:0xD	L1_CNTRL_1	2-190
L1CFGIND\:0xE	L1_CNTRL_2	2-190
L1CFGIND\:0xF	L1_CNTRL_3	2-191
L2CFGIND:0x10	L2_DTC_CONTROL	2-195
L2CFGIND:0x11	L2_DTC_HASH_CONTROL	2-195
L2CFGIND:0x12	L2_DTC_WAY_CONTROL	2-196
L2CFGIND:0x14	L2_ITC_CONTROL	2-196
L2CFGIND:0x15	L2_ITC_HASH_CONTROL	2-196
L2CFGIND:0x16	L2_ITC_WAY_CONTROL	2-197
L2CFGIND:0x18	L2_PTC_A_CONTROL	2-197
L2CFGIND:0x19	L2_PTC_A_HASH_CONTROL	2-197
L2CFGIND:0x1A	L2_PTC_A_WAY_CONTROL	2-198
L2CFGIND:0x1C	L2_PTC_B_CONTROL	2-198
L2CFGIND:0x1D	L2_PTC_B_HASH_CONTROL	2-198
L2CFGIND:0x1E	L2_PTC_B_WAY_CONTROL	2-199
L2CFGIND:0x43	L2_DEBUG_2	2-199
L2CFGIND:0x44	L2_DEBUG_3	2-200
L2CFGIND:0x45	L2_STATUS_1	2-200
L2CFGIND:0x50	L2_PDC_CONTROL	2-201
L2CFGIND:0x51	L2_PDC_HASH_CONTROL	2-202
L2CFGIND:0x52	L2_PDC_WAY_CONTROL	2-202
L2CFGIND:0x54	L2_TW_CONTROL	2-202
L2CFGIND:0x6	L2_DEBUG_0	2-193
L2CFGIND:0x7	L2_DEBUG_1	2-193
L2CFGIND:0x8	L2_STATUS_0	2-193
L2CFGIND:0xC	L2_CONTROL_0	2-194
L2CFGIND\:0x20	L2_CREDIT_CONTROL_2	2-199
L2CFGIND\:0x30	L2_ERR_RULE_CONTROL_3	2-199
L2CFGIND\:0x31	L2_ERR_RULE_CONTROL_4	2-199
L2CFGIND\:0x32	L2_ERR_RULE_CONTROL_5	2-199
L2CFGIND\:0x4C	L2_CONTROL_5	2-200
L2CFGIND\:0x4D	L2_CONTROL_6	2-201
L2CFGIND\:0x56	L2_CP_CONTROL	2-202
L2CFGIND\:0x60	L2_TW_CONTROL_1	2-203
L2CFGIND\:0x61	L2_TW_CONTROL_2	2-203
L2CFGIND\:0x62	L2_TW_CONTROL_3	2-203
L2CFGIND\:0x6A	L2_INT_CONTROL	2-203
L2CFGIND\:0x70	L2_CREDIT_CONTROL_0	2-203
L2CFGIND\:0x71	L2_CREDIT_CONTROL_1	2-204
L2CFGIND\:0x78	L2_MCIF_CONTROL	2-204
L2CFGIND\:0x80	L2_ERR_RULE_CONTROL_0	2-204
L2CFGIND\:0x81	L2_ERR_RULE_CONTROL_1	2-204
L2CFGIND\:0x82	L2_ERR_RULE_CONTROL_2	2-205
L2CFGIND\:0xC	L2_CONTROL_0	2-193
L2CFGIND\:0xD	L2_CONTROL_1	2-195
nbconfig:0x0	NB_VENDOR_ID	2-4
nbconfig:0x14	NB_BAR1_RCRB	2-7
nbconfig:0x18	NB_BAR2_PM2	2-7
nbconfig:0x1C	NB_BAR3_PCIEXP_MMCFG	2-8
nbconfig:0x2	NB_DEVICE_ID	2-4
nbconfig:0x20	NB_BAR3_UPPER_PCIEXP_MMCFG	2-8
nbconfig:0x2C	NB_ADAPTER_ID	1-1
nbconfig:0x2C	NB_ADAPTER_ID	2-8
nbconfig:0x34	NB_CAPABILITIES_PTR	2-8

Table 2-2 Registers Sorted by Address (Continued)

Address	Register Name	Page
nbconfig:0x3C	NB_INTERRUPT_LINE	2-8
nbconfig:0x3D	NB_INTERRUPT_PIN	2-9
nbconfig:0x4	NB_COMMAND	2-4
nbconfig:0x40	NB_HT_ERROR_RETRY_CAPABILITY	2-9
nbconfig:0x44	NB_HT_ERROR_RETRY_CONTROL_STATUS	2-9
nbconfig:0x48	NB_HT_ERROR_RETRY_COUNT	2-9
nbconfig:0x4C	NB_PCI_CTRL	2-10
nbconfig:0x50	NB_ADAPTER_ID_W	2-11
nbconfig:0x54	NB_UNITID_CLUMPING_CAPABILITY	2-11
nbconfig:0x58	NB_UNITID_CLUMPING_SUPPORT	2-12
nbconfig:0x5C	NB_UNITID_CLUMPING_ENABLE	2-12
nbconfig:0x6	NB_STATUS	2-5
nbconfig:0x60	NB_MISC_INDEX	2-12
nbconfig:0x64	NB_MISC_DATA	2-12
nbconfig:0x68	HT_PARITY_ERR_CONTROL_STATUS	2-12
nbconfig:0x70	MSI_CAPABILITY_POINTER_0	2-14
nbconfig:0x74	MSI_CAPABILITY_POINTER_1	2-14
nbconfig:0x78	MSI_CAPABILITY_POINTER_2	2-14
nbconfig:0x78	SCRATCH_NBCFG	2-14
nbconfig:0x7C	NB_IOC_CFG_CNTL	2-14
nbconfig:0x8	NB_REVISION_ID	2-6
nbconfig:0x84	NB_PCI_ARB	2-15
nbconfig:0x88	NB_CFG_STAT	2-16
nbconfig:0x9	NB_REGPROG_INF	2-6
nbconfig:0x90	NB_TOP_OF_DRAM_SLOT1	2-17
nbconfig:0x94	HTIU_NB_INDEX	2-17
nbconfig:0x98	HTIU_NB_DATA	2-17
nbconfig:0x9C	NB_HT3_CAPABILITY	2-17
nbconfig:0xA	NB_SUB_CLASS	2-6
nbconfig:0xA0	NB_HT3_GLOBAL_LINK_TRAIN	2-17
nbconfig:0xA4	NB_HT3_LINK_TRANSMITTER_CONF_0	2-19
nbconfig:0xA8	NB_HT3_LINK_RECEIVER_CONF_0	2-20
nbconfig:0xAC	NB_HT3_LINK_TRAINING_0	2-21
nbconfig:0xB	NB_BASE_CODE	2-6
nbconfig:0xB0	NB_HT3_LINK_FREQUENCY_EXTENSION	2-22
nbconfig:0xB4	NB_HT3_LINK_TRANSMITTER_CONF_1	2-23
nbconfig:0xB8	NB_HT3_LINK_RECEIVER_CONF_1	2-23
nbconfig:0xBC	NB_HT3_LINK_TRAINING_1	2-24
nbconfig:0xC	NB_CACHE_LINE	2-6
nbconfig:0xC0	NB_HT3_BIST_CONTROL	2-25
nbconfig:0xC4	NB_HT_LINK_COMMAND	2-25
nbconfig:0xCC	NB_HT_LINK_END	2-27
nbconfig:0xD	NB_LATENCY	2-6
nbconfig:0xD0	NB_HT_LINK_FREQ_CAP_A	2-27
nbconfig:0xD4	NB_HT_LINK_FREQ_CAP_B	2-28
nbconfig:0xD8	NB_HT_ENUMERATION_SCRATCHPAD	2-29
nbconfig:0xDC	NB_HT_MEMORY_BASE_UPPER	2-29
nbconfig:0xE	NB_HEADER	2-6
nbconfig:0xE0	NB_PCIE_INDX_ADDR	2-29
nbconfig:0xE4	NB_PCIE_INDX_DATA	2-30
nbconfig:0xF	NB_BIST	2-7
nbconfig:0xF0	MSI_MAPPING_CAPABILITY	2-30
nbconfig\:0xC8	NB_HT_LINK_CONF_CNTL	2-26
nbconfig\:0xF8	IOAPIC_INDEX	2-30
nbconfig\:0xFC	IOAPIC_DATA	2-30
nbconfigfunc2:0x0	IOMMU_VENDOR_ID	2-31
nbconfigfunc2:0x2	IOMMU_DEVICE_ID	2-31

Table 2-2 Registers Sorted by Address (Continued)

Address	Register Name	Page
nbconfigfunc2:0x2C	IOMMU_ADAPTER_ID	2-34
nbconfigfunc2:0x34	IOMMU_CAPABILITIES_PTR	2-34
nbconfigfunc2:0x3C	IOMMU_INTERRUPT_LINE	2-34
nbconfigfunc2:0x3D	IOMMU_INTERRUPT_PIN	2-34
nbconfigfunc2:0x4	IOMMU_COMMAND	2-31
nbconfigfunc2:0x40	IOMMU_CAP_HEADER	2-34
nbconfigfunc2:0x44	IOMMU_CAP_BASE_LO	2-35
nbconfigfunc2:0x48	IOMMU_CAP_BASE_HI	2-35
nbconfigfunc2:0x4C	IOMMU_CAP_RANGE	2-35
nbconfigfunc2:0x50	IOMMU_CAP_MISC	2-35
nbconfigfunc2:0x54	IOMMU_MSI_CAP	2-36
nbconfigfunc2:0x58	IOMMU_MSI_ADDR_LO	2-36
nbconfigfunc2:0x5C	IOMMU_MSI_ADDR_HI	2-36
nbconfigfunc2:0x6	IOMMU_STATUS	2-32
nbconfigfunc2:0x60	IOMMU_MSI_DATA	2-36
nbconfigfunc2:0x64	IOMMU_MSI_MAPPING_CAP	2-37
nbconfigfunc2:0x68	IOMMU_ADAPTER_ID_W	2-37
nbconfigfunc2:0x6C	IOMMU_CONTROL_W	2-37
nbconfigfunc2:0x8	IOMMU_REVISION_ID	2-33
nbconfigfunc2:0x9	IOMMU_REGPROG_INF	2-33
nbconfigfunc2:0xA	IOMMU_SUB_CLASS	2-33
nbconfigfunc2:0xB	IOMMU_BASE_CODE	2-33
nbconfigfunc2:0xC	IOMMU_CACHE_LINE	2-33
nbconfigfunc2:0xD	IOMMU_LATENCY	2-33
nbconfigfunc2:0xE	IOMMU_HEADER	2-33
nbconfigfunc2:0xF	IOMMU_BIST	2-34
nbconfigfunc2:0xF0	L2CFG_INDEX	2-37
nbconfigfunc2:0xF4	L2CFG_DATA	2-37
nbconfigfunc2:0xF8	L1CFG_INDEX	2-38
nbconfigfunc2:0xFC	L1CFG_DATA	2-38
NBMISCIND:0x0	NB_CNTL	2-132
NBMISCIND:0x1	NB_IOC_DEBUG	2-132
NBMISCIND:0x10	DFT_CNTL2	2-139
NBMISCIND:0x11	NB_BUS_NUM_CNTL	2-139
NBMISCIND:0x12	PCIE_CORE_ARB	2-139
NBMISCIND:0x16	NB_TOM_PCI	2-140
NBMISCIND:0x17	NB_MMIOBASE	2-140
NBMISCIND:0x18	NB_MMIOLIMIT	2-140
NBMISCIND:0x19	PCIE_NBCFG_REG17	2-140
NBMISCIND:0x1A	PCIE_NBCFG_REG18	2-141
NBMISCIND:0x1B	PCIE_NBCFG_REG19	2-142
NBMISCIND:0x1C	DFT_CNTL4	2-142
NBMISCIND:0x1D	DFT_CNTL5	2-143
NBMISCIND:0x1E	IOC_PCIE_D13_CSR_Count	2-143
NBMISCIND:0x1F	IOC_PCIE_D13_CNTL	2-143
NBMISCIND:0x2	NB_SPARE1	2-133
NBMISCIND:0x20	NB_PROG_DEVICE_REMAP_0	2-144
NBMISCIND:0x21	NB_PROG_DEVICE_REMAP_1	2-144
NBMISCIND:0x22	PCIE_NBCFG_REGA	2-144
NBMISCIND:0x23	PCIE_NBCFG_REGB	2-144
NBMISCIND:0x24	PCIE_NBCFG_REGC	2-145
NBMISCIND:0x25	PCIE_NBCFG_REGD	2-146
NBMISCIND:0x26	PCIE_NBCFG_REGE	2-147
NBMISCIND:0x27	PCIE_NBCFG_REGF	2-148
NBMISCIND:0x28	PCIE_NBCFG_REG10	2-149
NBMISCIND:0x29	PCIE_NBCFG_REG11	2-151
NBMISCIND:0x2A	PCIE_NBCFG_REG12	2-151

Table 2-2 Registers Sorted by Address (Continued)

Address	Register Name	Page
NBMISCIND:0x2B	PCIE_NBCFG_REG13	2-152
NBMISCIND:0x2C	PCIE_NBCFG_REG14	2-153
NBMISCIND:0x2D	PCIE_NBCFG_REG15	2-154
NBMISCIND:0x2E	PCIE_NBCFG_REG16	2-154
NBMISCIND:0x2F	PCIE_GFX2_P2P_ARBITRER_CONTROL	2-155
NBMISCIND:0x3	NB_STRAPS_READBACK_MUX	2-133
NBMISCIND:0x32	PCIE_NBCFG_REG2	2-156
NBMISCIND:0x33	PCIE_NBCFG_REG3	2-156
NBMISCIND:0x34	PCIE_NBCFG_REG4	2-158
NBMISCIND:0x35	PCIE_NBCFG_REG5	2-159
NBMISCIND:0x36	PCIE_NBCFG_REG6	2-160
NBMISCIND:0x37	PCIE_NBCFG_REG7	2-160
NBMISCIND:0x38	PCIE_NBCFG_REG8	2-161
NBMISCIND:0x39	PCIE_NBCFG_REG9	2-161
NBMISCIND:0x3A	NB_BROADCAST_BASE_LO	2-162
NBMISCIND:0x3B	NB_BROADCAST_BASE_HI	2-162
NBMISCIND:0x3C	NB_BROADCAST_CNTL	2-162
NBMISCIND:0x3D	NB_APIC_P2P_CNTL	2-162
NBMISCIND:0x3E	NB_APIC_P2P_RANGE_0	2-164
NBMISCIND:0x3F	NB_APIC_P2P_RANGE_1	2-164
NBMISCIND:0x4	NB_STRAPS_READBACK_DATA	2-133
NBMISCIND:0x40	NB_APIC_P2P_RANGE_2	2-164
NBMISCIND:0x41	GPIO_PAD_CNTL_PU_PD	2-164
NBMISCIND:0x42	GPIO_PAD_SCHMEM_OE	2-165
NBMISCIND:0x46	GPIO_PAD	2-167
NBMISCIND:0x47	IOC_JTAG_CNTL	2-167
NBMISCIND:0x48	PCIE_GFX_P2P_CONTROL	2-167
NBMISCIND:0x49	PCIE_GFX_P2P_ARBITRER_CONTROL	2-168
NBMISCIND:0x4A	EFUSE_CFG_HW_CONFIG_4	2-168
NBMISCIND:0x4E	CFG_IOC_TOM3	2-168
NBMISCIND:0x5	DFT_CNTL0	2-133
NBMISCIND:0x50	IOC_PCIE_D2_CSR_Count	2-169
NBMISCIND:0x51	IOC_PCIE_D2_CNTL	2-169
NBMISCIND:0x52	IOC_PCIE_D3_CSR_Count	2-169
NBMISCIND:0x53	IOC_PCIE_D3_CNTL	2-170
NBMISCIND:0x54	IOC_PCIE_D4_CSR_Count	2-170
NBMISCIND:0x55	IOC_PCIE_D4_CNTL	2-171
NBMISCIND:0x56	IOC_PCIE_D5_CSR_Count	2-171
NBMISCIND:0x57	IOC_PCIE_D5_CNTL	2-171
NBMISCIND:0x58	IOC_PCIE_D6_CSR_Count	2-172
NBMISCIND:0x59	IOC_PCIE_D6_CNTL	2-172
NBMISCIND:0x5A	IOC_PCIE_D7_CSR_Count	2-173
NBMISCIND:0x5B	IOC_PCIE_D7_CNTL	2-173
NBMISCIND:0x5C	IOC_PCIE_D9_CSR_Count	2-174
NBMISCIND:0x5D	IOC_PCIE_D9_CNTL	2-174
NBMISCIND:0x5E	IOC_PCIE_D10_CSR_Count	2-175
NBMISCIND:0x5F	IOC_PCIE_D10_CNTL	2-175
NBMISCIND:0x6	DFT_CNTL1	2-133
NBMISCIND:0x60	IOC_PCIE_D11_CSR_Count	2-176
NBMISCIND:0x61	IOC_PCIE_D11_CNTL	2-176
NBMISCIND:0x62	IOC_PCIE_D12_CSR_Count	2-177
NBMISCIND:0x63	IOC_PCIE_D12_CNTL	2-177
NBMISCIND:0x64	StrapsOutputMux_4	2-177
NBMISCIND:0x65	StrapsOutputMux_5	2-178
NBMISCIND:0x6D	StrapsOutputMux_D	2-183
NBMISCIND:0x6E	StrapsOutputMux_E	2-183

Table 2-2 Registers Sorted by Address (Continued)

Address	Register Name	Page
NBMISCIND:0x6F	StrapsOutputMux_F	2-183
NBMISCIND:0x7	PCIE_PDNB_CNTL	2-134
NBMISCIND:0x70	StrapsOutputMux_0	2-184
NBMISCIND:0x71	StrapsOutputMux_1	2-184
NBMISCIND:0x72	StrapsOutputMux_2	2-184
NBMISCIND:0x73	StrapsOutputMux_3	2-184
NBMISCIND:0x74	PCIE_CORE_ARB_2	2-184
NBMISCIND:0x76	MMIO_BASE_LIMIT_UPPER	2-185
NBMISCIND:0x77	SERR_PIN_CONTROL	2-186
NBMISCIND:0x78	FATAL_PIN_CONTROL	2-186
NBMISCIND:0x79	NON_FATAL_PIN_CONTROL	2-187
NBMISCIND:0x7A	CORR_PIN_CONTROL	2-187
NBMISCIND:0x7B	DFT_CNTL3	2-188
NBMISCIND:0x7F	DFT_SPARE	2-188
NBMISCIND:0x8	PCIE_LINK_CFG	2-134
NBMISCIND:0x9	IOC_DMA_ARBITER	2-136
NBMISCIND:0xA	IOC_PCIE_CSR_Count	2-136
NBMISCIND:0xB	IOC_PCIE_CNTL	2-136
NBMISCIND:0xC	IOC_P2P_CNTL	2-137
NBMISCIND:0xE	IOCIsocMapAddr_LO	2-139
NBMISCIND:0xF	IOCIsocMapAddr_HI	2-139
NBMISCIND\:0x43	GPIO_PAD_SP_SN	2-166
NBMISCIND\:0x4F	PCIE_LINK_DISABLE_CONTROL2	2-168
NBMISCIND\:0x66	StrapsOutputMux_6	2-178
NBMISCIND\:0x67	StrapsOutputMux_7	2-179
NBMISCIND\:0x68	StrapsOutputMux_8	2-180
NBMISCIND\:0x69	StrapsOutputMux_9	2-181
NBMISCIND\:0x6A	StrapsOutputMux_A	2-181
NBMISCIND\:0x6B	StrapsOutputMux_B	2-181
NBMISCIND\:0x6C	StrapsOutputMux_C	2-182
NBMISCIND\:0x75	IOC_FEATURE_CNTL	2-184
NBMISCIND\:0xD	PCIE_LINK_DISABLE_CONTROL1	2-138
pcieConfigDev[13:2]:0x0	PCIE_VENDOR_ID	2-39
pcieConfigDev[13:2]:0x100	PCIE_VENDOR_SPECIFIC_ENH_CAP_LIST	2-56
pcieConfigDev[13:2]:0x104	PCIE_VENDOR_SPECIFIC_HDR	2-56
pcieConfigDev[13:2]:0x108	PCIE_VENDOR_SPECIFIC1	2-56
pcieConfigDev[13:2]:0x10C	PCIE_VENDOR_SPECIFIC2	2-56
pcieConfigDev[13:2]:0x110	PCIE_VC_ENH_CAP_LIST	2-56
pcieConfigDev[13:2]:0x114	PCIE_PORT_VC_CAP_REG1	2-56
pcieConfigDev[13:2]:0x118	PCIE_PORT_VC_CAP_REG2	2-57
pcieConfigDev[13:2]:0x11C	PCIE_PORT_VC_CNTL	2-57
pcieConfigDev[13:2]:0x11E	PCIE_PORT_VC_STATUS	2-57
pcieConfigDev[13:2]:0x120	PCIE_VC0_RESOURCE_CAP	2-57
pcieConfigDev[13:2]:0x124	PCIE_VC0_RESOURCE_CNTL	2-57
pcieConfigDev[13:2]:0x12A	PCIE_VC0_RESOURCE_STATUS	2-58
pcieConfigDev[13:2]:0x12C	PCIE_VC1_RESOURCE_CAP	2-58
pcieConfigDev[13:2]:0x130	PCIE_VC1_RESOURCE_CNTL	2-58
pcieConfigDev[13:2]:0x136	PCIE_VC1_RESOURCE_STATUS	2-58
pcieConfigDev[13:2]:0x140	PCIE_DEV_SERIAL_NUM_ENH_CAP_LIST	2-58
pcieConfigDev[13:2]:0x144	PCIE_DEV_SERIAL_NUM_DW1	2-59
pcieConfigDev[13:2]:0x148	PCIE_DEV_SERIAL_NUM_DW2	2-59
pcieConfigDev[13:2]:0x150	PCIE_ADV_ERR_RPT_ENH_CAP_LIST	2-59
pcieConfigDev[13:2]:0x154	PCIE_UNCORR_ERR_STATUS	2-59
pcieConfigDev[13:2]:0x158	PCIE_UNCORR_ERR_MASK	2-59
pcieConfigDev[13:2]:0x15C	PCIE_UNCORR_ERR_SEVERITY	2-60
pcieConfigDev[13:2]:0x160	PCIE_CORR_ERR_STATUS	2-60
pcieConfigDev[13:2]:0x164	PCIE_CORR_ERR_MASK	2-60

Table 2-2 Registers Sorted by Address (Continued)

Address	Register Name	Page
pcieConfigDev[13:2]:0x168	PCIE_ADV_ERR_CAP_CNTL	2-60
pcieConfigDev[13:2]:0x16C	PCIE_HDR_LOG0	2-61
pcieConfigDev[13:2]:0x170	PCIE_HDR_LOG1	2-61
pcieConfigDev[13:2]:0x174	PCIE_HDR_LOG2	2-61
pcieConfigDev[13:2]:0x178	PCIE_HDR_LOG3	2-61
pcieConfigDev[13:2]:0x17C	PCIE_ROOT_ERR_CMD	2-61
pcieConfigDev[13:2]:0x18	PCIE_SUB_BUS_NUMBER_LATENCY	2-42
pcieConfigDev[13:2]:0x180	PCIE_ROOT_ERR_STATUS	2-61
pcieConfigDev[13:2]:0x184	PCIE_ERR_SRC_ID	2-62
pcieConfigDev[13:2]:0x190	PCIE_ACS_ENH_CAP_LIST	2-62
pcieConfigDev[13:2]:0x194	PCIE_ACS_CAP	2-62
pcieConfigDev[13:2]:0x196	PCIE_ACS_CNTL	2-63
pcieConfigDev[13:2]:0x1C	PCIE_IO_BASE_LIMIT	2-42
pcieConfigDev[13:2]:0x1E	PCIE_SECONDARY_STATUS	2-42
pcieConfigDev[13:2]:0x2	PCIE_DEVICE_ID	2-39
pcieConfigDev[13:2]:0x20	PCIE_MEM_BASE_LIMIT	2-43
pcieConfigDev[13:2]:0x24	PCIE_PREF_BASE_LIMIT	2-43
pcieConfigDev[13:2]:0x28	PCIE_PREF_BASE_UPPER	2-43
pcieConfigDev[13:2]:0x2C	PCIE_PREF_LIMIT_UPPER	2-43
pcieConfigDev[13:2]:0x30	PCIE_IO_BASE_LIMIT_HI	2-44
pcieConfigDev[13:2]:0x34	PCIE_CAP_PTR	2-44
pcieConfigDev[13:2]:0x3C	PCIE_INTERRUPT_LINE	2-44
pcieConfigDev[13:2]:0x3D	PCIE_INTERRUPT_PIN	2-45
pcieConfigDev[13:2]:0x3E	PCIE_IRQ_BRIDGE_CNTL	2-44
pcieConfigDev[13:2]:0x4	PCIE_COMMAND	2-39
pcieConfigDev[13:2]:0x50	PCIE_PMI_CAP_LIST	2-45
pcieConfigDev[13:2]:0x52	PCIE_PMI_CAP	2-45
pcieConfigDev[13:2]:0x54	PCIE_PMI_STATUS_CNTL	2-45
pcieConfigDev[13:2]:0x58	PCIE_CAP_LIST	2-46
pcieConfigDev[13:2]:0x5A	PCIE_CAP	2-46
pcieConfigDev[13:2]:0x5C	PCIE_DEVICE_CAP	2-46
pcieConfigDev[13:2]:0x6	PCIE_STATUS	2-40
pcieConfigDev[13:2]:0x60	PCIE_DEVICE_CNTL	2-47
pcieConfigDev[13:2]:0x62	PCIE_DEVICE_STATUS	2-48
pcieConfigDev[13:2]:0x64	PCIE_LINK_CAP	2-48
pcieConfigDev[13:2]:0x68	PCIE_LINK_CNTL	2-49
pcieConfigDev[13:2]:0x6A	PCIE_LINK_STATUS	2-49
pcieConfigDev[13:2]:0x6C	PCIE_SLOT_CAP	2-50
pcieConfigDev[13:2]:0x70	PCIE_SLOT_CNTL	2-51
pcieConfigDev[13:2]:0x72	PCIE_SLOT_STATUS	2-51
pcieConfigDev[13:2]:0x74	PCIE_ROOT_CNTL	2-52
pcieConfigDev[13:2]:0x76	PCIE_ROOT_CAP	2-52
pcieConfigDev[13:2]:0x78	PCIE_ROOT_STATUS	2-52
pcieConfigDev[13:2]:0x7C	PCIE_DEVICE_CAP2	2-52
pcieConfigDev[13:2]:0x8	PCIE_REVISION_ID	2-40
pcieConfigDev[13:2]:0x80	PCIE_DEVICE_CNTL2	2-52
pcieConfigDev[13:2]:0x82	PCIE_DEVICE_STATUS2	2-53
pcieConfigDev[13:2]:0x84	PCIE_LINK_CAP2	2-53
pcieConfigDev[13:2]:0x88	PCIE_LINK_CNTL2	2-53
pcieConfigDev[13:2]:0x8A	PCIE_LINK_STATUS2	2-53
pcieConfigDev[13:2]:0x8C	PCIE_SLOT_CAP2	2-53
pcieConfigDev[13:2]:0x9	PCIE_PROG_INTERFACE	2-41
pcieConfigDev[13:2]:0x90	PCIE_SLOT_CNTL2	2-53
pcieConfigDev[13:2]:0x92	PCIE_SLOT_STATUS2	2-54
pcieConfigDev[13:2]:0xA	PCIE_SUB_CLASS	2-41
pcieConfigDev[13:2]:0xA0	PCIE_MSI_CAP_LIST	2-54
pcieConfigDev[13:2]:0xA2	PCIE_MSI_MSG_CNTL	2-54

Table 2-2 Registers Sorted by Address (Continued)

Address	Register Name	Page
pcieConfigDev[13:2]:0xA4	PCIE_MSI_MSG_ADDR_LO	2-54
pcieConfigDev[13:2]:0xA8	PCIE_MSI_MSG_ADDR_HI	2-55
pcieConfigDev[13:2]:0xA8	PCIE_MSI_MSG_DATA	2-55
pcieConfigDev[13:2]:0xAC	PCIE_MSI_MSG_DATA_64	2-55
pcieConfigDev[13:2]:0xB	PCIE_BASE_CLASS	2-41
pcieConfigDev[13:2]:0xB0	PCIE_SSID_CAP_LIST	2-55
pcieConfigDev[13:2]:0xB4	PCIE_SSID_ID	2-55
pcieConfigDev[13:2]:0xB8	PCIE_MSI_MAP_CAP_LIST	2-55
pcieConfigDev[13:2]:0xC	PCIE_CACHE_LINE	2-41
pcieConfigDev[13:2]:0xD	PCIE_LATENCY	2-41
pcieConfigDev[13:2]:0xE	PCIE_HEADER	2-41
pcieConfigDev[13:2]:0xE0	PCIE_PORT_INDEX	2-55
pcieConfigDev[13:2]:0xE4	PCIE_PORT_DATA	2-55
pcieConfigDev[13:2]:0xF	PCIE_BIST	2-41
pcieConfigDev[13:2]\:0x40	PCIE_EXT_BRIDGE_CNTL	2-45
PCIEIND:0x0	PCIE_RESERVED	2-95
PCIEIND:0x1	PCIE_SCRATCH	2-95
PCIEIND:0x10	PCIE_CNTL	2-96
PCIEIND:0x11	PCIE_CONFIG_CNTL	2-96
PCIEIND:0x12	PCIE_DEBUG_CNTL	2-96
PCIEIND:0x13	PCIE_RTR_CPL_TIMEOUT_STATUS	2-97
PCIEIND:0x14	PCIE_CI_SLV_R_RTR_TIMEOUT_CNTL	2-97
PCIEIND:0x15	PCIE_CI_MST_R_RTR_TIMEOUT_CNTL	2-98
PCIEIND:0x16	PCIE_CI_MST_C_RTR_TIMEOUT_CNTL	2-98
PCIEIND:0x17	PCIE_REG_R_RTR_TIMEOUT_CNTL	2-98
PCIEIND:0x18	PCIE_TX_SLVCPL_TIMEOUT_CNTL	2-98
PCIEIND:0x19	PCIE_TX_SLVCPL_NS_TIMEOUT_CNTL	2-98
PCIEIND:0x1C	PCIE_CNTL2	2-99
PCIEIND:0x2	PCIE_HW_DEBUG	2-95
PCIEIND:0x20	PCIE_CI_CNTL	2-99
PCIEIND:0x21	PCIE_BUS_CNTL	2-100
PCIEIND:0x22	PCIE_LC_STATE6	2-100
PCIEIND:0x23	PCIE_LC_STATE7	2-100
PCIEIND:0x24	PCIE_LC_STATE8	2-100
PCIEIND:0x25	PCIE_LC_STATE9	2-100
PCIEIND:0x26	PCIE_LC_STATE10	2-100
PCIEIND:0x27	PCIE_LC_STATE11	2-101
PCIEIND:0x28	PCIE_LC_STATUS1	2-101
PCIEIND:0x29	PCIE_LC_STATUS2	2-101
PCIEIND:0x30	PCIE_WPR_CNTL	2-101
PCIEIND:0x31	PCIE_RX_LAST_TLP0	2-101
PCIEIND:0x32	PCIE_RX_LAST_TLP1	2-102
PCIEIND:0x33	PCIE_RX_LAST_TLP2	2-102
PCIEIND:0x34	PCIE_RX_LAST_TLP3	2-102
PCIEIND:0x35	PCIE_TX_LAST_TLP0	2-102
PCIEIND:0x36	PCIE_TX_LAST_TLP1	2-102
PCIEIND:0x37	PCIE_TX_LAST_TLP2	2-102
PCIEIND:0x38	PCIE_TX_LAST_TLP3	2-102
PCIEIND:0x39	PCIE_I2C_DEBUG_BUS	2-102
PCIEIND:0x3A	PCIE_I2C_REG_ADDR_EXPAND	2-103
PCIEIND:0x3B	PCIE_I2C_REG_DATA	2-103
PCIEIND:0x3C	PCIE_CFG_CNTL	2-103
PCIEIND:0x40	PCIE_P_CNTL	2-103
PCIEIND:0x41	PCIE_P_BUF_STATUS	2-104
PCIEIND:0x42	PCIE_P_DECODER_STATUS	2-104
PCIEIND:0x43	PCIE_P_MISC_STATUS	2-105
PCIEIND:0x44	PCIE_P_PLL_CNTL	2-105

Table 2-2 Registers Sorted by Address (Continued)

Address	Register Name	Page
PCIEIND:0x50	PCIE_P_RCV_L0S_FTS_DET	2-105
PCIEIND:0x60	PCIE_P_IMP_CNTL_STRENGTH	2-105
PCIEIND:0x61	PCIE_P_IMP_CNTL_UPDATE	2-105
PCIEIND:0x62	PCIE_P_STR_CNTL_UPDATE	2-106
PCIEIND:0x63	PCIE_P_PAD_MISC_CNTL	2-106
PCIEIND:0x64	PCIE_P_PAD_FORCE_EN	2-106
PCIEIND:0x65	PCIE_P_PAD_FORCE_DIS	2-106
PCIEIND:0xC0	PCIE_STRAP_MISC	2-107
PCIEIND:0xC1	PCIE_STRAP_MISC2	2-107
PCIEIND:0xC2	PCIE_STRAP_PI	2-107
PCIEIND:0xC3	PCIE_B_P90_CNTL	2-107
PCIEIND:0xC4	PCIE_STRAP_I2C_BD	2-108
PCIEIND:0xC6	PCIE_P90RX_PRBS10_CNTL	2-108
PCIEIND:0xC7	PCIE_P90_BRX_PRBS10_ER	2-108
PCIEIND:0xC8	PCIE_PRBS_CLR	2-108
PCIEIND:0xC9	PCIE_PRBS_STATUS1	2-108
PCIEIND:0xCA	PCIE_PRBS_STATUS2	2-108
PCIEIND:0xCB	PCIE_PRBS_FREERUN	2-109
PCIEIND:0xCC	PCIE_PRBS_MISC	2-109
PCIEIND:0xCD	PCIE_PRBS_USER_PATTERN	2-109
PCIEIND:0xCE	PCIE_PRBS_LO_BITCNT	2-109
PCIEIND:0xCF	PCIE_PRBS_HI_BITCNT	2-109
PCIEIND:0xD0	PCIE_PRBS_ERRCNT_0	2-110
PCIEIND:0xD1	PCIE_PRBS_ERRCNT_1	2-110
PCIEIND:0xD2	PCIE_PRBS_ERRCNT_2	2-110
PCIEIND:0xD3	PCIE_PRBS_ERRCNT_3	2-110
PCIEIND:0xD4	PCIE_PRBS_ERRCNT_4	2-110
PCIEIND:0xD5	PCIE_PRBS_ERRCNT_5	2-110
PCIEIND:0xD6	PCIE_PRBS_ERRCNT_6	2-110
PCIEIND:0xD7	PCIE_PRBS_ERRCNT_7	2-110
PCIEIND:0xD8	PCIE_PRBS_ERRCNT_8	2-111
PCIEIND:0xD9	PCIE_PRBS_ERRCNT_9	2-111
PCIEIND:0xDA	PCIE_PRBS_ERRCNT_10	2-111
PCIEIND:0xDB	PCIE_PRBS_ERRCNT_11	2-111
PCIEIND:0xDC	PCIE_PRBS_ERRCNT_12	2-111
PCIEIND:0xDD	PCIE_PRBS_ERRCNT_13	2-111
PCIEIND:0xDE	PCIE_PRBS_ERRCNT_14	2-111
PCIEIND:0xDF	PCIE_PRBS_ERRCNT_15	2-111
PCIEIND:0xE	PCIE_RX_NUM_NAK	2-95
PCIEIND:0xF	PCIE_RX_NUM_NAK_GENERATED	2-95
PCIEIND_P:0x0	PCIEP_RESERVED	2-113
PCIEIND_P:0x1	PCIEP_SCRATCH	2-113
PCIEIND_P:0x10	PCIEP_PORT_CNTL	2-113
PCIEIND_P:0x2	PCIEP_HW_DEBUG	2-113
PCIEIND_P:0x20	PCIE_TX_CNTL	2-114
PCIEIND_P:0x21	PCIE_TX_REQUESTER_ID	2-115
PCIEIND_P:0x22	PCIE_TX_VENDOR_SPECIFIC	2-115
PCIEIND_P:0x23	PCIE_TX_REQUEST_NUM_CNTL	2-115
PCIEIND_P:0x24	PCIE_TX_SEQ	2-115
PCIEIND_P:0x25	PCIE_TX_REPLAY	2-115
PCIEIND_P:0x26	PCIE_TX_ACK_LATENCY_LIMIT	2-115
PCIEIND_P:0x30	PCIE_TX_CREDITS_ADVT_P	2-116
PCIEIND_P:0x31	PCIE_TX_CREDITS_ADVT_NP	2-116
PCIEIND_P:0x32	PCIE_TX_CREDITS_ADVT_CPL	2-116
PCIEIND_P:0x33	PCIE_TX_CREDITS_INIT_P	2-116
PCIEIND_P:0x34	PCIE_TX_CREDITS_INIT_NP	2-116
PCIEIND_P:0x35	PCIE_TX_CREDITS_INIT_CPL	2-116

Table 2-2 Registers Sorted by Address (Continued)

Address	Register Name	Page
PCIEIND_P:0x36	PCIE_TX_CREDITS_STATUS	2-116
PCIEIND_P:0x37	PCIE_TX_CREDITS_FCU_THRESHOLD	2-117
PCIEIND_P:0x50	PCIE_P_PORT_LANE_STATUS	2-118
PCIEIND_P:0x60	PCIE_FC_P	2-118
PCIEIND_P:0x61	PCIE_FC_NP	2-118
PCIEIND_P:0x62	PCIE_FC_CPL	2-119
PCIEIND_P:0x6A	PCIE_ERR_CNTL	2-119
PCIEIND_P:0x70	PCIE_RX_CNTL	2-119
PCIEIND_P:0x71	PCIE_RX_EXPECTED_SEQNUM	2-119
PCIEIND_P:0x72	PCIE_RX_VENDOR_SPECIFIC	2-120
PCIEIND_P:0x80	PCIE_RX_CREDITS_ALLOCATED_P	2-120
PCIEIND_P:0x81	PCIE_RX_CREDITS_ALLOCATED_NP	2-120
PCIEIND_P:0x82	PCIE_RX_CREDITS_ALLOCATED_CPL	2-120
PCIEIND_P:0x83	PCIE_RX_CREDITS_RECEIVED_P	2-120
PCIEIND_P:0x84	PCIE_RX_CREDITS_RECEIVED_NP	2-120
PCIEIND_P:0x85	PCIE_RX_CREDITS_RECEIVED_CPL	2-121
PCIEIND_P:0xA0	PCIE_LC_CNTL	2-121
PCIEIND_P:0xA1	PCIE_LC_TRAINING_CNTL	2-122
PCIEIND_P:0xA2	PCIE_LC_LINK_WIDTH_CNTL	2-123
PCIEIND_P:0xA3	PCIE_LC_N_FTS_CNTL	2-124
PCIEIND_P:0xA4	PCIE_LC_SPEED_CNTL	2-124
PCIEIND_P:0xA5	PCIE_LC_STATE0	2-127
PCIEIND_P:0xA6	PCIE_LC_STATE1	2-127
PCIEIND_P:0xA7	PCIE_LC_STATE2	2-127
PCIEIND_P:0xA8	PCIE_LC_STATE3	2-127
PCIEIND_P:0xA9	PCIE_LC_STATE4	2-127
PCIEIND_P:0xAA	PCIE_LC_STATE5	2-128
PCIEIND_P:0xB1	PCIE_LC_CNTL2	2-128
PCIEIND_P:0xB2	PCIE_LC_BW_CHANGE_CNTL	2-129
PCIEIND_P:0xB3	PCIE_LC_CDR_CNTL	2-129
PCIEIND_P:0xB4	PCIE_LC_LANE_CNTL	2-129
PCIEIND_P:0xB5	PCIE_LC_CNTL3	2-130
PCIEIND_P:0xC0	PCIEP_STRAP_LC	2-130
PCIEIND_P:0xC1	PCIEP_STRAP_MISC	2-131
pmm2reg:0x0	PM2_CNTRL	2-80
pmm2reg:0x4	PM1_STATUS	2-80

Appendix B
Revision History

Rev 3.04 (August 2012)

- Updated the following registers by adding a note to some (or all) of the fields to indicate that "the contents of the field are preserved across a warm reset and are cleared by a cold reset".
  PcieConfigDev: 0x154
  PcieConfigDev: 0x160
  PcieConfigDev: 0x168
  PcieConfigDev: 0x16C to 0x178
  PcieConfigDev: 0x180 and 0x184

Rev 3.03 (May 2012)

- Updated PCIE_RX_CNTL [PCIEIND_P:0x70].

Rev 3.02 (October 2011)

- Updated description of bits[21:15] of IOMMU_CAP_MISC (nbconfigfunc2:0x50) to include 0x40 is the default value.

Rev 3.01 (April 2011)

- Added new register EFUSE_CFG_HW_CONFIG_4 (NBMISCIND:0x4A).

Rev 3.00 (December 2010)

- This revision becomes public.
- Bits[2:0] of L1_CNTRL_2 became reserved.
- For PCIE_ADV_ERR_CAP_CNTL [pcieConfigDev[13:2]:0x168, changed bits 6 and 8 from R (Read-only) to RW.

Rev 2.04 (March 2010)

- Fixed error in the field description of B_P90TX_DRV_STR_sb and of B_P90TX_DRV_STR_GFXGPP[1, 2, 3a] in registers StrapsOutputMux_8 and PCIE_NBCFG_REG[5,14] respectively, where the 00 setting is corrected from 18mA nominal to 26mA nominal.

Rev 2.03 (March 2010)

- Updated HTIU_DEBUG..
- Removed (R), i.e., Read-only, from bit 15 and bit 19 of these registers: PCIE_UNCORR_ERR_STATUS, PCIE_UNCORR_ERR_MASK, and PCIE_UNCORR_ERR_SEVERITY.

Rev 2.02 (May 2009)

- Based on engineering document revision 1.19
- Replaced the ASIC codename “SR5690/SR5670” with “SR5690/5670/5650” throughout the documentand and indicated differences between the variants where applicable.
- Updated the following registers:

Updated Registers
CLK_TOP_SPARE_A
HTIU_DEBUG
IOAPIC_CONF_LOWER
IOAPIC_VERSION_REGISTER
IOC_FEATURE_CNTL
L1_DEBUG_0
L1_DEBUG_1
L1_DEBUG_STATUS
L2_DEBUG_0
L1_DEBUG_1
L1_DEBUG_3
NB_HT3_LINK_FREQUENCY_EXTENSION
PCIE_CORE_ARB
PCIE_CORE_ARB_2
PCIE_HW_DEBUG
PCIE_LC_TRAINING_CNTL
PCIE_NBCFG_REG2 through to PCIE_NBCFG_REG19
PCIE_P_CNTL
PCIE_RX_CNTL
StrapsOutputMux_6 through to StrapsOutputMux_F

Rev 2.01 (Oct 2008)

- Based on engineering document revision 1.17
- Replaced the ASIC codename “RD890S” with “SR5690/SR5670” throughout the documentand and indicated differences between SR5690 and SR5670 where applicable.
- Replaced GFX, GFX2, GPP and GPP2 with GPP1, GPP2, GPP3a and GPP3b respectively throughout the document.
- Removed these registers: NB_MC_INDEX, NB_MC_DATA.
- Removed 4 BAR registers (CLK_BAR*_*_*) at Clkconfig: 0x14, 0x18, 0x1C and 0x20.
- Removed NB_GC_STRAPS.
- Removed previous section 2.2.5: APCCONFIG Registers.
- Updated the following registers (note: the affected bits are in brackets. An absence of bits indicates that most fields of the register or the register description itself have been updated):

Updated Registers [fields]
NB_MISC_DATA
NB_MISC_INDEX [6:0]
MC_CLK_INDEX
MC_CLK_DATA

Updated Registers [fields]
HTIU_NB_INDEX [7:0]
NB_PCIE_INDX_ADDR
NB_PCIE_INDX_DATA
IOAPIC_INDEX
IOAPIC_DATA
PCIE_BASE_CLASS (Changed default)
PCIE_SUB_CLASS (Changed default)
PCIE_LC_TRAINING_CNTL [19]
PCIE_NBCFG_REG(2 to19)
NB_HT3_CAPABILITY [21:18]
NB_HT_LINK_COMMAND
NB_HT_LINK_CONF_CNTL
NB_HT_LINK_END
NB_HT_LINK_FREQ_CAP_A
NB_HT_LINK_FREQ_CAP_B
NB_HT_ENUMERATION_SCRATCHPAD [25]
StrapsOutputMux_[6 to C; F] (8 registers)
IOC_FEATURE_CNTL
MSI_MAPPING_CAPABILITY [7]
Almost all CLK Config registers
IOAPIC_ID_REGISTER [31:28]
IOAPIC_VERSION_REGISTER [23:16]
IOMMU_CONTROL_W [2:0]
HTIU_DOWNSTREAM_CONFIG [5:4]
Transmiter_Control_0 [28]
PARITY_ERROR_INJECTION_CNTL [7:0]
GPIO_1_4 to GPIO_21_24 (6 registers)

Rev 2.00 (May, 2008)

- Based on engineering document revision 1.16.
- Added new Section 2.1: Register Spaces and Device IDs.
- Added new Section 2.4.2 IOAPICMMREG Registers
- Added new section 2.5.1 IOAPICCMISCIND Registers
- Added new Section 2.5.2 IOAPICMMISCIND Registers.
- Added the following registers [note: registers with similar names (distinguished by a running digit “n” at the end, e.g. L2_ERR_RULE_CONTROL_n), are lumped together using a range contraction notation of _[n:m], where n denotes 5 and m denotes 0 in this particular example]:

New Registers
HOTPLUG_BLINK_RATE
HOTPLUG_SPARE_[1:0]
HT3PHY_CNTL_14
IOAPIC_DATA
IOAPIC_INDEX
L1_CNTRL_3

New Registers
L1_FEATURE_CNTRL
L2_CONTROL_[6:5]
L2_CONTROL_1
L2_CP_CONTROL_[3:1]
L2_CREDIT_CONTROL_[1:0]
L2_CREDIT_CONTROL_2
L2_ERR_RULE_CONTROL_[5:0]
L2_INT_CONTROL
L2_MCIF_CONTROL
PCIE_DEVICE_SERIAL_NO_[2:1]
PCIE_EXT_BRIDGE_CNTL
PCIE_LINK_DISABLE_CONTROL_[2:1]
Registers under IOAPICCMISCIND space (see Section 2.5.1)
Registers under IOAPICMMISCIND space (see Section 2.5.2)
Registers under IOAPICMMREG space (see Section 2.4.2)

- Updated the following registers:

Updated Registers
CFG_HT_DIV_CTRL
CFG_IOC_TOM3
CLK_REVISION_ID
CLK_STATUS
HT_BIST_EXTENDED_CONTROL_0
HT_ERROR_INJECTION_CNTL
HT_PARITY_ERR_CONTROL_STATUS
HT3PHY_CNTL_[15:8] (8 registers)
HTIU_DEBUG
HTIU_IOMMU_CONTROL_[1:0] (2 registers)
HTIU_PCIE_ERR_FLOOD_CONTROL_[1:2] (2 registers)
HTIU_TAG_XTL_CONTROL_1
HTIU_UPSTREAM_ARB_CONTROL_[6:0] (7 registers)
HTIU_UPSTREAM_ARB_CONTROL_8
IOC_FEATURE_CNTL
IOMMU_CONTROL_W
IOMMU_DEVICE_ID
IOMMU_HEADER
IOMMU_INTERRUPT_PIN
IOMMU_MMIO_CNTRL_0
IOMMU_MSI_CAP
L1_BANK_DISABLE_0
L1_BANK_SEL_0
L1CFG_INDEX
L1_CNTRL_[2:0] (2 registers)
L1_DEBUG_[1:0] (2 registers)

Updated Registers
L1_DEBUG_STATUS
L1_WQ_STATUS_[3:0] (4 registers)
L2_CONTROL_0
L2_DTC_CONTROL
L2_DTC_HASH_CONTROL
L2_DTC_WAY_CONTROL
L2_ITC_CONTROL
L2_ITC_HASH_CONTROL
L2_ITC_WAY_CONTROL
L2_PDC_CONTROL
L2_PDC_HASH_CONTROL
L2_PDC_WAY_CONTROL
L2_PTC_A_CONTROL
L2_PTC_A_HASH_CONTROL
L2_PTC_A_WAY_CONTROL
L2_PTC_B_CONTROL
L2_PTC_B_HASH_CONTROL
L2_PTC_B_WAY_CONTROL
L2_PTC_B_WAY_CONTROL
L2_TW_CONTROL
NB_APIC_P2P_CNTL
NB_APIC_P2P_RANGE_2
NB_BUS_NUM_CNTL
NB_CNTL
NB_HT_CLK_CNTL_RECEIVER_COMP_CNTLI
NB_HT_LINK_FREQ_CAP_A
NB_HT_LINK_FREQ_CAP_B
NB_HT3_LINK_FREQUENCY_EXTENSION
NB_HTIU_CFG
NB_INTERRUPT_PIN
NB_LATENCY - Changed RW to R
NB_LOWER_TOP_OF_DRAM2
NB_STRAP_READ_BACK
NB_UPPER_TOP_OF_DRAM2
PARITY_ERROR_INJECTION_CNTL
PARITY_ERROR_STATUS_[25:0] (26 registers)
PCIE_CORE_ARB[
PCIE_CORE_ARB_2
PCIE_LC_TRAINING_CNTL
PCIE_SLOT_CNTL
PCIE_SLOT_STATUS
PCIE_VENDOR_ID
PCIEP_PORT_CNTL
RECEIVER_CONTROL_1
TRANSMITTER_CONTROL_[2:1] (2 registers)

- Removed all *PERF* registers.
- Removed NB_STRAP_READ_BACK

Rev 1.00 (Jan, 2008)

- Preliminary version, based on the engineering document revision 1.14.