AMD SP5100 Databook

Technical Reference Manual
Rev. 1.70

P/N: 44409_sp5100_ds_pub

Revision History

Date	Revision	Description
Oct 2010	1.70	First release of the public version. Changes from the latest released NDA version include: • Updated Table 11-3, “DC Characteristics for Interface on the SP5100”: Corrected VIL minimum value to -0.5V for CPU signals, RSMRST#, and SBPWRGD; filled in ILI values for NB-ALLOW_LDTSTP, RSMRST#, and SBPWRGD; corrected condition for GPIO/IMC_GPIO and IDE pins’ VOH to IOH=-8.0mA. • Updated Table 14-5, “List of Pins on the SP5100 XOR Chain and the Order of Connection”: Corrected pin names at XOR# 113 and 114 to USB_FSD13P and USB_FSD12P. • Updated Section 7.12, “Northbridge / Power Management Interface”: Revised description for WAKE#/GEVENT8#. • Updated Section 7.13, “SMBus Interface/General Purpose Open Controller”: Removed references to ASF, as the feature is no longer supported; SCL1/ SDA1 interface is now used as secondary SMBUS in the S5 power domain.

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1 Introduction

AMD's SP5100 is a Southbridge that integrates key I/O, communications, and other features required in a state-of-the-art server platform into a single device. It is specifically designed to operate with AMD's server Northbridges.

1.1 Features of the SP5100

CPU Interface

- Supports AMD Opteron™ server class processors, including:
  - Socket F processors ("Barcelona," Shanghai," and "Istanbul" series only)
  - Socket G34 processors
  - Socket C32 processors

A-Link Express II interface to AMD Northbridges

- 1 / 2 / 4-lane A-Link Express II interface
- Dynamic detection of lane configuration
- High data transfer bandwidth (up to 2.5 Gb/s / Lane)

PCI Host Bus Controller

- Supports PCI bus at 33 MHz
- PCI Rev. 2.3 specification support
- Supports up to 6 bus master devices
- Supports 40-bit addressing
- Interrupt steering supported for plug-n-play devices
- BIOS / Hardware support to hide PCI device
- Spread spectrum support

USB Controllers

- 5 OHCI and 2 EHCI Host controllers to supports 12 USB 2.0 ports and 2 dedicated USB 1.1 ports
- ACPI S1 ~ S5 supported
- Legacy Keyboard/Mouse support
- USB debug port
- Port disable supported with individual control

SMBus Controller

- SMBus Rev. 2.0 compliant
- Support SMBALERT # signal / GPIO

Interrupt Controller

- Supports IOAPIC/X-IO APIC mode for 24 channels of interrupts
- Supports 8259 legacy mode for 15 interrupts
- Supports programmable level/edge triggering on each channels
- Supports serial interrupt on quiet and continuous modes

DMA Controller

- Two cascaded 8237 DMA controllers
- Supports PC/PCI DMA
- Supports LPC DMA
- Supports type F DMA

LPC Host Bus Controller

- Supports LPC based super I/O and flash devices
- Two Master/DMA devices supported
- Support for TPM version 1.1/1.2 devices
- Supports SPI devices

SATA Controller

- Supports six SATA ports with transfer rates up to 3 Gb/s
- Complies with SATA 2.5 specification

- Supports both SATA 1.5 and SATA 3.0 compliance devices
- Two modes of operation are supported
  - Legacy Mode using I/O space
  - AHCI mode using the Memory space
- Parallel ATA emulation supported to allow seamless support for IDE software.
- Supports e-SATA
- Supports hot plug for AHCI mode

Legacy IDE Emulation Support

- Legacy Mode using I/O space
- Parallel ATA emulation supported to allow seamless support for IDE software.

RAID Support

- Supports integrated RAID 0, RAID 1, and RAID 10 (requires use of 4 or more SATA ports) functionalities across all 6 ports. **Note:** AMD does not provide RAID drivers for the SP5100.

AHCI Support

- AHCI mode using the memory space
- Supports AHCI hardware assist to support advanced features such as NCQ (Native Command Queuing), hot plug, and Device or Host initiated power Management (DIPM /HIPM)

IDE Controller

- Single PATA channel support
- Supports PIO, Multi-word DMA, and Ultra DMA 33/66/100/133 modes.
- 32x32-byte buffers each channel for buffering
- Swap bay support by tri-state IDE signals
- Integrated IDE series resistor

High Definition Audio

- 4 Independent output streams (DMA)
- 4 Independent input streams (DMA)
- Multiple channels of audio output per stream
- Support up to 4 codec's
- Up to 192 kHz Sample Rate and 32-bit Audio
- 64-bit addressing capability for DMA Bus Master
- Unified Audio Architecture (UAA) compatible
- HD Audio registers can be located anywhere in the 64-bit address space

Timers

- 8254 compatible timer
- Microsoft High Precision Event Timer (HPET)
- ACPI power management timer
- Watchdog timer

RTC (Real Time Clock)

- 256-byte battery-backed CMOS RAM
- Hardware supported century rollover
- RTC battery monitoring feature

Power Management

- ACPI specification 3.0 compliant power management schemes
  - Supports C1e, C2, C3 and C3 pop-up
  - Supports S0, S1, S3, S4, and S5
- Wakeup events for S1, S3, S4/S5 generated by:
  - Any GEVENT pin
  - Any GPM pin
  - USB
  - Power Button
  - Internal RTC wakeup
  - SMI# event
- Full support for On-Now
- CPU SMM support, generating SMI# signal upon power management events
- GPIO supports on external wake up events
- CLKRUN# supported on PCI power management
- ALPM (HIPM) on SATA

- DIPM on SATA

Note: Advanced Power Management (APM) is not supported.

Hardware Monitor

- Hardware monitoring support for voltage sensors, fan control, and digital TSI to AM3 processors. **Note:** Temperature monitoring is NOT supported.

1.2 Part Number and Branding

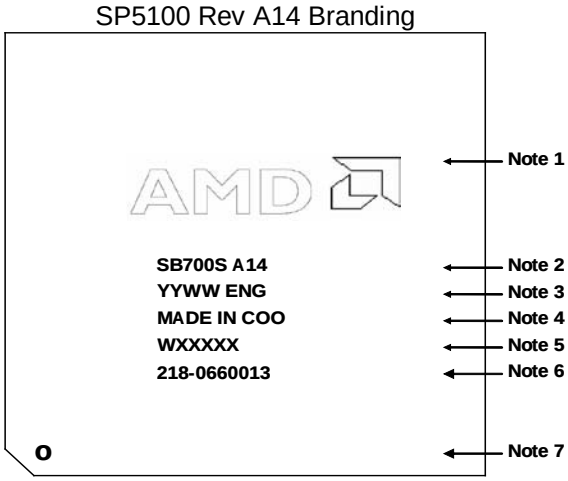


Figure 1-1: SP5100 Rev A14 Branding Diagram

Note 1: Marketing logo

Note 2: AMD product type

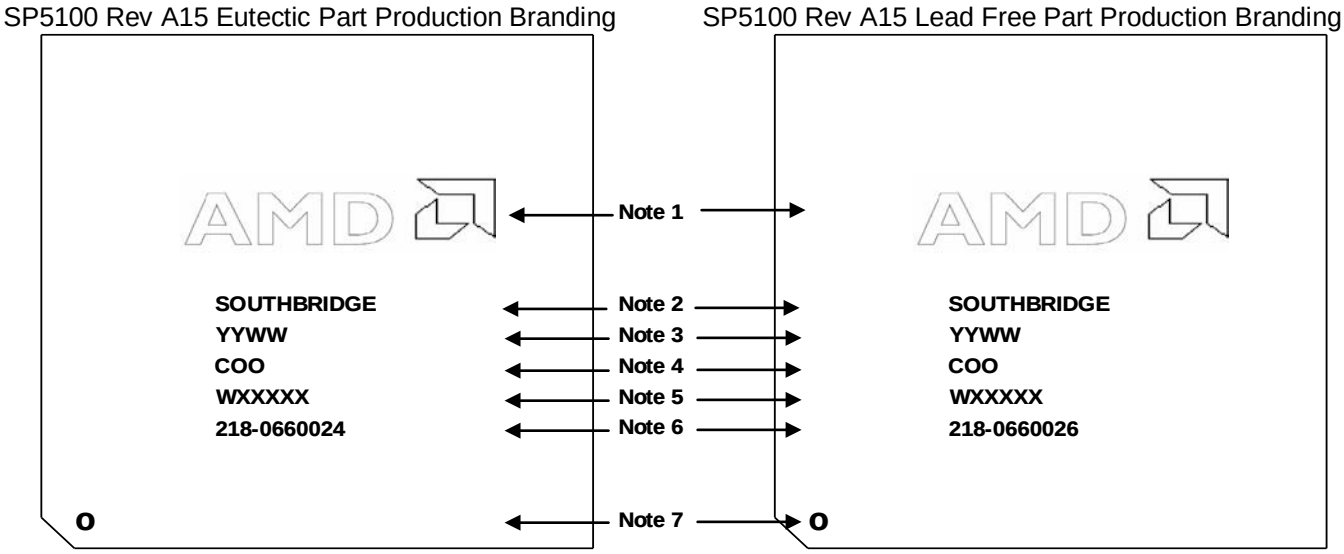
Note 3: Date Code (YYWW). YY-assembly start year, WW-assembly start week.

Note 4: COO. Country of origin (assembly site)

Note 5: This is wafer foundry's lot number for the product.

Note 6: AMD part number (see below)

Note 7: Pin 1 Orientation



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Note 6: AMD part number (see below)

Note 7: Pin 1 Orientation

Figure 1-2: SP5100 Rev A15 Branding Diagrams

Table 1-1: SP5100 Part Numbers

ASIC Revision	AMD Part Number
A14	218-0660013
A15 Eutectic Part	218-0660024
A15 Lead Free Part	218-0660026

2 SP5100 Block Diagram

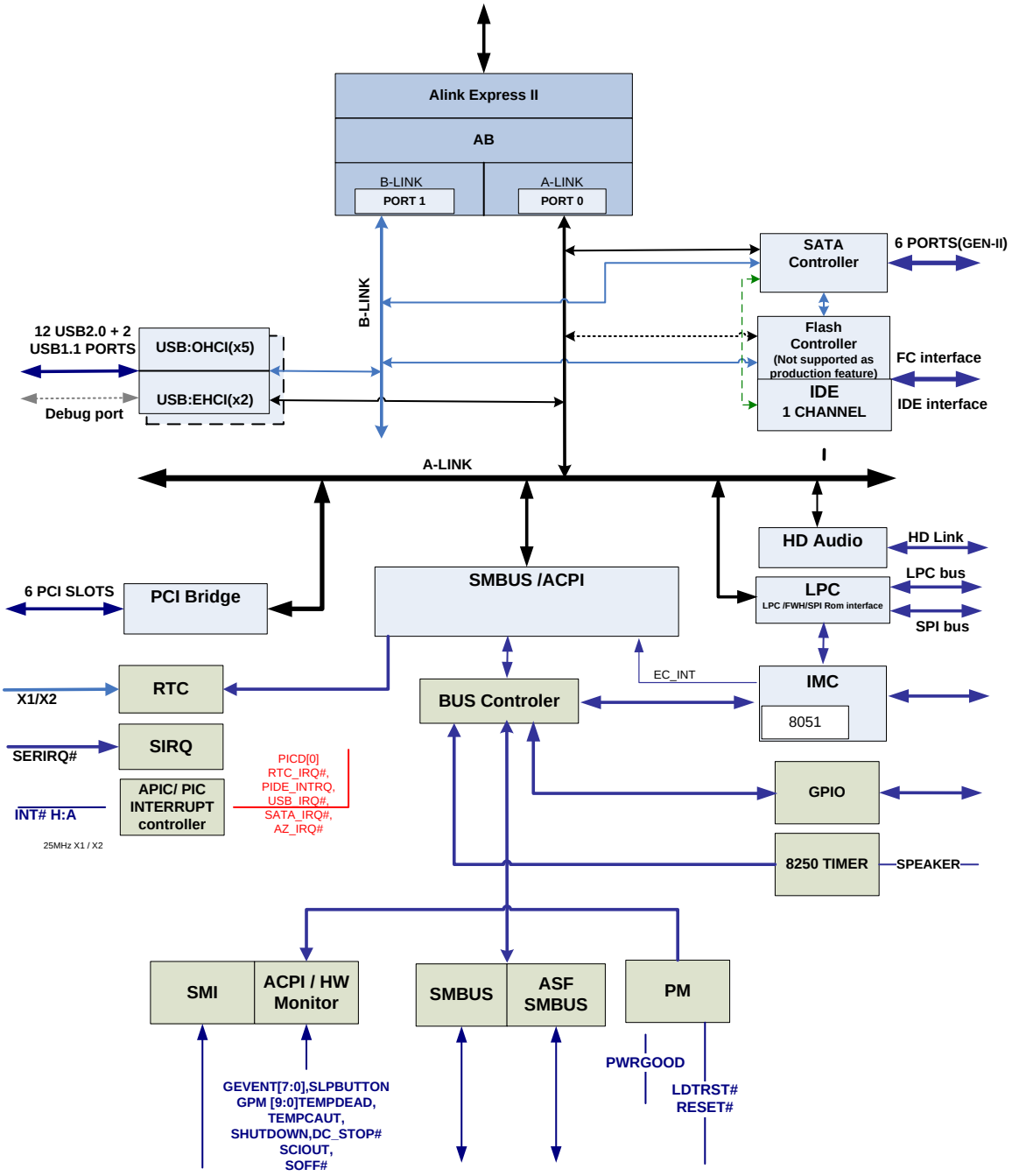


Figure 2-1: SP5100 Block Diagram Showing the Internal PCI Devices and Major Function Blocks

3 SP5100 Power on Sequence and Timing

3.1 Power Up and Down Sequences

Simple diagrams of the SP5100 power up sequences are shown in *Figure 3-1* and *Figure 3-2* below. A power detection circuit is integrated into the SP5100. This circuit will monitor SB PWR_GOOD and will assert A_RST# and LDT_RST# for as long as SB PWR_GOOD is false. After SB PWR_GOOD has been asserted, A_RST#, followed by LDT_RST#, will be de-asserted. *Table 4-1* shows the timing requirements referenced in *Figure 3-1* through *Figure 3-5*. Besides the illustrated requirements, it is also required that the ramp time for any rail be less than 40ms.

Table 3-1: SP5100 Power Up/Down Sequence Timing

Symbol	Min.	Max.	Description
T1	**Note 1**		+3.3V_S5 to +1.2V_S5
T2	10 ms	–	+3.3V_S5 to resume reset (RSMRST#).
T2A	–	50 ms	Resume reset (RSMRST#) rise time (10% to 90%). SP5100 has a Schmitt trigger input with de-bouncing logic on this pin, so the value is relaxed relative to earlier AMD SB designs.
T3	32 ms	–	RSMRST# de-asserted to Start of RTCCLK output from SP5100.
T4		50 ns	SB PWR_GOOD de-assertion to NB_PWRGD de-assertion delay.
T7	0 ns	30 ns	SB PWR_GOOD assertion to NB_PWRGD assertion delay when using the SP5100 NB_PWRGD output. This parameter is the internal delay of the SB. The system board design may add additional delay due to loading and trace length. The acceptable delay including system layout / loading is 1 ms maximum..
T7A	–	50 ms	SB PWR_GOOD rise time (10% to 90 %). See **Note 3**. SP5100 has a Schmitt trigger with de-bouncing logic on this pin, so the value is relaxed relative to earlier AMD SB designs.
T7B	–	1 ms	SB PWR_GOOD fall time.
T8A	0 ns **Note 4**	100 ns	A_RST# (PCI host bus reset) to PCIRST#.
T8B	–	**Note 5**	KBRST# to A_RST#.
T8C	1.0 ms	2.3 ms	PCIRST# to LDT_RST#.
T8D	98 ms	108 ms	NB_PWRGD to LDT_PG.
T9	101 ms	113 ms	SB PWR_GOOD to PCIRST#.
T9A	101 ms	113 ms	SB PWR_GOOD to A_RST# (T9-T8A).
T9B	31 ms	–	SB PWR_GOOD to LDT_STP#. See **Note 11**
T10	-31 ms	–	PCIE_CLKP/N stable time before SB PWRGOOD assertion.
T11	36 ms	41 ms	SB PWR_GOOD to stable PCICLK 33 MHz. See **Note 8**.
T13	–	15 ns	Wake Event (except PwrButton) to SLP_S3# / SLP_S5#.
	200 ns	–	Wake Event (PwrButton) to SLP_S3# / SLP_S5# (S5/S4/S3 → S0)
	8 ns	--	Wake Event (PwrButton) to SLP_S3# / SLP_S5# (G3 → S5 → S0)
T13A	80 ns	–	SB PWR_GOOD must be de-asserted before VDD (PS PWOK) drops more than 5% off the nominal value. See **Note 9.**
T14	1 ns	–	SB PWR_GOOD de-assertion to Resume Reset (RSMRST#) assertion. See **Note 10**.
T15	5 s	–	[Not illustrated] VBAT to +3.3V_S5 to +1.2V_S5. Must be greater than 5 seconds to allow start time for the internal RTC.
T16A	40 µs	–	LDT_STP# assertion to LDT_RST# assertion.
T16B	4 µs	–	LDT_RST# assertion to SLP_S3# assertion.

See Notes 1 to 12 in the *Power Up Sequence Timing Notes* section following the timing diagrams.

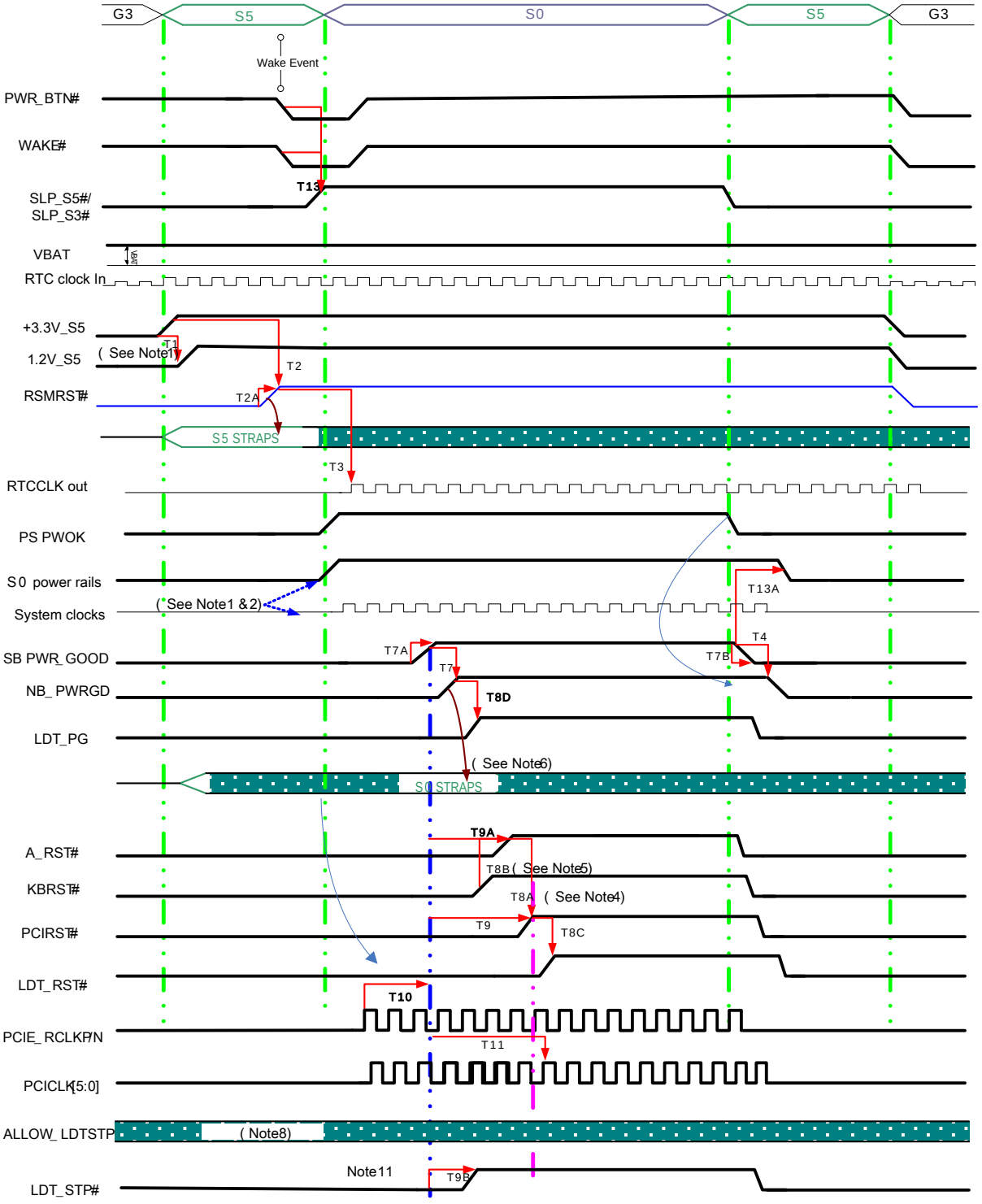


Figure 3-1: SP5100 Power Up/Down Sequence

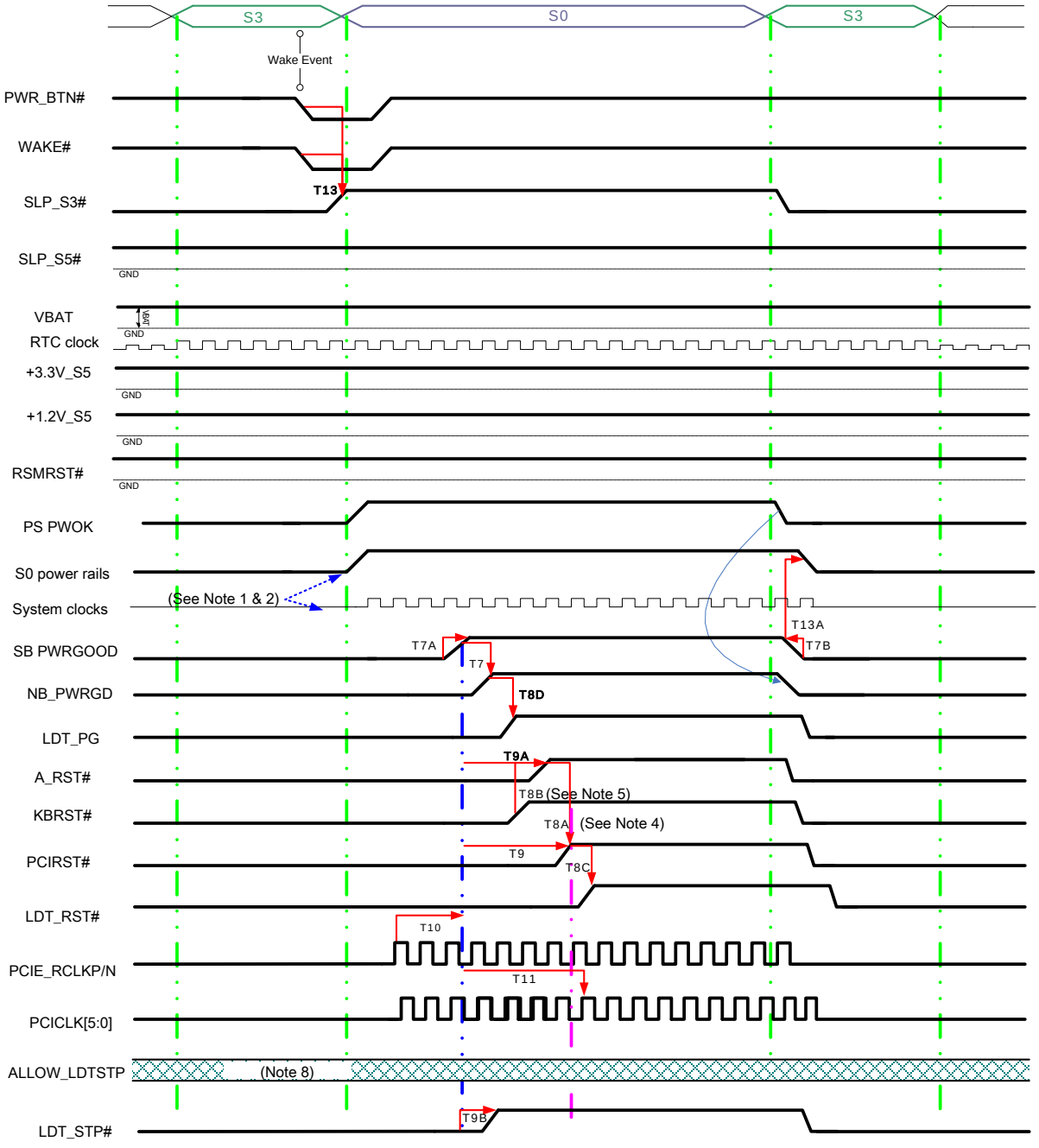


Figure 3-2: SP5100 S3/S0 Power Up/Down Sequence

Power up Sequence Timing Notes

Note 1: There is no specific power sequencing requirement other than those indicated in Note 2 below. The SP5100 power rails are grouped in four different voltages:

I. +5 V, which includes V5_VREF
II. +3.3 V, which includes VDDQ, VDD33_18 (IDE mode)
III. +1.2 V, which includes AVDDCK_1.2V, AVDD_SATA, PLLVDD_SATA, PCIE_PVDD, PCIE_VDDR, CKVDD_1.2V
IV. +1.8 V

Note 2: V5_VREF is used in the SP5100 for the 5-V PCI signal tolerance. VDDQ (+3.3 V) & VDD33_18 (3.3 V) must not exceed V5_VREF by more than 0.6 V at any time during ramp up, steady state, or ramp down. The suggested circuit below should be used to maintain relationship between V5_VREF and VDDQ and VDD33_18.

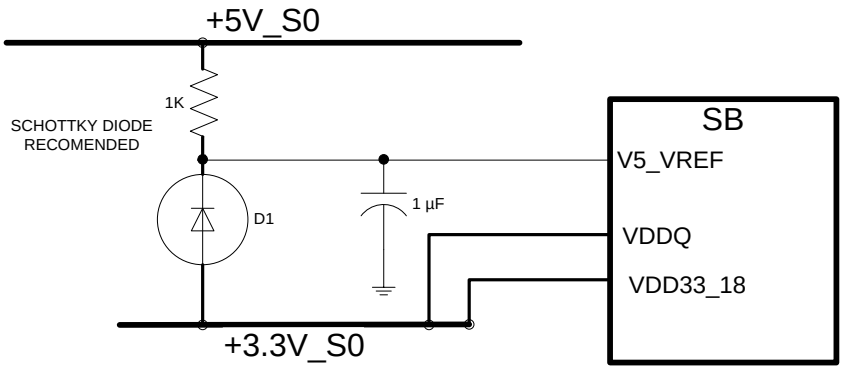


Figure 3-3: Circuit for Maintaining Proper Relationship between +V5_VREF and VDDQ

Note 3: The SP5100 will latch the straps after rising edge of SB PWR_GOOD only once. With debouncing of SB PWR_GOOD, the latching of strap will occur at approximately ~10ms after the rising edge of SB PWR_GOOD.

Note 4: Typical time between A_RST# and PCIRST# is 75 ns. The measurement should be done at 10% of both signals. Loading on the motherboard may cause the measurement at 90% be more than the spec.

Note 5: The KBRST# should be de-asserted before A_RST# (LDT_RST#) is de-asserted.

Note 6: Type II Standard and Debug straps will be latched after SB PWR_GOOD is asserted. Type I straps are latched on resume reset rising edge. Refer to *Section 4: SP5100 Strap Information* for strap timing.

Note 7: The SP5100 will not monitor the ALLOW_LDTSTP signal on power up. This signal is only used on C3 transitions.

Note 8: The PCI Clock may be stable before T11 min. under some conditions; however in all cases, the PCI Clock is guaranteed to be stable only between T11 min and max.

Note 9: The SP5100 will monitor internally the power down events and protect the internal circuit during the power down event. This includes power down during the S3, S4, and S5 states. During an unexpected power failure or G3 state, the relationship between the 1.2 V (VDD) and SB Power Good should be maintained to protect the internal logic of the SP5100.

Note 10: The following figure shows the timing of SB PWR_GOOD de-asserted to RSMRST# de-asserted during a power down sequence. However, this timing only applies to S0 to G3 state transition, because G3 state is where both signals are inactivated.

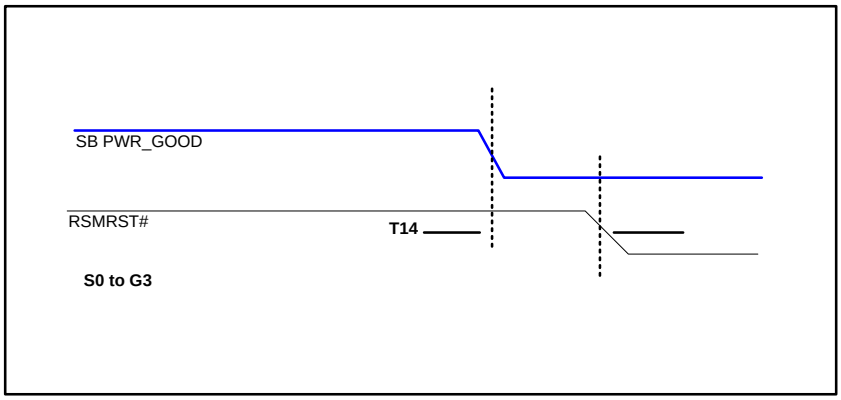


Figure 3-4: Timing for SB PWR_GOOD De-asserted to RSMRST# De-asserted

Note 11: On first power up, G3 → S5, or after RSMRST# assertion, the LDT_STP# will be asserted with CPU_VDDIO power. On subsequent power up, S5 → S0, the timing on T9B will apply.

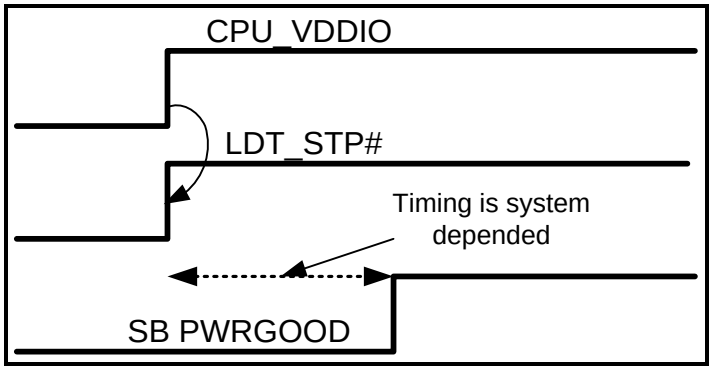


Figure 3-5: Timing for LDT_STP# assertion on first power up (G3 → S5)

Note 12: The S5_3.3V ramp down should be controlled to achieve a slew rate of 8mV/ µS or lower.

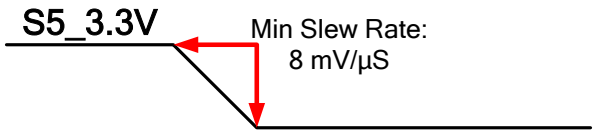


Figure 3-6: S5_3.3V Power Down Sequence Requirement

4 SP5100 Strap Information

There are two kinds of strap-latching logic, Type I and Type II. Type I straps will be latched on G3 to S5 transition on rising edge of RSMRST#. Type II straps are latched on S5 to S0 transition after rising edge of PWR_GOOD assertion.

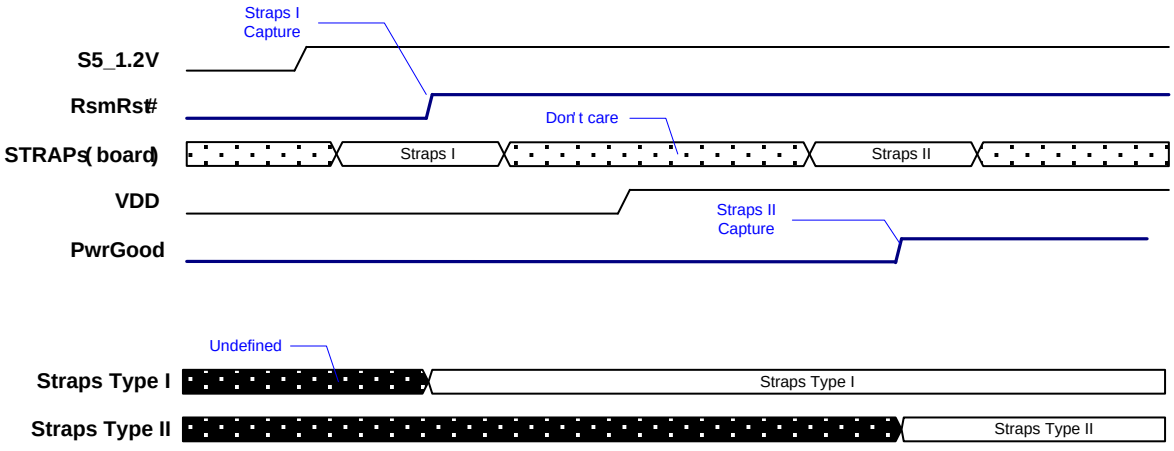


Figure 4-1: Straps Capture

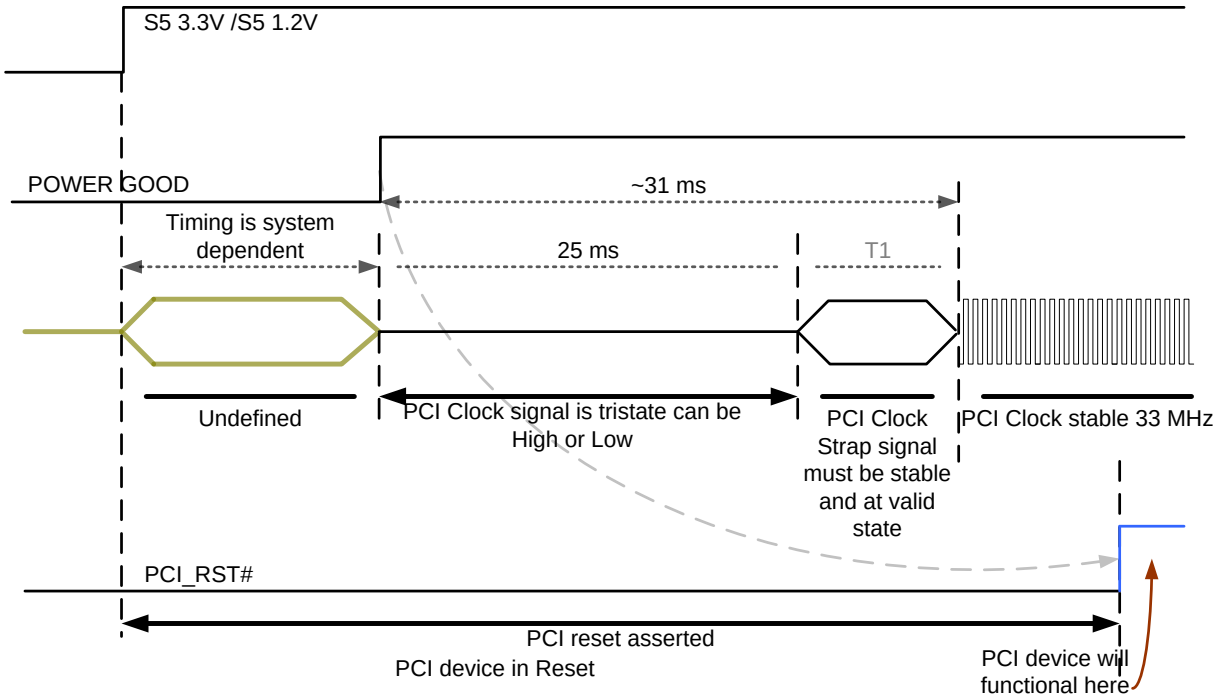


Figure 4-2: Type II Straps Capture timing

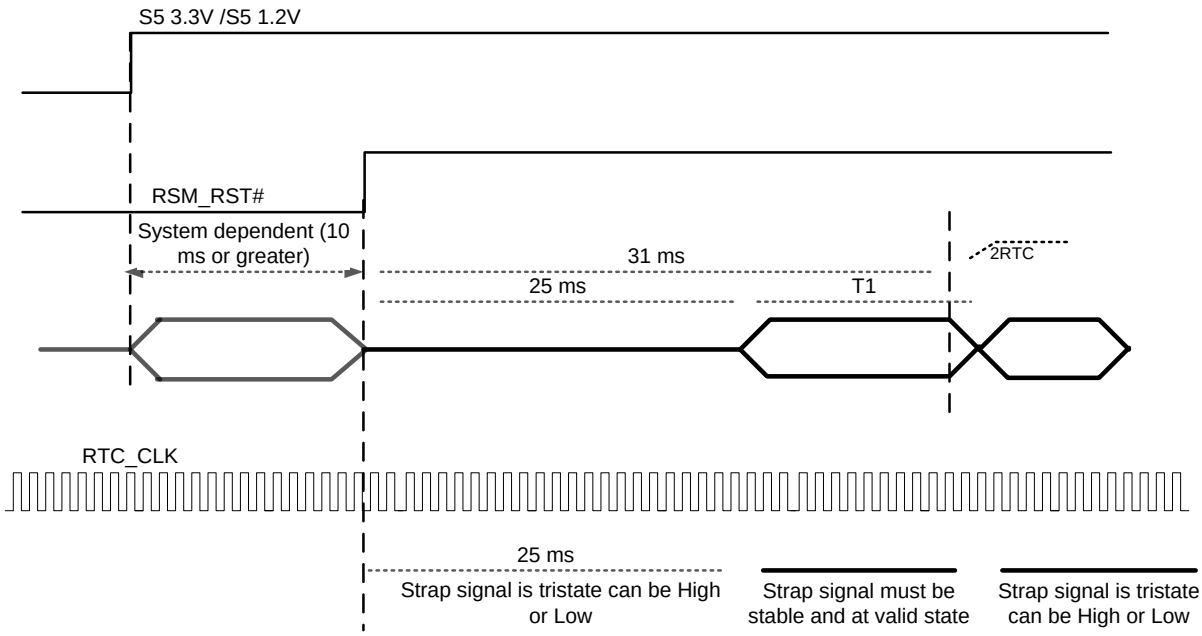


Figure 4-3: Type I Straps Capture timing

Straps are also classified in two groups, standard and debug. Straps in the standard group are used for selecting on power up the desired modes of ASIC operation and additional optional features. Straps in debug group are for debugging at the system-level, mainly during the pre-production stage. Debug straps should have provision for PU or PD so they can be configured to either option when required for debug purposes.

Table 4-1 and *Table 4-2* show the function of every strap signal in the design. All straps are defined such that in the most likely scenario of operation, they will be set to the recommended (or safest) values. The values shown in the Description column are the external board strap values, with 3.3V being a pull-up (PU) and 0V a pull-down (PD).

Table 4-1: Standard Straps

<table>
<tr><th>Pad Name</th><th>Strap Name</th><th>Type</th><th>Description</th></tr>
<tr><td>{IMCGPIO17, IMCGPIO16 }</td><td>{ ROM_TYPE_1, ROM_TYPE_0 }</td><td>I</td><td>
<table>
<tr><th>ROM_TYPE_1</th><th>ROM_TYPE_0</th><th>ROM Type</th></tr>
<tr><td>3.3 V</td><td>3.3 V</td><td>Reserved</td></tr>
<tr><td>3.3 V</td><td>0 V</td><td>SPI ROM</td></tr>
<tr><td>0 V</td><td>3.3 V</td><td>LPC ROM (Supports both LPC and PMC ROM types)</td></tr>
<tr><td>0 V</td><td>0 V</td><td>Firmware Hub</td></tr>
</table>
These two strap pins should be configured to the corresponding state that matches the Hardware ROM type installed.
</td></tr>
</table>

Pad Name	Strap Name	Type	Description
LPCCLK0	IMC_ENABLE	I	Integrated Microcontroller (IMC) 0 V – Disable IMC 3.3 V – Enable IMC
	PCI_ROM_BOOT	II	**Revision A11 strap defination** Booting from PCI memory 0 V – disable PCI ROM boot (**Default**) 3.3 V – enable PCI ROM boot **Note:** This feature is for debug pupose only. After a G3 → S5 transition the system will allow boot from PCI memory only once. Subsequent S5 → S0 transition will not boot from PCI memory.
LPCCLK1	PCIE_PLL_ENABLE	II	Enable PCI Expresse® PLL 0 V – Normal operation. PCI Express clock enabled for internal PLL reference clock. 3.3 V – Test / debug. PCI Express clock disconnected from internal PLL.
AZ_RST#	IMC_ENABLE	I	**Revision A11 strap defination** Integrated Microcontroller (IMC) 0 V – disable IMC 3.3 V – enable IMC
	PCI_ROM_BOOT	II	Booting from PCI memory 0 V – disable PCI ROM boot (**Default**) 3.3 V – enable PCI ROM boot **Note:** This feature is for debug pupose only. After a G3 → S5 transition the system will allow boot from PCI memory only once. Subsequent S5 → S0 transition will not boot from PCI memory.
PCICLK5	Reserved	—	Reserved
PCICLK4	Reserved	—	Reserved
PCICLK3	Debug_Straps	II	Enable/Disable additional straps for debugging (see Table 4-2) 0 V – use hardcoded defaults for Debug Straps (**Default**) 3.3 V – enable additional Debug Straps
PCICLK2	Watchdog_Enable	II	Watchdog function 0 V – disable watchdog function on NB_PWRGD ball 3.3 V – enable watchdog function on NB_PWRGD ball

Table 4-2: Debug Straps

Pad Name	Strap Name	Type	Description
PCI_AD30	Reserved	—	Reserved (Internal PU of 15 kΩ)
PCI_AD29	Reserved	—	Reserved (Internal PU of 15 kΩ)
PCI_AD28	Reset_Length	II	Generate a short reset 0 V – Use short reset (reserved, do not use) 3.3 V – Use long reset (**Default**) (Internal PU of 15 kΩ)

Pad Name	Strap Name	Type	Description
PCI_AD27	PCI_PLL	II	Bypass PCI PLL 0 V – Bypass internal PLL clock . Use REQ3# as A-Link bypass clock Use GNT3# as B-Link bypass clock 3.3 V – Use internal PLL-generated PLL CLK (**Default**) (Internal PU of 15 kΩ)
PCI_AD26	ACPI_BCLK	II	Bypass ACPI_BCLK 0 V – Bypass internal generated acpi_bclk. GNT0# as acpi_bclk bypass clock. 3.3 V – Use internal generated acpi_bclk (**Default**) (Internal PU of 15 kΩ)
PCI_AD25	IDE_PLL	II	Bypass IDE CLK 0 V – Bypass internal Ide Clk Use GNT2# as Ide 66-MHz bypass clock. Use REQ2# as Ide 50-MHz bypass clock. Use REQ1# as Ide 33-MHz bypass clock. 3.3 V – Use internal PLL Ide Clk (**Default**) (Internal PU of 15 kΩ).
PCI_AD24	PCIE_EEPROM	II	A-Link Express-II core strap from I2C ROM enable 0 V – Use EEPROM PCI Express straps, getting the value from I2C EPROM. I2C EPROM ADDRESS set to all zeroes. Use GNT4# as SDA Use REQ4# as SCL. 3.3 V – Use default PCI Express straps (**Default**) (Internal PU of 15 kΩ)
PCI_AD23	Reserved	—	Reserved (Internal PU of 15 kΩ)

Table 4-3: Additional Straps

The following strap is not captured by the straps logic, but is required to make the internal RTC work properly.

Pad Name	Strap Name	Description
RTCCLK	—	The pin should be pulled-up to S5_3.3V and a crystal should be put on X1/X2 to enable the internal RTC. Otherwise, the internal RTC may not function properly

5 Integrated Resistor and External Pull-up/Pull-down Resistor Requirements

Table 5-1: External Resistor Requirements and Integrated Pull-Up/Down

Interface	Signal Name	Value of Integrated / External Resistor	Resistor Type	Register for programming the integrated PU/PD
IDE	IDE_DRQ	Integrated 5.6 K	Pull-down	—
	IDE_IORDY	Integrated 4.7 K	Pull-up	—
	IDE_IRQ	Integrated 10 K	Pull-down	—
	IDE_D7/GPIO22	Integrated 27 Ω + integrated 10 K	Series + Pull-down	(See GPIO section below)
	IDE_D[15:0]/GPIO[30:23, 21:15]	Integrated 27 Ω	Series	
	IDE_A[2:0]	Integrated 27 Ω	Series	—
	IDE_CS[3,1]#	Integrated 27 Ω	Series	—
	IDE_DACK#, IOW#, IOR#,	Integrated 27 Ω	Series	——
PCI Express®	PCIE_CALRP	External 562 Ω (1% tolerance) Reference resistor for the Tx termination.	Pull-down to VSS_PCIE	
	PCIE_CALRN	External 2.05 K (1% tolerance) Reference resistor for the Rx termination	Pull-UP to VDD_PCIE	—
USB	USB_HSD[11:0]P	Integrated 15 K	Pull-down	—
	USB_HSD[11:0]N	Integrated 15 K	Pull-down	—
	USB_FSD[13:12]P	Integrated 15 K	Pull-down	—
	USB_FSD[13:12]N	Integrated 15 K	Pull-down	—
HD Audio	AZ_SDIN[2:0]/ GPIO[44:42]	Integrated 50 K	Pull-down	(See GPIO section below)
	AZ_SDIN3/GPIO46	Integrated 50 K	Pull-down	(See GPIO section below)
NB	ALLOW_LDTSTP	External Pull-up	Pull-up	—
Processor	LDT_PG	External Pull-up	Pull-up	—
	LDT_STP#	External Pull-up	Pull-up	—
	LDT_RST#	External Pull-up	Pull-up	—
PCI	INTE#/GPIO33	Integrated 8.2 K	Pull-up	(See GPIO section below)
	INTF#/GPIO34	Integrated 8.2 K	Pull-up	(See GPIO section below)
	INTG#/GPIO35	Integrated 8.2 K	Pull-up	(See GPIO section below)
	INTH#/GPIO36	Integrated 8.2 K	Pull-up	(See GPIO section below)

Interface	Signal Name	Value of Integrated / External Resistor	Resistor Type	Register for programming the integrated PU/PD
	AD[31:23]	Integrated 15 K	Pull-up	PM_REG 41h / PM_REG 40h Default: Pull-up enabled
	FRAME#	Integrated 8.2 K	Pull-up	—
	TRDY#/ROMOE#	Integrated 8.2 K	Pull-up	—
	IRDY#	Integrated 8.2 K	Pull-up	—
	DEVSEL#/ROMA0	Integrated 8.2 K	Pull-up	—
	STOP#	Integrated 8.2 K	Pull-up	—
	SERR #	Integrated 8.2 K	Pull-up	—
	PCI_PERR#	Integrated 8.2 K	Pull-up	—
	LOCK#	Integrated 8.2 K	Pull-up	—
	CLKRUN#	Integrated 8.2 K	Pull-up	—
	REQ0#	Integrated 15 K	Pull-up	—
	REQ1#	Integrated 15 K	Pull-up	—
	REQ2#	Integrated 15 K	Pull-up	—
	REQ3#/GPIO70	Integrated 15 K	Pull-up	(See GPIO section below)
	REQ4#/GPIO71	Integrated 15 K	Pull-up	(See GPIO section below)
	BMREQ#/REQ5#/GPIO65	External Pull-up if used as REQ5#	Pull-up	(See GPIO section below)
LPC/ SIO/ SPI	LAD[3:0]	Integrated 15 K	Pull-up	—
	LDRQ0#	Integrated 15 K	Pull-up	—
	LDRQ1#/GNT5#/GPIO68	Integrated 15 K	Pull-up	(See GPIO section below)
	LPC_SMI#/EXTEVNT1#	Integrated 10 K	Pull-up	(See GEVENT section below)
	SERIRQ	Integrated 8.2 K	Pull-up	—
	GA20IN	Integrated 8.2 K	Pull-up	—
	KBRST#	Integrated 8.2 K	Pull-up	—
	SPI_CLK/GPIO47	Integrated 10 K	Pull-down	(See GPIO section below)
	SPI_DI/GPIO12	Integrated 10 K	Pull-down	(See GPIO section below)
	SPI_DO/GPIO11	Integrated 10 K	Pull-down	(See GPIO section below)
	SPI_HOLD#/GPIO31	Integrated 10 K	Pull-up	—
	SPI_CS1#/GPIO32	Integrated 10 K	Pull-up	—
	SPI_CS2#/IMC_GPIO2	Integrated 10 K	Pull-up	LPC PCI config CEh; default Pull-up disabled

Interface	Signal Name	Value of Integrated / External Resistor	Resistor Type	Register for programming the integrated PU/PD
Power Manage-ment	SLP_S2/ GPM9#	Integrated 10 K	Pull-down	PM2_Rg F8h Default: Pull-down enabled
	PWR_BTN#	Integrated 10 K	Pull-up	—
	PWR_GOOD	Integrated 10 K	Pull-up	—
	TEST[1:0]	Integrated 10 K	Pull-down	—
	TEST2	Integrated 10 K	Pull-down	—
	RTCCLK	Integrated 10 K	Pull-up	PM_Reg: 0Eh Default: Pull-up enabled.
	FANOUT0/GPIO3	Integrated 10 K	Pull-up	—
	FANOUT1/GPIO48	Integrated 8.2 K	Pull-up	—
	FANOUT2/GPIO49	Integrated 8.2 K	Pull-up	—
	RSMRST#	Integrated 10 K	Pull-up	—
General Events/ GPM/ GPIO	RI#/EXTEVNT0#	Integrated 10 K	Pull-up	PM2_Rg F5h Default: Pull-up enabled
	LPC_SMI#/EXTEVNT1#	Integrated 8.2 K	Pull-up	PM2_Rg F5h Default: Pull-up enabled
	SMBALERT#/THRMTRIP#/ GEVENT2#	Integrated 10 K	Pull-up	PM2_Rg F3h Default: Pull-up enabled
	LPC_PME#/GEVENT3#	Integrated 10 K	Pull-up	PM2_Rg F3h Default: Pull-up enabled
	PCI_PME#/GEVENT4#	Integrated 10 K	Pull-up	PM2_Rg F4h Default: Pull-up enabled
	S3_STATE/GEVENT5#	GEVENT5#: Integrated 10 K S3_STATE: Push/Pull	Pull-up	PM2_Rg F4h Default: Pull-up enabled
	USB_OC6#/GEVENT6#	Integrated 10 K	Pull-up	PM2_Rg F4h Default: Pull-up enabled
	GEVENT7#	Integrated 10 K	Pull-up	PM2_Rg F4h Default: Pull-up enabled
	WAKE#/GEVENT8#	Integrated 10 K	Pull-up	PM2_Rg F5h Default: Pull-up enabled
	USB_OC0#/GPM0#	Integrated 10 K	Pull-up	PM2_Rg F6h Default: Pull-up enabled
	USB_OC1#/GPM1#	Integrated 10 K	Pull-up	PM2_Rg F6h Default: Pull-up enabled
	USB_OC2#/GPM2#	Integrated 10 K	Pull-up	PM2_Rg F6h Default: Pull-up enabled

Interface	Signal Name	Value of Integrated / External Resistor	Resistor Type	Register for programming the integrated PU/PD
	USB_OC3#/GPM3#	Integrated 10 K	Pull-up	PM2_Rg F6h Default: Pull-up enabled
	USB_OC4#/GPM4#	Integrated 10 K	Pull-up	PM2_Rg F7h Default: Pull-up enabled
	USB_OC5#/GPM5#	Integrated 10 K	Pull-up	PM2_Rg F7h Default: Pull-up not enabled
	BLINK/GPM6#	Integrated 10 K	Pull-up	PM2_Rg F7h Default: Pull-up enabled
	SYS_RESET#/GPM7#	Integrated 10 K	Pull-up	PM2_Rg F7h Default: Pull-up enabled
	USB_OC8#/AZ_DOCK_RST#/ GPM8#	Integrated 10 K	Pull-up	PM2_Rg F8h Default: Pull-up enabled
	SLP_S2/ GPM9#	Integrated 10 K	Pull-down	PM2_Rg F8h Default: Pull-down enabled
GPIO	CLK_REQ0#/SATA_IS3#/ GPIO0	Integrated 10 K	Pull-down	PM2_Rg E0h Default: Pull-down enabled
	SPKR/GPIO2	Integrated 8.2 K	Pull-up	PM2_Rg E0h Default: Pull-up/Pull-down not enabled
	FANOUT0/GPIO3	Integrated 8.2 K	Pull-up	PM2_Rg E0h Default: Pull-up enabled
	SMARTVOLT1/SATA_IS2#/ GPIO4	Integrated 8.2 K	See **Note**	PM2_Rg E1h Default: Pull-up/Pull-down not enabled
	SMARTVOLT2/SHUTDOWN#/ GPIO5	Integrated 8.2 K	See **Note**	PM2_Rg E1h Default: Pull-up/Pull-down not enabled
	CLK_REQ3#/SATA_IS1#/GPIO6	Integrated 8.2 K	See **Note**	PM2_Rg E1h Default: Pull-up/Pull-down not enabled
	NB_PWRGD	Integrated 10 K	See **Note**	PM2_Rg E1h Default: Pull-up/Pull-down not enabled
	DDC1_SDA/GPIO8	Integrated 8.2 K	See **Note**	PM2_Rg E2h Default: Pull-up/Pull-down not enabled
	DDC1_SCL/GPIO9	Integrated 8.2 K	See **Note**	PM2_Rg E2h Default: Pull-up/Pull-down not enabled
	SATA_IS0#/GPIO10	Integrated 8.2 K	See **Note**	PM2_Rg E2h Default: Pull-up/Pull-down not enabled

Interface	Signal Name	Value of Integrated / External Resistor	Resistor Type	Register for programming the integrated PU/PD
	SPI_DO/GPIO11	Integrated 10 K	Pull down	PM2_Rg E2h Default: Pull-down Enabled
	SPI_DI/GPIO12	Integrated 10 K	Pull down	PM2_Rg E3h Default: Pull-down Enabled
	LAN_RST#/GPIO13	Integrated 8.2 K	See **Note**	PM2_Rg E3h Default: Pull-up/Pull-down not enabled
	ROM_RST#/GPIO14	Integrated 10 K	See **Note**	PM2_Rg E3h Default: Pull-up/Pull-down not enabled
	IDE_D0/FC_ADQ0/GPIO15	Integrated 27 Ω	Series	PM2_Rg E3h Default: Pull-up/Pull-down not enabled
	IDE_D1/FC_ADQ1/GPIO16	Integrated 27 Ω	Series	PM2_Rg E4h Default: Pull-up/Pull-down not enabled
	IDE_D2/FC_ADQ2/GPIO17	Integrated 27 Ω	Series	PM2_Rg E4h Default: Pull-up/Pull-down not enabled
	IDE_D3/FC_ADQ3/GPIO18	Integrated 27 Ω	Series	PM2_Rg E4h Default: Pull-up/Pull-down not enabled
	IDE_D4/FC_ADQ4/GPIO19	Integrated 27 Ω	Series	PM2_Rg E4h Default: Pull-up/Pull-down not enabled
	IDE_D5/FC_ADQ5/GPIO20	Integrated 27 Ω	Series	PM2_Rg E5h Default: Pull-down not enabled
	IDE_D6/FC_ADQ6/GPIO21	Integrated 27 Ω	Series	PM2_Rg E5h Default: Pull-up/Pull-down not enabled
	IDE_D7/FC_ADQ7/GPIO22	Integrated 27 Ω + integrated 10 K	Series + Pull-down	PM2_Rg E5h Default: Pull-down not enabled
	IDE_D8/FC_ADQ8/GPIO23	Integrated 27 Ω	Series	PM2_Rg E5h Default: Pull-down not enabled
	IDE_D9/FC_ADQ9/GPIO24	Integrated 27 Ω	Series	PM2_Rg E6h Default: Pull-down not enabled
	IDE_D10/FC_ADQ10/GPIO25	Integrated 27 Ω	Series	PM2_Rg E6h Default: Pull-down not enabled
	IDE_D11/FC_ADQ11/GPIO26	Integrated 27 Ω	Series	PM2_Rg E6h Default: Pull-down not enabled
	IDE_D12/FC_ADQ12/GPIO27	Integrated 27 Ω	Series	PM2_Rg E6h Default: Pull-down not enabled

Interface	Signal Name	Value of Integrated / External Resistor	Resistor Type	Register for programming the integrated PU/PD
	IDE_D13/FC_ADQ13/GPIO28	Integrated 27 Ω	Series	PM2_Rg E7h Default: Pull-up/Pull-down not enabled
	IDE_D14/FC_ADQ14/GPIO29	Integrated 27 Ω	Series	PM2_Rg E7h Default: Pull-up/Pull-down not enabled
	IDE_D15/FC_ADQ15/GPIO30	Integrated 27 Ω	Series	PM2_Rg E7h Default: Pull-up/Pull-down not enabled
	SPI_HOLD#/GPIO31	Integrated 10 K	Pull-Up	PM2_Rg E7h Default: Pull-up enabled
	SPI_CS1#/GPIO32	Integrated 10 K	Pull-up	PM2_Rg E8h Default: Pull-up enabled
	INTE#/GPIO33	Integrated 8.2 K	Pull-up	PM2_Rg E8h Default: Pull-up enabled
	INTF#/GPIO34	Integrated 8.2 K	Pull-up	PM2_Rg E8h Default: Pull-up enabled
	INTG#/GPIO35	Integrated 8.2 K	Pull-up	PM2_Rg E8h Default: Pull-up enabled
	INTH#/GPIO36	Integrated 8.2 K	Pull-up	PM2_Rg E9h Default: Pull-up enabled
	CLK_REQ1#/SATA_IS4/ FANOUT3/GPIO39	Integrated 8.2 K	Pull-down	PM2_Rg E9h Default: Pull-down enabled
	CLK_REQ2#/SATA_IS5/ FANIN3/GPIO40	Integrated 8.2 K	Pull-down	PM2_Rg EAh Default: Pull-down enabled
	AZ_SDIN[2:0]/ GPIO[44:42]	Integrated 50 K	Pull-down	PM2_Rg EAh Default: Pull-down enabled
	AZ_SDIN3/GPIO46	Integrated 50 K	Pull-down	PM2_Rg EBh. Default: Pull-down enabled
	SPI_CLK/GPIO47	Integrated 10 K	Pull-down	PM2_Rg EBh. Default: Pull-down enabled
	FANOUT1/GPIO48	Integrated 8.2 K	Pull-up	PM2_Rg ECh. Default: Pull-up enabled
	FANOUT2/GPIO49	Integrated 8.2 K	Pull-up	PM2_Rg ECh. Default: Pull-up enabled
	GPIO 64:50	Integrated 10 K	See **Note**	PM2_rg F0h:ECh Default: Pull-up/Pull-down not enabled

Interface	Signal Name	Value of Integrated / External Resistor	Resistor Type	Register for programming the integrated PU/PD
	BMREQ#/REQ5#/GPIO65	Integrated 8.2 K	See **Note**	PM2_Rg F0h Default: Pull-up/Pull-down not enabled
	LLB#/GPIO66	Integrated 10 K	Pull-up	PM2_Rg F0h Default: Pull-up enabled
	SATA_ACT#/GPIO67	Integrated 8.2 K	See **Note**	PM2_Rg F0h Default: Pull-up/Pull-down not enabled
	LDRQ1#/GNT5#/GPIO68	Integrated 15 K	Pull-up	PM2_Rg F1h Default: Pull-up enabled
	REQ3#/GPIO70	Integrated 15 K	Pull-up	PM2_Rg F1h Default: Pull-up enabled
	REQ4#/GPIO71	Integrated 15 K	Pull-up	PM2_Rg F1h Default: Pull-up enabled
	GNT3#/GPIO72	Integrated 8.2 K	See **Note**	PM2_rg F2h Default: Pull-up/Pull-down not enabled
	GNT4#/GPIO73	Integrated 8.2 K	See **Note**	PM2_rg F2h Default Pull-up/Pull-down not enabled
IMC GPIO	IMC_GPIO	Integrated 10 K		LPC PCI config DCh:CCh. Default: Pull-up/Pull-down not enabled

Note: The pin has an internal integrated pull-up or pull-down resistor that is not enabled by default. The pin's default function does not require a pull-up or pull-down. However, if the pin is used for an alternate function and a pull-up or pull-down is required, the internal resistor can be enabled by the indicated register.

6 SP5100 Ballout Map

21 mm x 21 mm 528 Ball BGA with 0.8 mm pitch.

	1	2	3	4	5	6	7	8	9	10	11	12	13
A		VSS_1	X1	VIN0/GPIO53	TEMPIN2/GPIO63	TEMPIN1/GPIO62	VIN6/GPIO59	USB_OC4#/IR_RX0/GPM4#	USB_OC3#/IR_RX1/GPM3#	USB_PHY_1.2V_1	USB_HSD9P	USB_HSD4N	USB_HSD1P
B	VSS_3	VBAT	X2	VIN1/GPIO54	TEMPIN3/TALERT#/GPIO64	TEMPIN0/GPIO61	VIN7/GPIO60	USB_OC5#/IR_TX0/GPM5#	USB_OC6#/IR_TX1/GEVENT6#	USB_PHY_1.2V_2	USB_HSD9N	USB_HSD4P	USB_HSD1N
C	LLB#/GPIO66	INTRUDER_ALERT#	RTCCLK	VIN2/GPIO55		TEMP_COMM		USBCLK/14M_25M_48M_OSC		USB_HSD8P		USB_HSD5P	
D	SPI_CLK/GPIO47	SPI_DO/GPIO11	RSMRST#	VIN3/GPIO56	VIN4/GPIO57	VIN5/GPIO58	VSS_4	AVSS_USB_4	AVSS_USB_5	USB_HSD8N	AVSS_USB_6	USB_HSD5N	AVSS_USB_7
E	PCI_PME#/GEVENT4#	RI#/EXTEVNT0#		USB_OC0#/GPM0#	USB_OC2#/GPM2#	USB_FSD13P	USB_FSD13N	USB_FSD12N	AVDDC		USB_HSD10P	USB_HSD6P	
F	S3_STATE/GEVENT5#	BLINK/GPM6#	SPI_CS1#/GPIO32	SPI_HOLD#/GPIO31	SLP_S3#	AVDD	USB_FSD12P	USB_OC1#/GPM1#	AVSSC		USB_HSD10N	AVSS_USB_11	
G	SLP_S5#	S5_1.2V_1		S5_1.2V_2	DDR3_RST#/GEVENT7#	SPI_DI/GPIO12	AVSS	USB_RCOMP	AVSS_USB_13		USB_HSD7P	USB_HSD3P	
H	PWR_GOOD	PWR_BTN#	TEST0	TEST1	TEST2	WAKE#/GEVENT8#	SLP_S2/GPM9#	VSS_7	AVSS_USB_14		USB_HSD11P	USB_HSD7N	
J	ROM_RST#/GPIO14	SYS_RESET#/GPM7#		S5_3.3V_4	S5_3.3V_5	SMBALERT#/THRMTRIP#/GEVENT2#	AZ_SDIN0/GPIO42	AZ_SDIN1/GPIO43	AVSS_USB_16	USB_HSD11N	AVSS_USB_17	AVSS_USB_18	
K	SCL1/GPOC2#	SDA1/GPOC3#	SUS_STAT#	LPC_PME#/GEVENT3#					VSS_8	AVSS_USB_21	VSS_9	AVSS_USB_22	
L	S5_3.3V_6	S5_3.3V_7		VSS_11	AZ_DOCK_RST#/GPM8#	AZ_SYNC	VSS_12	AZ_SDIN2/GPIO44	VDDQ_1	VSS_13	VSS_14	VSS_15	
M	AZ_BITCLK	AZ_SDOUT	AZ_SDIN3/GPIO46	AZ_RST#	FANOUT1/GPIO48	VSS_18	FANOUT2/GPIO49	FANOUT0/GPIO3	VDDQ_2	VSS_19	VSS_20	VDD_2	VSS_21
N	PCIRST#	A_RST#		VSS_23								VSS_24	VDD_4
P	PCICLK2	PCICLK3	PCICLK1	PCICLK0	FANIN0/GPIO50	VSS_26	AD1	FANIN1/GPIO51	VSS_27	VSS_28	VSS_29	VDD_5	VSS_30
R	VSS_32	VSS_33		VSS_34	AD13	AD11	AD12	FANIN2/GPIO52	VSS_35	VSS_36	VDD_7	VSS_37	
T	AD3	AD8	PCICLK5/GPIO41	PCICLK4					AD10	AVSS_SATA_1	VSS_39	VSS_40	
U	AD5	AD0		VSS_42	AD15	PAR	CBE1#	AD14	VDDQ_4	AVSS_SATA_2	AVSS_SATA_3	AVSS_SATA_4	
V	AD6	AD7	AD4	AD2	LOCK#	VSS_44	SERR#	VDDQ_7	AD18		AVSS_SATA_5	SATA_CAL	
W	AD9	CBE0#		PERR#	DEVSEL#	STOP#	VDDQ_8	AD17	AVSS_SATA_7		SATA_ACT#/GPIO67	XTLVDD_SATA	
Y	CBE3#	AD23	AD22	AD21	TRDY#	VDDQ_9	AD16	AD19	AVSS_SATA_8		AVSS_SATA_9	SATA_X1	
AA	AD26	AD24		VDDQ_10	IRDY#	FRAME#	CBE2#	AD20	AVSS_SATA_12		PLLVDD_SATA	SATA_X2	
AB	VSS_46	AD28	AD27	AD25	VDDQ_11	REQ4#/GPIO71	REQ2#	LDRQ1#/GNT5#/GPIO68	AVSS_SATA_13	SATA_RX0N	AVSS_SATA_14	SATA_TX2P	AVSS_SATA_15
AC	AD29	AD30	REQ0#	INTF#/GPIO34		GNT3#/GPIO72		AVSS_SATA_18		SATA_RX0P		SATA_TX2N	
AD	AD31	GNT0#	INTE#/GPIO33	REQ1#	GNT2#	CLKRUN#	BMREQ#/REQ5#/GPIO65	AVSS_SATA_19	SATA_TX0P	SATA_TX1N	SATA_RX1N	SATA_RX2P	SATA_TX3P
AE	VSS_49	INTG#/GPIO35	INTH#/GPIO36	GNT1#	GNT4#/GPIO73	REQ3#/GPIO70	V5_VREF	AVSS_SATA_20	SATA_TX0N	SATA_TX1P	SATA_RX1P	SATA_RX2N	SATA_TX3N
	1	2	3	4	5	6	7	8	9	10	11	12	13

Figure 6-1: SP5100 Ball-out Assignment (Left)

14	15	16	17	18	19	20	21	22	23	24	25	
USB_HSD0N	AVSS_USB_1	AVDDTX_0	S5_3.3V_1	IMC_GPIO8	IMC_GPIO39	IMC_GPIO36	IMC_GPIO33	IMC_GPIO30	IMC_GPIO28	S5_3.3V_2	VSS_2	A
USB_HSD0P	AVSS_USB_2	AVDDTX_1	S5_3.3V_3	IMC_GPIO9	IMC_GPIO38	IMC_GPIO37	IMC_GPIO32	IMC_GPIO31	IMC_GPIO27	IMC_GPIO26	IMC_GPIO24	B
AVSS_USB_3		AVDDTX_2		IMC_GPIO41		IMC_GPIO35		IMC_GPIO29	IMC_GPIO25	IMC_GPIO23	IMC_GPIO22	C
AVSS_USB_8	AVSS_USB_9	AVDDTX_3	AVDDTX_4	IMC_GPIO40	IMC_PWM2/IMC_GPO16	IMC_GPIO34	SCL2/IMC_GPIO11	IMC_GPIO4	IMC_GPIO7	IMC_GPIO21	IMC_GPIO20	D
USB_HSD6N	AVSS_USB_10		AVDDTX_5	IMC_PWM3/IMC_GPO17	IMC_PWM1/IMC_GPIO15	SCL3_LV/IMC_GPIO13	SDA3_LV/IMC_GPIO14	LPCCLK1		IMC_GPIO5	IMC_GPIO6	E
AVSS_USB_12	AVDDRX_0		AVDDRX_1	AVDDRX_2	SDA2/IMC_GPIO12	VSS_5	IMC_PWM0/IMC_GPIO10	LDT_PG	ALLOW_LDTSTP	PROCHOT#	IDE_RST#/F_RST#/IMC_GPO3	F
USB_HSD3N	AVDDRX_3		AVDDRX_4	AVDDRX_5	VSS_6	IMC_GPIO18	IMC_GPIO19	LPCCLK0		LDT_RST#	LDT_STP#	G
USB_HSD2P	USB_HSD2N		AVSS_USB_15	PCIE_CK_VSS_1	IMC_GPIO0	IMC_GPIO1	SPI_CS2#/IMC_GPIO2	LDRQ0#	LAD1	LAD0	LFRAME#	H
AVSS_USB_19	AVSS_USB_20	AVDDCK_3.3V	PCIE_CK_VSS_2	GPP_CLK0N	GPP_CLK0P	14M_X2*	14M_X1*	PCIE_CK_VSS_3		LAD3	LAD2	J
AVSS_USB_23	AVSS_USB_24	VSS_10	AVDDCK_1.2V					NB_DISP_CLKN	NB_DISP_CLKP	LPC_SMI#/EXTEVNT1#	PCIE_CK_VSS_4	K
VSS_16	VDD_1	VSS_17	AVSSCK	25M_48M_66M_OSC	GPP_CLK1N	GPP_CLK1P	CKVDD_1.2V_1	CKVDD_1.2V_2		CKVDD_1.2V_3	CKVDD_1.2V_4	L
VDD_3	VSS_22	PCIE_CK_VSS_5	PCIE_CK_VSS_6	CPU_HT_CLKN	GPP_CLK2P	GPP_CLK2N	PCIE_CK_VSS_7	SLT_GFX_CLKN	SLT_GFX_CLKP	NB_HT_CLKP	NB_HT_CLKN	M
VSS_25								GPP_CLK3P		PCIE_RCLKN/NB_LNK_CLKN	PCIE_RCLKP/NB_LNK_CLKP	N
VDD_6	VSS_31	PCIE_CK_VSS_8	CPU_HT_CLKP	PCIE_VDDR_1	PCIE_VDDR_2	PCIE_VDDR_3	PCIE_VDDR_4	GPP_CLK3N	PCIE_CK_VSS_9	PCIE_PVDD	PCIE_PVSS	P
VSS_38	VDD_8	PCIE_CK_VSS_10	PCIE_RX3N	PCIE_RX3P	PCIE_CK_VSS_11	PCIE_RX2P	PCIE_RX2N	PCIE_VDDR_5		PCIE_VDDR_6	PCIE_VDDR_7	R
VSS_41	VDDQ_3	VDD_9	PCIE_CK_VSS_12					PCIE_TX3N	PCIE_TX3P	PCIE_CALRN	PCIE_CALRP	T
VSS_43	LAN_RST#/GPIO13	VDDQ_5	VDDQ_6	PCIE_CK_VSS_13	PCIE_RX1P	PCIE_CK_VSS_14	PCIE_RX0N	PCIE_RX0P		PCIE_TX2N	PCIE_TX2P	U
AVSS_SATA_6	SERIRQ		CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39	PCIE_CK_VSS_15	PCIE_RX1N	PCIE_CK_VSS_16	PCIE_CK_VSS_17	PCIE_TX0N	PCIE_TX0P	PCIE_TX1P	PCIE_TX1N	V
NB_PWRGD	KBRST#/GEVENT1#		CLK_REQ0#/SATA_IS3#/GPIO0	SDA0/GPOC1#	PCIE_CK_VSS_18	CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40	SPKR/GPIO2	PCIE_CK_VSS_19		PCIE_CK_VSS_20	PCIE_CK_VSS_21	W
AVSS_SATA_10	GA20IN/GEVENT0#		AVSS_SATA_11	DDC1_SDA/GPIO8	SMARTVOLT2/SHUTDOWN#/GPIO5	VDD33_18_1	VSS_45	IDE_A0	IDE_A2	IDE_CS3#	IDE_CS1#	Y
AVDD_SATA_1	AVDD_SATA_2		AVDD_SATA_3	SCL0/GPOC0#	SMARTVOLT1/SATA_IS2#/GPIO4	DDC1_SCL/GPIO9	VDD33_18_2	VDD33_18_3		IDE_IORDY	IDE_IRQ	AA
SATA_RX3N	AVSS_SATA_16	SATA_TX5P	AVSS_SATA_17	AVDD_SATA_4	VSS_47	IDE_D6/GPIO21	VDDQ_12	IDE_D12/GPIO27	IDE_A1	IDE_DACK#	VSS_48	AB
SATA_RX3P		SATA_TX5N		AVDD_SATA_5		IDE_D9/GPIO24		IDE_D3/GPIO18	IDE_D15/GPIO30	IDE_IOW#	IDE_IOR#	AC
SATA_TX4N	SATA_RX4N	SATA_RX5P	AVDD_SATA_6	CLK_REQ3#/SATA_IS1#/GPIO6	IDE_D7/GPIO22	IDE_D10/GPIO25	IDE_D4/GPIO19	IDE_D13/GPIO28	IDE_D1/GPIO16	IDE_D0/GPIO15	IDE_DRQ	AD
SATA_TX4P	SATA_RX4P	SATA_RX5N	AVDD_SATA_7	SATA_IS0#/GPIO10	IDE_D8/GPIO23	IDE_D5/GPIO20	IDE_D11/GPIO26	IDE_D2/GPIO17	IDE_D14/GPIO29	VSS_50	VDD33_18_4	AE
14	15	16	17	18	19	20	21	22	23	24	25	

Figure 6-2: SP5100 Ball-out Assignment (Right)

7 Signal Description

7.1 CPU Interface

Pin name	Type	Voltage	Functional Description
LDT_PG	OD	S5_3.3V	LDT Power Good
LDT_RST#	OD	S5_3.3V	LDT Reset# LDT Reset#: Reset signal to the CPU. Assertion of LDT_RST# causes the CPU to transition into a low power state and to de-assert MEMCLKEA/B and assert MEMREST_L. Assertion of LDT_RST# takes place sometime after SB PWR_GOOD has been de-asserted. De-assertion of LDT_RST# allows MEMRESET_L to be de-asserted and MEMCLK to be enabled. De-assertion of LDT_RST# takes place sometime after SB PWR_GOOD has been asserted.
LDT_STP#	OD	S5_3.3V	Assertion of LDTSTOP# on the CPU causes it to enter C3, or S1/S2/S3/S4/S5. Assertion takes place: (a) for S1/S2/S3/S4/S5: after SUS_STAT# is asserted; (b) for C3: after the STPGNT message is received by the system. De-assertion of LDTSTOP_L causes the CPU to return to C0 or S0 state. De-assertion takes place following a wake-up event: (a) in S1: at an interval (programmed by an SB register) after de-assertion of CPU_STP#; (b) in S2: after SLP_S2 is de-asserted; (c) in S3/S4/S5: after SB PWR_GOOD is asserted; (d) in C3: at an interval (programmed by an SB register) Starting with RS78x, NB will control the LDT_STP# during C state.
PROCHOT#	I	0.8-V threshold, S5_3.3V domain	Processor Hot: Similar to TALERT#. When it is asserted, it can generate SCI or SMI to OS/BIOS.

7.2 LPC Interface

Pin Name	Type	Voltage	Functional Description
GA20IN	I	3.3 V	A20 Gate Input from SIO
KBRST#	I	3.3 V	Keyboard reset#
LAD[3:0]	I/O	S5_3.3 V	Multiplexed Command/Address/Data [3:0]
LPCCLK0	O	S5_3.3 V	LPCCLK 0 (See **Note**)
LPCCLK1	O	S5_3.3 V	LPCCLK 1 (See **Note**)
LFRAME#	O	S5_3.3 V	Frame. Indicates start of a new cycle or termination of broken cycle.
LDRQ0#	I	S5_3.3 V	Encoded DMA/Bus Master Request 0
LDRQ1#/GNT5#/ GPIO68	I/O	3.3 V	Encoded DMA/Bus Master Request 1 / PCI bus Grant 5 from SP5100 / GPIO 68
LPC_SMI#/EXTEVNT1#	I	S5_3.3 V	LPC SMI / External Event 1
SERIRQ	I/O	3.3 V	Serial IRQ

Note: LPCCLK[1:0] can be assigned to any LPC device. LPCCLK0 will be active during S2 – S5 states if the IMC is enabled. LPCCLK1 will be disabled in S2 to S5 states. PCI Clock can be used for additional LPC devices that do not require clock in S2 –S5 states.

7.3 A-Link Express II Interface

Pin Name	Type	Voltage	Functional Description
PCIE_TX[3:0]P	O	1.2 V (Filtered)	A-Link Express II Lane 3-0 Transmit Positive
PCIE_TX[3:0]N	O		A-Link Express II Lane 3-0 Transmit Negative
PCIE_RX[3:0]P	I		A-Link Express II Lane 3-0 Receive Positive
PCIE_RX[3:0]N	I		A-Link Express II Lane 3-0 Receive Negative
PCIE_RCLKP	I/O		A-Link Express II Reference Clock Positive
PCIE_RCLKN	I/O		A-Link Express II Reference Clock Negative
PCIE_CALRP	O		A-Link Express II Calibration, TX termination reference resistor connection
PCIE_CALRN	O		A-Link Express II Calibration, RX termination reference resistor connection

7.4 PCI Interface (PCI Host Bus and Internal PCI/PCI Bridge)

Pin Name	Type	Voltage	Functional Description
AD[31:0]	I/O	3.3 V (5-V Tolerance)	PCI Bus Address/Data [31:0]
BMREQ#/REQ5#/ GPIO65	I/O	3.3 V (5-V Tolerance)	Bus master REQ# / PCI Request 5 Input / GPIO 65
CBE[3:0]#	I/O	3.3 V (5-V Tolerance)	Command/Byte Enable[3:0]
CLKRUN#	I/O	3.3 V (5-V Tolerance)	Clock running is de-asserted by the clock provider to indicate the system is about to shut down the PCI clock. When it is driven low by other agents, it means the agent is requesting the clock provider not to deactivate the clock.
DEVSEL#	I/O	3.3 V (5-V Tolerance)	Device Select Device Select: driven by target to indicate it has decoded its address as the target of the current access.
FRAME#	I/O	3.3 V (5-V Tolerance)	Cycle Frame: driven by the current master to indicate the beginning and duration of an access.
GNT#[2:0]	O	3.3 V (5-V Tolerance)	PCI Bus Grant [2:0] from the SP5100: indicates to the agent that access to the bus has been granted.
GNT3#/GPIO72	O	3.3 V (5-V Tolerance)	PCI Bus Grant 3 from SP5100 / GPIO 72
GNT4#/GPIO73	I/O	3.3 V (5-V Tolerance)	PCI Bus Grant 4 from SP5100 / GPIO 73
INT[H:E]#/GPIO[36:33]	I/O	3.3 V (5-V Tolerance)	PCI Interrupt [H:E] / GPIO [36:33]
IRDY#	I/O	3.3 V (5-V Tolerance)	Initiator Ready: indicates the initiating agent's ability to complete the current data phase of the transaction
LDRQ1#/GNT5#/ GPIO68	I/O	3.3 V (5-V Tolerance)	Encoded DMA/Bus Master Request 1 / PCI bus Grant 5 from SP5100 /GPIO 68
LOCK#	I/OD	3.3 V (5-V Tolerance)	PCI Bus Lock
PAR	I/O	3.3 V (5-V Tolerance)	PCI Bus Parity
PCICLK[4:0]	O	3.3 V (5-V Tolerance)	33-MHz PCI clocks [4:0]
PCICLK5/GPIO41	O	3.3 V (5-V Tolerance)	33-MHz PCI clock 5 / LPC CLK 0

Pin Name	Type	Voltage	Functional Description
PCIRST#	O	3.3 V (5-V Tolerance)	Hardware Reset for PCI Slots Assertion: (a) at power on, (b) sometime after CPU_STP#'s assertion in S0, (c) after the system has transitioned into S4/S5. De-assertion: sometime after SB PWR_GOOD is asserted during power on or during a transition from S4/S5 to S0.
PERR#	I/O	3.3 V (5-V Tolerance)	Parity Error: reports data parity errors during all PCI transactions, except in a special cycle.
REQ#[2:0]	I	3.3 V (5-V Tolerance)	Request [2:0] Input: indicates that the agent desires use of the bus.
REQ3#/GPIO70	I	3.3 V (5-V Tolerance)	PCI Request 3 Input / GPIO 70
REQ4#/GPIO71	I	3.3 V (5-V Tolerance)	PCI Request 4 Input / GPIO 71
SERR#	I/OD	3.3 V (5-V Tolerance)	System Error: for reporting address parity errors and data parity errors on the special cycle command, or any other system error where the result will be catastrophic.
STOP#	I/O	3.3 V (5-V Tolerance)	Stop: indicates the current target is requesting the master to stop the current transaction
TRDY#	I/O	3.3 V (5-V Tolerance)	Target Ready Target Ready: indicates the target agent's ability to complete the current data phase of the transaction.

7.5 USB Interface

Pin Name	Type	Voltage	Functional Description
USB_HSD[11:0]P	I/O	AVDD_TX	USB 2.0 Port 11 ~ 0 Positive I/O (See **Note 1**)
USB_HSD[11:0]N	I/O	AVDD_TX	USB 2.0 Port 11 ~ 0 Negative I/O (See **Note 1**)
USB_FSD[13:12]P	I/O	S5_3.3V	USB 1.1 port 13:12 (full/low speed) Positive I/O (See **Note 2**)
USB_FSD[13:12]N	I/O	S5_3.3V	USB 1.1 port 13:12 (full/low speed) Negative I/O (See **Note 2**)
USBCLK/ 14M_25M_48M_OSC	I	S5_3.3V	48-MHz input clock used for USB
USB_RCOMP	I	AVDDC	Compensating resistors input
USB_OC[5:0[#/ GPM[5:0]#	I/O	S5_3.3V	USB Over Current [5:0] / GPM [5:0] USB_OC4# is also multiplexed as IR_RX0
USB_OC6#/IR_TX1/ GEVENT6#	I/O	S5_3.3V	USB Over Current 5 / General Event 6

Notes: (1) The USB_HSD[11:0]P and USB_HSD[11:0]N signals are used for connecting internal or external USB devices via USB Port connectors. These ports are handled by users and are subject directly to ESD events to either the connector, the device, or to the pins themselves. The USB_HSDP and USB_HSDN signals that may be exposed to the user through an USB port connection must have ESD protection.

(2) The USB_FSD[13:12]P and USB _FSD[13:12]N signals are used only for connecting to internal devices. They support only full or low, but not high speed devices.

7.6 PATA 66/100/133

Note: The SP5100 does not support the flash controller function. The flash controller should be disabled by BIOS, and the interface can only be used for IDE function (or as GPIOs, in case of the IDE data bus bits). Portions of the pin names below that imply flash controller function should be ignored. See the *SP5100 Schematic Review Checklist* for how to terminate these signals if they are not used.

Pin Name	Type	Voltage	Functional Description
IDE_IORDY/FC_FBCKIN	I	3.3 V (5-V Tolerance)	IDE IO Ready
IDE_IRQ/FC_INT2	I	3.3 V (5-V Tolerance)	IDE Interrupt Request/
IDE_A0/FC_OE#	O	3.3 V (5-V Tolerance)	IDE Address bus bit 0
IDE_A1/FC_FBCLKOUT	O	3.3 V (5-V Tolerance)	IDE Address bus bit 1
IDE_A2	O	3.3 V (5-V Tolerance)	IDE Address bus bit 2
IDE_DACK#/FC_AVD#	O	3.3 V (5-V Tolerance)	IDE DMA ACK
IDE_DRQ/FC_INT2	I	3.3 V (5-V Tolerance)	IDE DMA Request/
IDE_IOR#/FC_CLK	O	3.3 V (5-V Tolerance)	IDE IO Read/
IDE_IOW#/FC_WE#	O	3.3 V (5-V Tolerance)	IDE IO Write
IDE_CS1#/FC_CE#	O	3.3 V (5-V Tolerance)	IDE chip select for I/O 1xxh address
IDE_CS3#/FC_CE2#	O	3.3 V (5-V Tolerance)	IDE chip select for I/O 3xxh address
IDE_D[15:0]/FC_ADQ[15:0]/ GPIO[30:15]	I/O	3.3 V (5-V Tolerance)	IDE data bus bit [15:0] / GPIO [30:15]
IDE_RST#/FC_RST#/ IMC_GPO3	O	S5_3.3V (5-V Tolerance)	IDE reset/ IMC GPIO3

7.7 Serial ATA Interface

Pin Name	Type	Voltage	Functional Description
SATA_ACT#/GPIO67	OD	3.3 V	SATA Channel Active / GPIO 67
SATA_CAL	I	1.2 V (Filtered)	SATA Calibration
SATA_RX[5:0] -	I	1.2 V (Filtered)	SATA Channel[5:0] Receive Negative
SATA_RX[5:0] +	I	1.2 V (Filtered)	SATA Channel[5:0] Receive Positive
SATA_TX[5:0] -	O	1.2 V (Filtered)	SATA Channel[5:0] Transmit Negative
SATA_TX[5:0] +	O	1.2 V (Filtered)	SATA Channel[5:0] Transmit Positive
SATA_X1	I	3.3 V (Filtered)	SATA Crystal Input.
SATA_X2	O	3.3 V (Filtered)	SATA Crystal Output
SATA_IS0#/GPIO10	I/O	3.3 V	SATA Interlock Switch Port 0 (Input) / GPIO 10
SATA_IS1#/GPIO6	I/O	3.3 V	SATA Interlock Switch Port 1 (Input) / GPIO 6
SMARTVOLT1/ SATA_IS2#/GPIO4	I/O	3.3 V	Reduce system voltages / SATA Interlock Switch Port 2 (input) / GPIO 4
SATA_IS3#/CLK_REQ0#/ GPIO0	I/O	3.3 V	SATA Interlock Switch Port 3 (input) / PCI Express® clock request / GPIO0
SATA_IS4#/CLK_REQ1#/ FANOUT3/GPIO39	I/O	3.3 V	SATA Interlock Switch Port 4 (input) / PCI Express clock request/ Fan Output 3 / GPIO39

Pin Name	Type	Voltage	Functional Description
SATA_IS5#/CLK_REQ2#/ FANIN3/GPIO40	I/O	3.3 V	SATA Interlock Switch Port 5 (input) / PCI Express clock request/ Fan Tach In3 / GPIO40

Note: For each port there is a pin (SATA_IS) for sensing the status of the external interlock switch. If the motherboard implements SATA interlock switches, it should connect the statuses of the switches to those pins. The SP5100 will sense the statuses of those pins and can generate a PME or interrupt when the statuses change. Normally, an inter-lock switch is required for supporting hot plug.

7.8 HD Audio Interface

Pin Name	Type	Voltage	Functional description
AZ_BITCLK	O	3.3 V	HD Audio Interface Bit Clock
AZ_RST#	O	S5_3.3V	HD Audio interface Reset
AZ_SDIN[2:0]/GPIO[44:42]	I/O	S5_3.3V	HD Audio Serial Data Input from Codec [2:0] / GPIO [44:42]
AZ_SDIN3/GPIO46	I/O	S5_3.3V	HD Audio Serial Data Input from Codec 3/ GPIO 46
AZ_SDOUT	O	3.3 V	HD Audio Serial Data Output to Codec
AZ_SYNC	O	3.3 V	HD Audio Sync signal to Codec

7.9 Real Time Clock Interface

Pin Name	Type	Voltage	Functional Description
RTCCLK	I/O	S5_3.3V/VBAT	32-kHz output for internal RTC
VBAT	I	S5_3.3V/VBAT	RTC battery supply
X1	I	S5_3.3V/VBAT	RTC crystal oscillator input 1
X2	O	S5_3.3V/VBAT	RTC crystal oscillator input 2

7.10 Hardware Monitor

Note: Hardware monitor support is available for voltage sensors, fan control, and digital TSI to AM3 processors. However, temperature monitoring is NOT supported. See the *SP5100 Schematic Review Checklist* for how to terminate these signals if they are not used for either hardware monitor or GPIO function.

Pin Name	Type	Voltage	Functional Description
FANOUT0/GPIO3	I/O	3.3 V (5-V Tolerance)	Fan Output 0 / GPIO 3
FANOUT1/GPIO48	I/O	3.3 V (5-V Tolerance)	Fan Output 1 / GPIO 48
FANOUT2/GPIO49	I/O	3.3 V (5-V Tolerance)	Fan Output 2 / GPIO 49
FANIN0/GPIO50	I/O	3.3 V (5-V Tolerance)	Fan Tachometer Input 0 / GPIO 50
FANIN1/GPIO51	I/O	3.3 V (5-V Tolerance)	Fan Tachometer Input 1 / GPIO 51
FANIN2/GPIO52	I/O	3.3 V (5-V Tolerance)	Fan Tachometer Input 2 / GPIO 52
CLK_REQ1#/SATA_IS4/ FANOUT3/GPIO39	I/O	3.3 V	PCI Express® Clock Request / SATA Interlock Switch Port 4 (input) / Fan Output 3 / GPIO39
TEMP_COMM	I	Analog Ground	Temperature sensor diode current return path.
TEMPIN0*/GPIO61	I/O	3.3 V	Temperature Monitor Input 0* / GPIO 61
TEMPIN1*/GPIO62	I/O	3.3 V	Temperature Monitor Input 1* / GPIO 62
TEMPIN2*/GPIO63	I/O	3.3 V	Temperature Monitor Input 2* / GPIO 63

Pin Name	Type	Voltage	Functional Description
TEMPIN3*/TALERT#/ GPIO64	I/O	S5_3.3V	Temperature Monitor Input 3* / Temperature has reached cautionary state / GPIO 64
VIN0/GPIO53	I/O	3.3 V	Voltage Monitor Input 0 / GPIO 53
VIN1/GPIO54	I/O	3.3 V	Voltage Monitor Input 1 / GPIO 54
VIN2/GPIO55	I/O	3.3 V	Voltage Monitor Input 2 / GPIO 55
VIN3/GPIO56	I/O	3.3 V	Voltage Monitor Input 3 / GPIO 56
VIN4/GPIO57	I/O	3.3 V	Voltage Monitor Input 4 / GPIO 57
VIN5/GPIO58	I/O	3.3 V	Voltage Monitor Input 5 / GPIO 58
VIN6/GPIO59	I/O	3.3 V	Voltage Monitor Input 6 / GPIO 59
VIN7/GPIO60	I/O	3.3 V	Voltage Monitor Input 7 / GPIO 60
AVDD	-	3.3 V (Analog Power)	Hardware Monitor Analog PWR
AVSS	-	Analog Ground	Hardware Monitor Analog GND

*__Note:__ Temperature monitoring function is NOT supported on the SP5100. TEMPIN[3:0] can only be used as GPIOs.

7.11 SPI ROM Interface

SPI ROM is supported up to 33 MHz. Maximum ROM size supported is 16 MB. Burst read and fast read cycles are not supported.

Pin Name	Type	Voltage	Functional Description
SPI_DI/GPIO12	I/O	S5_3.3V	SPI Data In / GPIO 12
SPI_DO/GPIO11	I/O	S5_3.3V	SPI Data Output / GPIO 11
SPI_CLK/GPIO47	I/O	S5_3.3V	SPI Clock / GPIO 47
SPI_HOLD#/GPIO31	I/O	S5_3.3V	SPI HOLD# / GPIO 31
SPI_CS1#/GPIO32	I/O	S5_3.3V	SPI Chip Select# / GPIO 32
SPI_CS2#/IMC_GPIO2	I/O	S5_3.3V	Alternate SPI chip select#/IMC GPIO 2

7.12 Northbridge / Power Management Interface

Pin Name	Type	Voltage	Functional Description
LPC_PME#/ GEVENT3#	I/O	S5_3.3V	LPC PME# Input / General Event 3
LPC_SMI#/ EXTEVNT1#	I/O	3.3 V (5-V tolerance)	LPC SMI# Input / External Event 1
PCI_PME#/ GEVENT4#	I/O	S5_3.3V	PCI PME# Input / General Event 4
PWR_BTN#	I	S5_3.3V	Power Button: The Power Button will cause an SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state with only the PWRBTN# available as a wake event. Override will occur even if the system is in the S1 state. This signal has an internal pull-up resistor.

Pin Name	Type	Voltage	Functional Description
PWR_GOOD	I	S5_3.3V	SB power good input Assertion of PWR_GOOD by the SB power good circuit on the motherboard indicates that power supplies to the SB are valid. Assertion takes place sometime after NB Power Good is asserted. De-assertion of PWR_GOOD by the SB power good circuit indicates that the power supplies to the SB are NOT valid. De-assertion takes place sometime after SLP_S3# or SLP_S5#'s assertion, or after Power Supply Power Good is de-asserted.
RI#/EXTEVNT0#	I/O	S5_3.3V	Ring Indicator / External Event 0
SMARTVOLT2/ SHUTDOWN#/ GPIO5	I/O	S0	Set system rails to lower voltage / System Shutdown / GPIO5 System Shutdown: Assertion will cause the SP5100 to assert SLP_S3# and SLP_S5# to force system to transition to S5 immediately, without waiting for the STPGNT message from the processor.
SLP_S3#	O	S5_3.3V	S3 Sleep Power plane control Assertion of SLP_S3# shuts off power to non-critical components when system transitions to S3, S4, or S5 states. Assertion takes place sometime after CPU_STP# is asserted. De-assertion of SLP_S3# turns on power to non-critical components when system transitions from S3, S4, or S5 back to S0. De-assertion takes place sometime after a wake-up event has been triggered.
SLP_S5#	O	S5_3.3V	S5 Sleep Power plane control - Assertion of SLP_S5# shuts power off to non-critical components when system transitions to S4 or S5 state. Assertion takes place sometime after CPU_STP# is asserted. De-assertion of SLP_S5# turns on power to non-critical components when transitioning from S4/S5 back to S0 state. De-assertion takes place sometime after a wake-up event is triggered.
SMBALERT#/ THRMTRIP#/ GEVENT2#	I/O	S5_3.3V	SMBus Alert / Thermal Trip / General Event 2 Thermal Trip: Signal indicates to the SP5100 that a thermal trip has occurred. Its assertion will cause the SP5100 to transition the system to S5 immediately, without waiting for the STPGNT message from the processor.
SUS_STAT#	OD	S5_3.3V	Suspend Status - Assertion by the SP5100 indicates that the system will be entering a low-power state soon. The signal is monitored by those devices with memory that needs to switch from normal refresh to suspend refresh mode when the system transitions to a low-power state. Assertion takes place after the Stop Grant message from the CPU is received by the system. De-assertion by the SP5100 indicates that the system is exiting a low power state now and is returning to S0. De-assertion takes place after LDT_STP# is de-asserted.
TEMPIN3/ TALERT#/ GPIO64	I/O	S5_3.3V	Temperature Monitor Input 3/ Thermal Alert / GPIO 64 Thermal Alert: The signal is a thermal alert to the SP5100. SP5100 can be programmed to generate an SMI#, SCI, or IRQ13 through GPE, or generate an SMI# without GPE in response to the signal's assertion. See the *AMD SP5100 Register Reference Guide* for details.

Pin Name	Type	Voltage	Functional Description
S3_STATE/ GEVENT5#	I/O	S5_3.3V	S3 State: Assertion of S3_STATE by the SP5100 indicates to the power supply that the system has transitioned into S3 state. Asserted after the Sleep S3 command is completed. De-assertion indicates that the system is leaving S3 state. De-assertion takes place after SUS_STAT# is de-asserted.
WAKE#/ GEVENT8#	I/O	S5_3.3V	PCI Express® Wake /General Event 8 PCI Express Wake: On Power up this pin will function as WAKE# in legacy mode. Optionally, WAKE# in native mode can be enabled after power up, only by software. When the pin is asserted (active low) the Southbridge will generate the wake event. The Wake# function is supported in S5 through S0, with the following restriction: *Wake function in S5 state*—When transitioning from G3 to S5, the WAKE# function will not be enabled. However, after an initial transition from S5 to S0 and back to S5, the WAKE# function will be enabled. It will stay enabled for any subsequent transition from S0 to S5. Care must be taken when plugging in PCIe devices. The system should be transitioned into the G3 state (S5 power off) before a PCIe device is installed. Plugging in a PCIe device when the system is in S5 state may cause the system to wake up, because the WAKE# signal driven by the PCIe device may transition momentarily to the active state when the device is installed but has not been initialized to drive the signal in an inactive state.
SLP_S2/GPM9#	I/O	S5_3.3V	S2 Sleep control: Assertion of SLP_S2 shuts off clocks when system transitions to S2 state, and it takes place sometime after CPU_STP# is asserted. De-assertion of SLP_S2 turns on clocks when system transitions from S2 back to S0, and it takes place sometime after a wake-up event has been triggered.
ALLOW_LDTSTP	I/OD	0.8-V threshold, S5_3.3V domain	ALLOW_LDTSTP: It is an input from NB to allow assertion of LDT_STP#. When ALLOW_LDTSTP is de-asserted, SP5100 cannot assert LDT_STP#. ALLOW_LDTSTP can be used to implement stutter mode operation for the CPU. Starting with RS78x, NB will control the LDT_STP# during C state. In this configuration, SB can drive ALLOW_LDTSTP to inform NB when it can assert LDT_STP#.
NB_PWRGD	OD	3.3 V	Northbridge Power good

7.13 SMBus Interface / General Purpose Open Collector

Pin Name	Type	Voltage	Functional Description
SCL0/GPOC0#	I/OD	3.3 V (5-V Tolerance)	SMBus Clock 0 / General Purpose Open Collector 0 **Note:** Pin type is I/O when the pin is configured as GPIO.
SDA0/GPOC1#	I/OD	3.3 V (5-V Tolerance)	SMBus Data 0 / General Purpose Open Collector 1 **Note:** Pin type is I/O when the pin is configured as GPIO.
SCL1/GPOC2#	I/OD	S5_3.3V	SMBus Clock 1 / General Purpose Open Collector 2 **Note:** Pin type is I/O when the pin is configured as GPIO.
SDA1/GPOC3#	I/OD	S5_3.3V	SMBus Data 1 / General Purpose Open Collector 3 **Note:** Pin type is I/O when the pin is configured as GPIO.

SCL2/IMC_GPIO11	I/OD	S5_3.3V (5-V Tolerance)	SMBus Clock 2/IMC GPIO11 **Note:** Pin type is I/O when the pin is configured as GPIO.
SDA2/IMC_GPIO12	I/OD	S5_3.3V (5-V Tolerance)	SMBus Data 2/IMC GPIO12 **Note:** Pin type is I/O when the pin is configured as GPIO.
SCL3/IMC_GPIO13	I/OD	0.8-V threshold, S5_3.3V domain	SMBus Clock 3/IMC GPIO13 **Note:** Pin type is I/O when the pin is configured as GPIO.
SDA3/IMC_GPIO14	I/OD	0.8-V threshold, S5_3.3V domain	SMBus Data 3/IMC GPIO14 **Note:** Pin type is I/O when the pin is configured as GPIO.
SMBALERT#/ THRMTRIP#/ GEVENT2#	I/O	S5_3.3V	SMBus Alert# / Thermal Trip / General Event 2 SM Bus Alert: This signal is used to wake the system or generate an SMI#. If not used for SMBALERT#, it can be used for thermal trip or as a GEVENT.

Notes: (1) SDA1 and SCL1 SMBus interface is the secondary SMBUS in the S5 power domain, and should be connected to devices that reside in the S5 power domain.
(2) There are only two SMBus controllers. The SCL1/SDA1 pair is controlled by SMBus controller 1. SCL0/SDA0, SCL2/SDA2, and SCL3/SDA3 are multiplexed pins that are all controlled by SMBus controller 0, and only 1 pair of those pins can be active at any time.

7.14 External Event / General Event / General Power Management / General Purpose Open Collector

The EXTEVENT/GEVENT/GPM/GPOC pins of the SP5100 are multiplexed with other functions. For information on how to configure the EXTEVENT/GEVENT/GPM/ GPOC pins for the desired functions, see the *AMD SP5100 Register Reference Guide.*

The table below lists all the EXTEVENT/GEVENT/GPM/GPOC pins on the SP5100. The Default Type column shows the state of the pin (default function) after de-assertion of the PCI host bus reset (A_RST#), which happens after power up or after system reset. Signals that are in input state after reset will be tri-state (TS) if they do not have any internal PU (pull-up) or PD (pull-down). For pins that have PU or PD internally, their states after reset will depend on the PU or PD: for signals with PU, the state will be HIGH and for signals with PD the state will be LOW. The PU and PD shown are enabled by default after PCI Reset and can be disabled by System BIOS.

Abbreviations: PU = pull-up, PD = pull-down, OD = open drain, I/O = Input/Output, TS = tri-state

Ball Name (Default Function in Blue)	Type	Voltage and Domain	Internal Resistor (Default in Blue)	Default Type (Default State in Blue)	Functional Description
USB_OC0#/ **GPM0#**	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	USB Over Current 0/ GPM 0
USB_OC1#/ **GPM1#**	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	USB Over Current 1/ GPM 1
USB_OC2#/ **GPM2#**	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	USB Over Current 2/ GPM 2

Ball Name (Default Function in Blue)	Type	Voltage and Domain	Internal Resistor (Default in Blue)	Default Type (Default State in Blue)	Functional Description
USB_OC3#/ IR_RX1/ **GPM3#**	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	USB Over Current 3/ Infrared Receive 1/ GPM 3
USB_OC4#/ IR_RX0/ **GPM4#**	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	USB Over Current 4/ Infrared Receive 0/ GPM 4
USB_OC5#/ IR_TX0/ **GPM5#**	I/O/ OD	3.3V_S5	10-kΩ PU 10-kΩ PD	Input	USB Over Current 5/ Infrared Transmit 0/ GPM 5
BLINK/ **GPM6#**	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	LED Blink/ GPM 6
SYS_RESET#/ **GPM7#**	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	System Reset/ GPM 7
AZ_DOCK_RST/ **GPM8#**	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	HD Audio Dock Reset/ GPM 8
SLP_S2/ **GPM9#**	I/O	3.3V_S5	10-kΩ PU **10-kΩ PD**	Input	Sleep S2/ GPM 9
RI#/ **EXTEVENT0#**	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	Ring Indicator/ External Event 0
LPC_SMI#/ **EXTEVENT1#**	I/O	3.3V_S0 (5-V Tolerance)	**8.2-kΩ PU** 8.2-kΩ PD	Input	LPC System Management Interrupt / External Event 1
GA20IN/ **GEVENT0#**	I/O	3.3V_S0 (5-V Tolerance)	**8.2-kΩ PU** 8.2-kΩ PD	Input	A20 Gate Input/ General Event 0
KBRST#/ GEVENT1#	I/O	3.3V_S0 (5-V Tolerance)	**8.2-kΩ PU** 8.2-kΩ PD	Input	Keyboard Reset/ General Event 1
SMBALERT#/ **THRMTRIP#/** GEVENT2#	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	SM Bus Alert/ Thermal Trip/ General Event 2
LPC_PME#/ **GEVENT3#**	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	LPC Power Management Event / General Event 3
PCI_PME#/ **GEVENT4#**	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	PCI Power Management Event / General Event 4
S3_STATE/ **GEVENT5#**	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Output **Low**	S3 State/ General Event 5
USB_OC6#/ IR_TX1/ **GEVENT6#**	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	USB Over Current 6/ Infrared Transmit 1/ General Event 6
DDR3_RST#/ **GEVENT7#**	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	DDR3 Memory Reset/ General Event 7
WAKE#/ **GEVENT8#**	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	PCI Express® Wake/ General Event 8
SCL0/ **GPOC0#**	I/O	3.3V_S0 (5-V Tolerance)	8.2-kΩ PU 8.2-kΩ PD	Input	SMBus Clock 0/ GP Open Collector 0
SDA0/ **GPOC1#**	I/O	3.3V_S0 (5-V Tolerance)	8.2-kΩ PU 8.2-kΩ PD	Input	SMBus Data 0/ GP Open Collector 1
SCL1/ **GPOC2#**	I/O	3.3V_S5	10-kΩ PU 10-kΩ PD	Input	SMBus Clock 1/ GP Open Collector 2
SDA1/ **GPOC3#**	I/O	3.3V_S5	10-kΩ PU 10-kΩ PD	Input	SMBus Data 1/ GP Open Collector 3

7.15 General Purpose I/O

The GPIO pins of the SP5100 are multiplexed with other functions. For information on how to configure the GPIO pins for the desired functions, see the *AMD SP5100 Register Reference Guide.*

The table below lists all the GPIO pins on the SP5100. The Default Type column shows the state of the pin (default function) after de-assertion of the PCI host bus reset (A_RST#), which happens after power up or after system reset. Signals that are in input state after reset will be tri-state (TS) if they do not have any internal PU (pull up) or PD (Pull Down). For pins that have PU or PD internally, their states after reset will depend on the PU or PD: for signals with PU, the state will be HIGH and for signals with PD the state will be LOW. The PU and PD shown are enabled by default after PCI Reset and can be disabled by System BIOS.

Ball Name (Default Function in Blue)	Type	Voltage and Domain	Internal Resistor (Default in Blue)	Default Type (Default State in Blue)	Functional Description
CLK_REQ0#/ SATA_IS3#/ **GPIO0**	I/O	3.3V_S0 (5-V Tolerance)	10-kΩ PU **10-kΩ PD**	Input	Clock Request 0/ Serial ATA Interlock 3/ GPIO 0
SPKR/ **GPIO2**	I/O	3.3V_S0 (5-V Tolerance)	8.2-kΩ PU 8.2-kΩ PD	Input	Speaker/ GPIO 2
FANOUT0/ **GPIO3**	I/O	3.3V_S0 (5-V Tolerance)	**8.2-kΩ PU** 8.2-kΩ PD	Input	Fan Output 0/ GPIO 3
SMARTVOLT1/ SATA_IS2#/ **GPIO4**	I/O	3.3V_S0 (5-V Tolerance)	8.2-kΩ PU 8.2-kΩ PD	Input	Smartvolt Select 1/ Serial ATA Interlock 2/ GPIO 4
SMARTVOLT2/ SHUTDOWN#/ **GPIO5**	I/O	3.3V_S0 (5-V Tolerance)	8.2-kΩ PU 8.2-kΩ PD	Input	Smartvolt Select 2/ System Shutdown/ GPIO 5
CLK_REQ3#/ SATA_IS1#/ **GPIO6**	I/O	3.3V_S0 (5-V Tolerance)	8.2-kΩ PU 8.2-kΩ PD	Input **TS**	Clock Request 3/ Serial ATA Interlock 1/ GPIO 6
DDC1_SDA/ **GPIO8**	I/O	3.3V_S0 (5-V Tolerance)	8.2-kΩ PU 8.2-kΩ PD	Input	DDC1 Serial Data/ GPIO 8
DDC1_SCL/ **GPIO9**	I/O	3.3V_S0 (5-V Tolerance)	8.2-kΩ PU 8.2-kΩ PD	Input	DDC1 Serial Control/ GPIO 9
SATA_IS0#/ **GPIO10**	I/O	3.3V_S0 (5-V Tolerance)	8.2-kΩ PU 8.2-kΩ PD	Input	Serial ATA Interlock 0/ GPIO 10
SPI_DO/ GPIO11	I/O	3.3V_S5	10-kΩ PU **10-kΩ PD**	Input	SPI ROM Data Out/ GPIO 11
SPI_DI/ GPIO12	I/O	3.3V_S5	10-kΩ PU **10-kΩ PD**	Input	SPI ROM Data In/ GPIO 12
LAN_RST#/ GPIO13	I/O	3.3V_S0 (5-V Tolerance)	8.2-kΩ PU 8.2-kΩ PD	Output **Low**	LAN Reset/ GPIO 13
ROM_RST#/ GPIO14	I/O	3.3V_S5	10-kΩ PU 10-kΩ PD	Output **Low**	SPI ROM Reset/ GPIO 14
IDE_D[6:0]/ GPIO[21:15]	I/O	3.3V_S0 (5-V Tolerance)	**27-Ω series**	Output **High**	IDE data [6:0]/ GPIO [21:15]
IDE_D7/ GPIO22	I/O	3.3V_S0 (5-V Tolerance)	**27-Ω series** **10-kΩ PD**	Output **High**	IDE data 7/ GPIO 22

Ball Name (Default Function in Blue)	Type	Voltage and Domain	Internal Resistor (Default in Blue)	Default Type (Default State in Blue)	Functional Description
IDE_D[15:8]/ GPIO[30:23]	I/O	3.3V_S0 (5-V Tolerance)	**27-Ω series**	Output **High**	IDE data [15:8]/ GPIO [30:23]
SPI_HOLD#/ GPIO31	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	SPI ROM Hold/ GPIO 31
SPI_CS1#/ GPIO32	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	SPI ROM Chip Select 1/ GPIO 32
INTE#/ GPIO33	I/O	3.3V_S0 (5-V Tolerance)	**8.2-kΩ PU**	Input	PCI Interrupt E/ GPIO 33
INTF#/ GPIO34	I/O	3.3V_S0 (5-V Tolerance)	**8.2-kΩ PU**	Input	PCI Interrupt F/ GPIO 34
INTG#/ GPIO35	I/O	3.3V_S0 (5-V Tolerance)	**8.2-kΩ PU**	Input	PCI Interrupt G/ GPIO 35
INTH#/ GPIO36	I/O	3.3V_S0 (5-V Tolerance)	**8.2-kΩ PU**	Input	PCI Interrupt H/ GPIO 36
CLK_REQ1#/ SATA_IS4#/ FANOUT3/ **GPIO39**	I/O	3.3V_S0 (5-V Tolerance)	8.2-kΩ PU **8.2-kΩ PD**	Input	Clock Request 1/ Serial ATA Interlock 4/ Fan Output 3/ GPIO 39
CLK_REQ2#/ SATA_IS5#/ FANIN3/ **GPIO40**	I/O	3.3V_S0 (5-V Tolerance)	8.2-kΩ PU **8.2-kΩ PD**	Input	Clock Request 2/ Serial ATA Interlock 5/ Fan Input 3/ GPIO 40
PCICLK5/ **GPIO41** **Revision A11:** **PCICLK5**/ GPIO41	I/O	3.3V_S0 (5-V Tolerance)	8.2-kΩ PU 8.2-kΩ PD	Input **A11**: Output **Clock**	PCI Clock 5/ GPIO 41
AZ_SDIN0/ GPIO42	I/O	3.3V_S5	**50-kΩ PD**	Input	HD Audio Serial Data In 0/ GPIO 42
AZ_SDIN1/ GPIO43	I/O	3.3V_S5	**50-kΩ PD**	Input	HD Audio Serial Data In 1/ GPIO 43
AZ_SDIN2/ GPIO44	I/O	3.3V_S5	**50-kΩ PD**	Input	HD Audio Serial Data In 2/ GPIO 44
AZ_SDIN3/ GPIO46	I/O	3.3V_S5	**50-kΩ PD**	Input	HD Audio Serial Data In 3/ GPIO 46
SPI_CLK/ GPIO47	I/O	3.3V_S5	10-kΩ PU **10-kΩ PD**	Input	SPI ROM Clock/ GPIO 47
				Output **SPICLK**	SPI Clock if ROM select is SPI
FANOUT1/ **GPIO48**	I/O	3.3V_S0 (5V tolerance)	**8.2-kΩ PU** 8.2-kΩ PD	Input	Fan Output 1/ GPIO 48
FANOUT2/ **GPIO49**	I/O	3.3V_S0 (5V tolerance)	**8.2-kΩ PU** 8.2-kΩ PD	Input	Fan Output 2/ GPIO 49
FANIN0/ **GPIO50**	I/O	3.3V_S0 (5V tolerance)	10-kΩ PU 10-kΩ PD	Input	Fan Input 0/ GPIO 50
FANIN1/ **GPIO51**	I/O	3.3V_S0 (5V tolerance)	10-kΩ PU 10-kΩ PD	Input	Fan Input 1/ GPIO 51
FANIN2/ **GPIO52**	I/O	3.3V_S0 (5V tolerance)	10-kΩ PU 10-kΩ PD	Input	Fan Input 2/ GPIO 52

Ball Name (Default Function in Blue)	Type	Voltage and Domain	Internal Resistor (Default in Blue)	Default Type (Default State in Blue)	Functional Description
VIN0/ **GPIO53**	I/O	3.3V_S5	10-kΩ PU 10-kΩ PD	Input	Voltage Input 0/ GPIO 53
VIN1/ **GPIO54**	I/O	3.3V_S5	10-kΩ PU 10-kΩ PD	Input	Voltage Input 1/ GPIO 54
VIN2/ **GPIO55**	I/O	3.3V_S5	10-kΩ PU 10-kΩ PD	Input	Voltage Input 2/ GPIO 55
VIN3/ **GPIO56**	I/O	3.3V_S5	10-kΩ PU 10-kΩ PD	Input	Voltage Input 3/ GPIO 56
VIN4/ **GPIO57**	I/O	3.3V_S5	10-kΩ PU 10-kΩ PD	Input	Voltage Input 4/ GPIO 57
VIN5/ **GPIO58**	I/O	3.3V_S5	10-kΩ PU 10-kΩ PD	Input	Voltage Input 5/ GPIO 58
VIN6/ **GPIO59**	I/O	3.3V_S5	10-kΩ PU 10-kΩ PD	Input	Voltage Input 6/ GPIO 59
VIN7/ **GPIO60**	I/O	3.3V_S5	10-kΩ PU 10-kΩ PD	Input	Voltage Input 7/ GPIO 60
TEMPIN0/ **GPIO61**	I/O	3.3V_S5	10-kΩ PU 10-kΩ PD	Input	Temperature Input 0/ GPIO 61
TEMPIN1/ **GPIO62**	I/O	3.3V_S5	10-kΩ PU 10-kΩ PD	Input	Temperature Input 1/ GPIO 62
TEMPIN2/ **GPIO63**	I/O	3.3V_S5	10-kΩ PU 10-kΩ PD	Input	Temperature Input 2/ GPIO 63
TEMPIN3/ TALERT#/ **GPIO64**	I/O	3.3V_S5	10-kΩ PU 10-kΩ PD	Input	Temperature Input 3/ Temperature Alert/ GPIO64
BMREQ#/ REQ5#/ **GPIO65**	I/O	3.3V_S0 (5-V tolerance)	8.2-kΩ PU 8.2-kΩ PD	Input	Bus Master Request/ PCI Request 5/ GPIO 65
LLB#/ **GPIO66**	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	Low-Low Battery/ GPIO 66
SATA_ACT#/ GPIO67	OD	3.3V_S0	8.2-kΩ PU 8.2-kΩ PD	Output **TS**	Serial ATA Activity/ GPIO 67
LDRQ1#/ GNT5#/ GPIO68	I/O	3.3V_S0 (5-V Tolerance)	**15-kΩ PU**	Input	LPC DMA Req 1/ PCI Grant 5/ GPIO 68
REQ3#/ GPIO70	I/O	3.3V_S0 (5-V Tolerance)	**15-kΩ PU**	Input	PCI Request 3/ GPIO 70
REQ4#/ GPIO71	I/O	3.3V_S0 (5-V Tolerance)	**15-kΩ PU**	Input	PCI Request 4/ GPIO 71
GNT3#/ GPIO72	I/O	3.3V_S0 (5-V Tolerance)	8.2-kΩ PU 8.2-kΩ PD	Output **High**	PCI Grant 3/ GPIO 72
GNT4#/ GPIO73	I/O	3.3V_S0 (5-V Tolerance)	8.2-kΩ PU 8.2-kΩ PD	Output **High**	PCI Grant 4/ GPIO 73
IMC_GPIO[1:0]	I/O	3.3V_S5 (5-V tolerance)	**10-kΩ PU** 10-kΩ PD	Input	Integrated Microcontroller (IMC) GPIO [1:0]
SPI_CS2#/ **IMC_GPIO2**	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	SPI ROM Chip Select 2/ Integrated Microcontroller (IMC) GPIO 2

Ball Name (Default Function in Blue)	Type	Voltage and Domain	Internal Resistor (Default in Blue)	Default Type (Default State in Blue)	Functional Description
IDE_RST#/ F_RST#/ **IMC_GPO3**	OD	3.3V_S5 (5-V tolerance)	10-kΩ PU 10-kΩ PD	Output **Low**	IDE Reset/ Integrated Microcontroller (IMC) GPO 3
IMC_GPIO[7:4]	I/O	3.3V_S5 (5-V tolerance)	**10-kΩ PU** 10-kΩ PD	Input	Integrated Microcontroller (IMC) GPIO [7:4]
IMC_GPIO[9:8]	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	Integrated Microcontroller (IMC) GPIO [9:8]
IMC_PWM0 ◊ / **IMC_GPIO10**	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	Integrated Microcontroller (IMC) PWM 0/ IMC GPIO 10
SCL2 ◊ / **IMC_GPIO11**	I/O	3.3V_S5 (5-V tolerance)	10-kΩ PU 10-kΩ PD	Input	SMBus Clock 2/ Integrated Microcontroller (IMC) GPIO 11
SDA2 ◊ / **IMC_GPIO12**	I/O	3.3V_S5 (5-V tolerance)	10-kΩ PU 10-kΩ PD	Input	SMBus Data 2/ Integrated Microcontroller (IMC) GPIO 12
SCL3_LV ◊ / **IMC_GPIO13**	I/O	3.3V_S5	10-kΩ PU 10-kΩ PD	Input	Low Voltage SMBus Clock 3/ Integrated Microcontroller (IMC) GPIO 13
SDA3_LV ◊ / **IMC_GPIO14**	I/O	3.3V_S5	10-kΩ PU 10-kΩ PD	Input	Low Voltage SMBus Data 3 / Integrated Microcontroller (IMC) GPIO 14
IMC_PWM1 ◊ / **IMC_GPIO15**	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	Integrated Microcontroller (IMC) PWM 1/ IMC GPIO 15
IMC_PWM2 ◊ / **IMC_GPO16 §**	I/O	3.3V_S5 (5-V tolerance)	**10-kΩ PU** 10-kΩ PD	Input	Integrated Microcontroller (IMC) PWM 2/ IMC GPO 16
IMC_PWM3 ◊ / **IMC_GPO17 §**	I/O	3.3V_S5 (5-V tolerance)	**10-kΩ PU** 10-kΩ PD	Input	Integrated Microcontroller (IMC) PWM 3/ IMC GPO 17
IMC_GPIO[41:18]	I/O	3.3V_S5	**10-kΩ PU** 10-kΩ PD	Input	Integrated Microcontroller (IMC) GPIO [41:18]

Notes: For information on how to configure the GPIO pins, see the *AMD SP5100 Register Reference Guide*. Notice that the IMC GPIOs can also be used as general purpose GPIOs.

* The "default function" and the "default state" refer to function and state of the pin after deassertion of PCI host bus reset (A_RST#), i.e., right after system power up or reset.

◊ The IMC PWM and SMBus functions are not available if the IMC is disabled via the strap setting on AZ_RST#.

§ To avoid corrupting the ROM type strap settings, IMC_GPO[17:16] must not be driven from an external source until after RSMRST# had been de-asserted.

7.16 Integrated Micro-Controller (IMC)

Note: Integrated Micro-Controller (IMC) interface advanced features are **not** supported by the SP5100. However, the GPIOs on the IMC interface can be used like any other GPIO pins, with IMC enabled or

disabled. If not used, pins on this interface should be terminated in the manner described in the *AMD SP5100 Schematic Review Checklist.*

The SMBUS is independent of the IMC controller. It is usable even when the IMC is disabled. When the IMC is enabled, the SMBUS controller is shared between the host and the IMC. The IMC can control the SMBus and the IMC interfaces if they are not used by the host, and that is achieved through software.

Pin Name	Type	Voltage	Functional Description
IMC_GPIO[1:0]	I/O	S5_3.3V (5-V Tolerance)	IMC GPIO [1:0]
SPI_CS2#/IMC_GPIO2	I/O	S5_3.3V	2nd SPI Chip Select# / IMC GPIO 2
IDE_RST#/F_RST#/ IMC_GPO3	I/O	S5_3.3V (5-V Tolerance)	IDE Reset / IMC GPO 3
IMC_GPIO [7:4]	I/O	S5_3.3V (5-V Tolerance)	IMC GPIO [7:4]
IMC_GPIO [9:8]	I/O	S5_3.3V	IMC GPIO [9:8]
IMC_PWM0/IMC_GPIO10	I/O	S5_3.3V	IMC PWM 0 / IMC GPIO 10
SCL2/IMC_GPIO11	I/O	S5_3.3V (5-V Tolerance)	SMBus Clk 2 / IMC GPIO 11
SDA2/IMC_GPIO12	I/O	S5_3.3V (5-V Tolerance)	SMBus Data 2 / IMC GPIO 12
SCL3_LV/IMC_GPIO13	I/O	0.8-V threshold, S5_3.3V domain	IMC GPIO 13/ SMBus Clk 3 for CPU temp status
SDA3_LV/IMC_GPIO14	I/O	0.8-V threshold, S5_3.3V domain	IMC GPIO 14/ SMBus Data 3 for CPU temp status
IMC_PWM1/IMC_GPIO15	I/O	S5_3.3V	IMC PWM 1* / IMC GPIO 15
IMC_PWM2/IMC_GPO16	I/O	S5_3.3V (5-V Tolerance)	IMC PWM 2* / IMC GPIO 16
IMC_PWM3/IMC_GPO17	I/O	S5_3.3V (5-V Tolerance)	IMC PWM 3* / IMC GPIO 17
IMC_GPIO[41:18]	I/O	S5_3.3V	IMC GPIO [41:18]

***Note:** The IMC power management controller is NOT supported by the SP5100. The pins can only be used as GPIOs.

7.17 Reset / Clocks / ATE

Note: Clock generator function is NOT SUPPORTED by the SP5100.

Pin Name	Type	Voltage	Functional Description
A_RST#	O	S5_3.3V	PCI Host Bus Reset. Asserted during transition to S3/S4/S5 to reset all devices in the SP5100 or connected to it, except the ACPI logic in the SP5100
14M_X1	I	AVDDCK_1.2	Reserved. See *SP5100 Schematic Review Checklist* for how to connect.
14M_X2	O	AVDDCK_1.2	Reserved. See *SP5100 Schematic Review Checklist* for how to connect.
PCIE_RCLKP/ NB_LNK_CLKP	I/O	CKVDD_1.2	Positive phase 100-MHz reference clock (positive) for SP5100.

Pin Name	Type	Voltage	Functional Description
PCIE_RCLKN/ NB_LNK_CLKN	I/O	CKVDD_1.2	Negative phase 100-MHz reference clock (negative) for SP5100.
GPP_CLK[3:0]P	O	CKVDD_1.2	Reserved. See *SP5100 Schematic Review Checklist* for how to connect.
GPP_CLK[3:0]N	O	CKVDD_1.2	Reserved. See *SP5100 Schematic Review Checklist* for how to connect.
CLK_REQ0#/SATA_IS3#/ GPIO0	I	3.3 V	PCI Express® clock request 0
CLK_REQ1#/SATA_IS4#/ FANOUT3/GPIO39	I	3.3 V	PCI Express clock request 1
CLK_REQ2#/SATA_IS5#/ FANIN3/GPIO40	I	3.3 V	PCI Express clock request 2
CLK_REQ3#/SATA_IS1#/ GPIO6	I	3.3 V	PCI Express clock request 3
25M_48M_66M_OSC	O	S5_VDD33	14 MHz reference clock input
NB_DISP_CLKP	O	CKVDD_1.2	Reserved. See *SP5100 Schematic Review Checklist* for how to connect.
NB_DISP_CLKN	O	CKVDD_1.2	Reserved. See *SP5100 Schematic Review Checklist* for how to connect.
CPU_HT_CLKP	O	CKVDD_1.2	Reserved. See *SP5100 Schematic Review Checklist* for how to connect.
CPU_HT_CLKN	O	CKVDD_1.2	Reserved. See *SP5100 Schematic Review Checklist* for how to connect.
NB_HT_CLKP	O	CKVDD_1.2	Reserved. See *SP5100 Schematic Review Checklist* for how to connect.
NB_HT_CLKN	O	CKVDD_1.2	Reserved. See *SP5100 Schematic Review Checklist* for how to connect.
SLT_GFX_CLKP	O	CKVDD_1.2	Reserved. See *SP5100 Schematic Review Checklist* for how to connect.
SLT_GFX_CLKN	O	CKVDD_1.2	Reserved. See *SP5100 Schematic Review Checklist* for how to connect.
USBCLK/ 14M_25M_48M_OSC	I/O	S5_3.3V	48-MHz input clock used for USB
RSMRST#	I	S5_3.3V	Resume Reset from Motherboard – Assertion of RSMRST# resets all SP5100 registers to their default values. It also causes all reset signals originating from the SP5100 (A_RST#, PCIRST#, LDT_RST#, AZ_RST#, AC_RST#) to be issued. RSRMT# should be asserted when system power is being applied. Type-I straps are captured on the rising edge of RSRMT# during its de-assertion. RSMRST# should be de-asserted sometime after S5 power is up, and should stay de-asserted until system power is removed.
SYS_RESET#/GPM7#	I/O	S5_3.3V	System Reset / GPM 7 System Reset: Signal coming from the power button circuit signaling a reset for the system. On receiving the signal, the SP5100 asserts all reset signals that originate from the SP5100 including: A_RST#, PCIRST#, LDT_RST#, AZ_RST#, and AC_RST#; it also resets all SP5100 registers to their default values.
LAN_RST#/GPIO13	I/O	3.3 V	Early version of A_RST#; meant for resetting LAN MAC. This signal is early to allow LAN to load its LON first
ROM_RST#/GPIO14	I/O	S5_3.3V	Early version of A_RST#, meant for resetting the system BIOS flash

Pin Name	Type	Voltage	Functional Description
TEST0	I	S5_3.3V	ATE Test 0
TEST1	I	S5_3.3V	ATE Test 1
TEST2	I	S5_3.3V	ATE Test 2

7.18 Intruder Alert

Pin Name	Type	Voltage	Functional Description
Intruder_Alert#	I	VBAT	Intruder alert sense input

7.19 Power and Ground

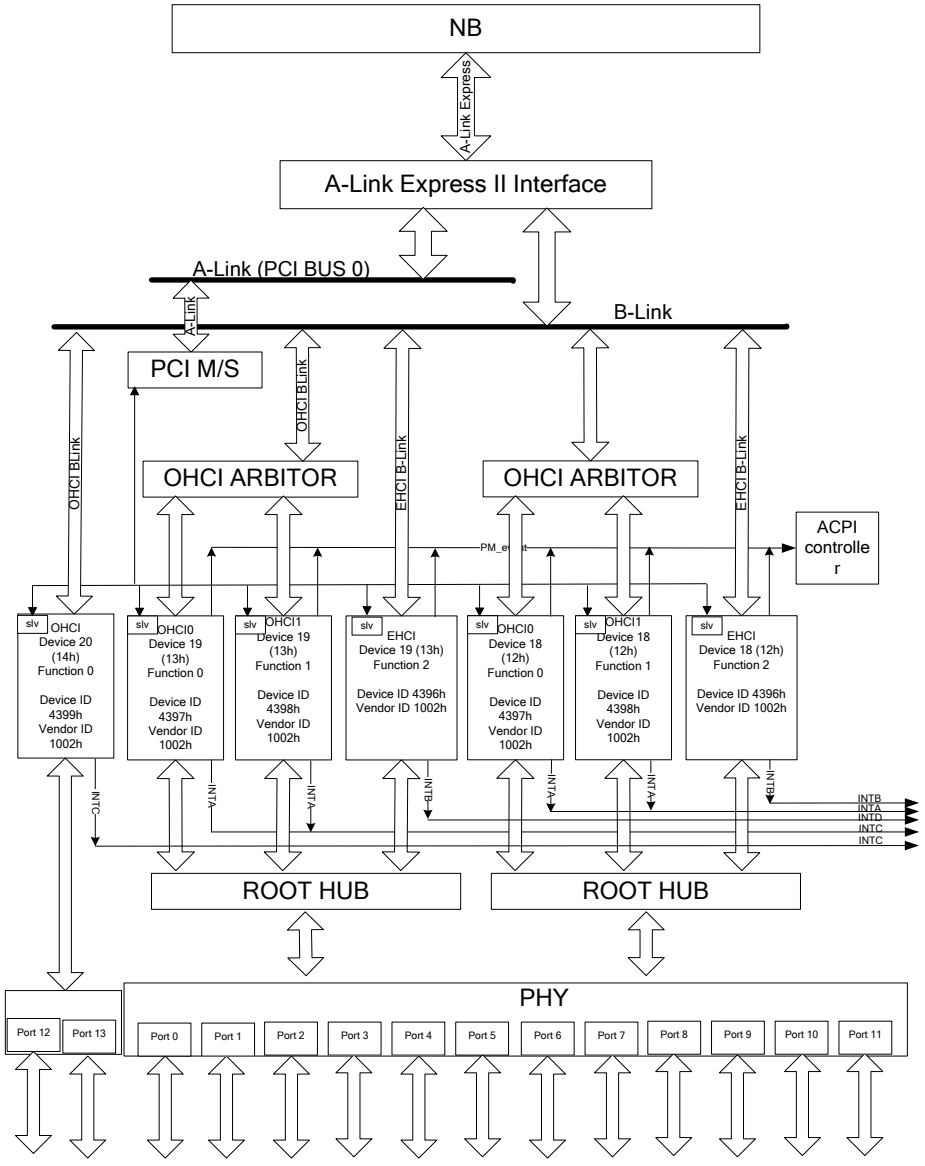
Signal Name	Voltage/ Ground	ACPI STATE	GND reference	Note	Description
VDD_[9:1]	1.2 V	S0-S2	VSS	-	Core power
VDDQ_[12:1]	3.3 V	S0-S2	VSS	-	3.3-V I/O Power
VDD33_18_[4:1]	3.3V	S0-S2	VSS	-	3.3 V power for PATA interface
S5_1.2V_[2:1]	1.2 V	S0-S5	VSS		1.2-V S5 Power
S5_3.3V_[7:1]	S5_3.3V	S0-S5	VSS	-	3.3-V S5 Power
AVDDCK_3.3V	3.3 V	S0-S2	AVSSCK	1	3.3-V power for analog PLLs
AVDDCK_1.2V	1.2 V	S0-S2	AVSSCK		1.2-V power for analog PLLs
CKVDD_1.2_[4:1]	1.2 V	S0-S2	PCIE_CK_VSS		1.2-V power for PCI Express® and clock buffers
PCIE_PVDD	1.2 V	S0-S2	PCIE_VSS	1	A-Link Express II PLL Power
PCIE_VDDR[7:1]	1.2 V	S0-S2	PCIE_VSS	1	A-Link Express II Analog power
AVDD_SATA[7:1]	1.2 V	S0-S2	AVSS_SATA	1	SATA Analog Power
PLLVDD_SATA_1	1.2 V	S0-S2	AVSS_SATA	1	SATA PLL Power
XTLVDD_SATA	3.3 V	S0-S2	AVSS_SATA	1	SATA XTAL Power
VBAT	2.5 - 3.6 V BAT	-	RTC_GND	-	RTC backup power
AVDD	S5_3.3V	S0-S5 / S0-S3	AVSS	1, 2	Analog Power for Hardware Monitor
AVDDC	S5_3.3V	S0-S5 / S0-S3	AVSSC	1, 2	Analog Power for USB PHY PLL
AVDDRX_[5:0]	S5_3.3V	S0-S5 / S0-S3	AVSS_USB	1, 2	Analog Power for USB PHY RX
AVDDTX_[5:0]	S5_3.3V	S0-S5 / S0-S3	AVSS_USB	1, 2	Analog Power for USB PHY TX
USB_PHY_1.2V[2:1]	1.2 V	S0-S5 / S0-S3	AVSS_USB	2	1.2-V USB PHY standby Power
V5_VREF	5 V	S0-S2	VSS	-	5-V Reference voltage for PCI interface
VSS_[50:1]	GND	-	-	-	Digital Ground
AVSSCK	GND	-	-	-	Common Ground for Analog PLLs
PCIE_PVSS	GND	-	-	-	A-Link Express II PLL Ground
PCIE_CK_VSS_[21:1]	GND	-	-	-	A-Link Express II Analog Ground

Signal Name	Voltage/ Ground	ACPI STATE	GND reference	Note	Description
AVSS_SATA[20:1]	GND	-	-	-	SATA Analog Ground (Plane)
AVSS	GND	-	-	-	Analog Ground for Hardware Monitor.
AVSSC	GND	-	-	-	Analog Ground for USB PHY PLL.
AVSS_USB_[24:1]	GND_USB	-	-	-	Analog Ground for USB PHY

Note 1: These power rails should be filtered.
Note 2: These power rails can be tied to S0-S5 or S0-S3 power.

8 Functional Description

8.1 EHCI USB 2.0 and OHCI USB 1.1 Controllers



Controller	Controls Port
OHCI (dev-20)	Port 12/13

Controller	Controls Port
OHCI0 (dev-18)	Port 0/1/2
OHCI1 (dev-18)	Port 3/4/5
EHCI (dev-18)	Port 0-5
OHCI0 (dev-19)	Port 6/7/8
OHCI1 (dev-19)	Port 9/10/11
EHCI (dev-19)	Port 6 - 11

Figure 8-1: SP5100 USB 2.0 System Block Diagram

8.1.1 USB Power Management

An advanced power management capability interface compliant with *PCI Bus Power Management Interface Specification Revision 1.1* is incorporated into the EHCI. This interface allows the EHCI to be placed in various power management states, offering a variety of power savings for a host system.

Table 8-1 highlights the EHCI support for power management states and features supported for each of the power management states. An EHCI implementation may internally gate-off USB clocks and suspend the USB transceivers (low power consumption mode) to provide these power savings.

Table 8-1: EHCI Support for Power Management States

PCI Power Management State	State Required/ Optional by Spec	Comments
D0	Required	**Supported in SP5100.** Fully awake backward compatible state. All logic in full power mode.
D1	Optional	**Not supported in SP5100.** USB Sleep state with EHCI bus master capabilities disabled. All USB ports in suspended state. All logic in low latency power saving mode because of low latency returning to D0 state.
D2	Optional	**Not supported in SP5100.** USB Sleep state with EHCI bus master capabilities disabled. All USB ports in suspended state.
D3hot	Required	**Supported in SP5100.** Deep USB Sleep state with EHCI bus master capabilities disabled. All USB ports in suspended state.
D3cold	Required	**Supported in SP5100.** Fully asleep backward compatible state. All downstream devices are either suspended or disconnected based on the implementation's capability to supply downstream port power within the power budget.

The functional and wake-up characteristics for the EHCI power states are summarized in Table 8-2 below.

Table 8-2: EHCI Power State Summary

Power State	Functional Characteristics	Wake-up Characteristics (Associated Enables must be Set)
D0	• Fully functional EHCI device state • Unmasked interrupts are fully functional	• Resume detected on suspended port • Connect or Disconnect detected on port Over Current detected on port
D1	• EHCI shall preserve PCI configuration • EHCI shall preserve USB configuration • Hardware masks functional interrupts • All ports are disabled or suspended	• Resume detected on suspended port • Connect or Disconnect detected on port • Over Current detected on port
D2	• EHCI shall preserve PCI configuration • EHCI shall preserve USB configuration • Hardware masks functional interrupts • All ports are disabled or suspended	• Resume detected on suspended port • Connect or Disconnect detected on port • Over Current detected on port

Power State	Functional Characteristics	Wake-up Characteristics (Associated Enables must be Set)
D3hot	• EHCI shall preserve PCI configuration • EHCI shall preserve USB configuration • Hardware masks functional interrupts • All ports are disabled or suspended	• Resume detected on suspended port • Connect or Disconnect detected on port • Over Current detected on port
D3cold	• PME Context in PCI Configuration space is preserved • Wake Context in EHCI Memory • Space is preserved • All ports are disabled or suspended	• Resume detected on suspended port • Connect or Disconnect detected on port • Over Current detected on port

8.2 SMI#/SCI Generation

Certain system events are routable between SMI# and SCI. When an event is routed to SMI#, an SMI# assertion message will be sent by the SP5100 to the processor and it will enter SMM space. The SMI status remains active until the EOS bit is set. When the EOS is set, SMI# de-assertion message will be sent to the processor for at least 4 PCICLK cycles. If the event is routed to SCI, then BIOS can route it to any of the legacy interrupts (except IRQ8) or INT21 in the case of IOAPIC.

Table 8-3: Causes of SMI# and SCI

Cause	SCI	SMI	Additional Enable	Where reported
SMI Command port	Yes	Yes	PM x0E, bit 2	PM x0F, bit 2
SERR# port	Yes	Yes	PCI config x64, bit 16	PCI config x04, bit 30; PM x0F, bit 1
GBLRLS written to	Yes	Yes	PM x0E, bit 0	PM x0F ,bit 0
PM Timer1	Yes	Yes	PM x00, bit 1; PM x08, x09, x0A	PM x01, bit 1
PM x00, bit 4 is written 1	Yes	Yes	PM x00, bit 4	PM x01, bit 4
IRQ[15:8] activity	Yes	Yes	PM x02	PM x05
IRQ[7:0] activity	Yes	Yes	PM x03	PM x06
Legacy IO activity	Yes	Yes	PM x04	PM x07
IO activity	Yes	Yes	PM x1C, PM xA8	PM x1D, PM xA9
Temperature Warning	Yes	Yes	XC50/C51, index x03, bit 1	XC50/C51, index x02, bit 1
Temperature Warning (this input can generate SMI# through this set of register)	Yes	Yes	AcpiGpe0Blk, index 00, bit 9	AcpiGpe0Blk, index 04, bit 9
GEVENT/GPM inputs	Yes	Yes	AcpiGpe0Blk, index 00, bits [7:0] for GEVENT, bits [29, 28, 26, 25, 22:19] for GPM	AcpiGpe0Blk, index 04, same bits
USB SMI#	Yes	Yes	AcpiGpe0Blk, index 00, bit 8	AcpiGpe0Blk, index 04, bit 8; PM x0F, bit 5
SMBus SMI#	Yes	Yes	AcpiGpe0Blk, index 00, bit 8	AcpiGpe0Blk, index 04, bit 8; PM x0F, bit 4
HDAudio wake	Yes	Yes	AcpiGpe0Blk, index 00, bit 27	–
USB wake	Yes	Yes	AcpiGpe0Blk, index 00, bit 11	AcpiGpe0Blk, index 04, bit 11
RTC	Yes	Yes	RTC_STS	RTC_EN
ACPI timer	Yes	Yes	TMR_STS	TMR_EN
GBL_STS	Yes	Yes	GBL_STS	GBL_EN
PowerButton	Yes	Yes	PWRBTN_STS	PWRBTN_EN

8.3 LPC ISA Bridge

8.3.1 LPC Interface Overview

The Low Pin Count (LPC) bus interface is a cost-efficient, low-speed interface designed to support low-speed legacy (ISA, X-bus) devices. The LPC interface essentially eliminates the need of ISA and X-bus in the system. A typical setup of the system with LPC interface is shown in Figure 8-2 below. Here the ISA bus is internal to SP5100 and is used for connecting to the legacy DMA logic. The LPC controller connects to the A-Link bus on one side and the LPC and SPI bus on the other side.

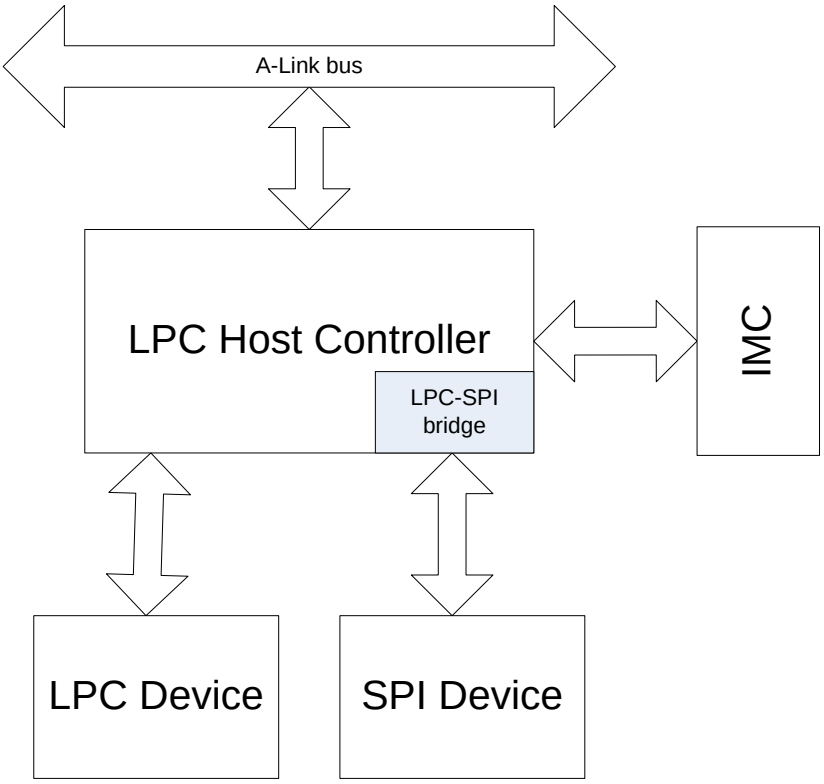


Figure 8-2: A Typical LPC Bus System

Examples of LPC devices include Super I/O (floppy-disk controller, keyboard controller), BIOS, audio, TPM, and system management controller. BIOS ROM can also be populated on the SPI interface. SP5100 can support FWH, LPC, or SPI type BIOS ROM. The ROM selection is determined by two strap pins during RSMRST# assertion. In addition to the straps, software can change the ROM selection through programming in the PMIO registers. SP5100 SPI interface is designed to allow ROM sharing with an external device such as an Ethernet MAC to save BOM cost. (**Note:** Device that shares the ROM must follow AMD SPI ROM sharing specification).

Note that the ISA interface is only used for legacy DMA operation. LPC host controller has the A-Link interface on one side and LPC interface on the other. Some LPC signals are optional. A more detailed description of each signal is given in *section 7.2*.

The host controller supports memory and IO read/write, DMA read/write, and bus master memory/IO

read/write. It supports up to two bus masters and 7 DMA channels. A bus master or DMA agent uses LDRQ pin to assert bus master or DMA request. The host controller uses LFRAME# to indicate the start or termination of a cycle. The following table shows a list of cycles supported by the host controller, initiator, data flow direction, and their PCI counterparts.

Table 8-4: LPC Cycle List and Data Direction

Cycle	Size (bytes)	Initiator	Data Direction	PCI counterpart
Memory read	1	Host	P-2-Host	MemRead to LPC range
Memory write	1	Host	Host-2-P	MemWrit to LPC range
I/O read	1	Host	P-2-Host	IORead to LPC range
I/O write	1	Host	Host-2-P	IOWrit to LPC range
DMA read	1,2,4	Peripheral	Host-2-P	DMA Cntrl Setup; DMA data fetch
DMA write	1,2,4	Peripheral	P-2-Host	DMA Cntrl Setup; DMA data store
BM Memory read	1,2,4	Peripheral	Host-2-P	DMA Cntrl Setup; DMA data fetch
BM Memory write	1,2,4	Peripheral	P-2-Host	DMA Cntrl Setup; DMA data store
BM I/O read	1,2,4	Peripheral	Host-2-P	DMA Cntrl Setup; IO data fetch
BM I/O write	1,2,4	Peripheral	P-2-Host	DMA Cntrl Setup; IO data store

The host controller has a SERIRQ (Serial IRQ) pin, which is used by peripherals that require interrupt support. All legacy interrupts are serialized on this pin, and then decoded by the host controller and sent to the interrupt controller for processing. Please refer to the Serial IRQ Specification (Rev 5.4) for detailed description on serial IRQ protocol.

8.3.2 LPC Module Block Diagram

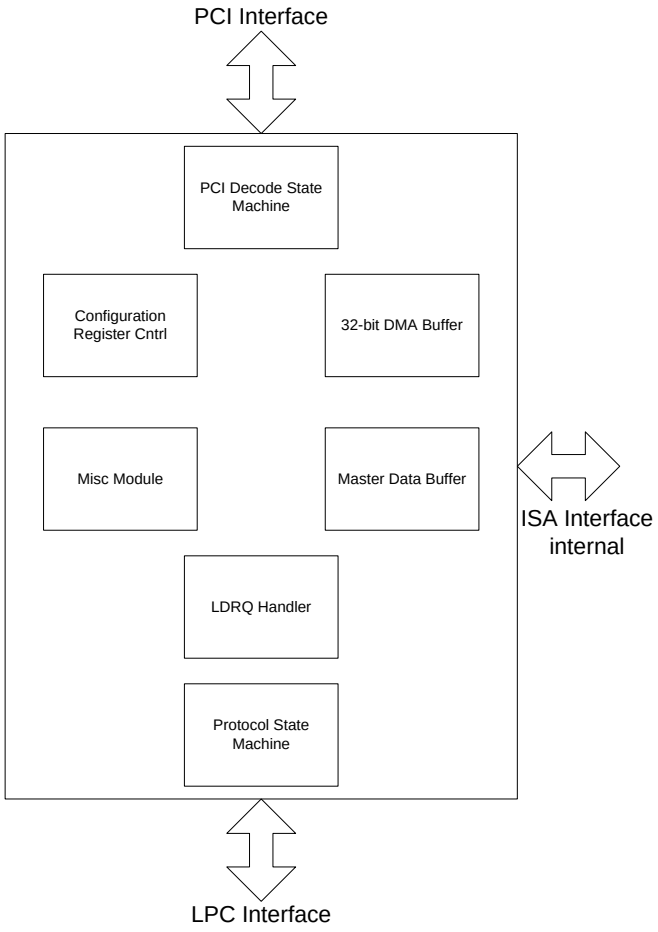


Figure 8-3: Block Diagram of LPC Module

8.4 Integrated Micro-Controller (IMC)

Note: Whether the IMC interface is enabled or not, the IMC GPIO pins can be used as general purpose GPIOs without IMC support. If not used, pins on this interface should be terminated in the manner described in the *SP5100 Schematic Review Checklist*.

8.5 Real Time Clock

The Real Time Clock (RTC) is used for updating a computer's time. In addition to that, it also generates interrupts for periodic events and pre-set alarm. The SP5100's RTC includes a 256-byte CMOS RAM, which is used to store the configuration of a computer, such as the number and type of floppy drive, graphics adapter, base memory, checksum value, etc. The RTC supports leap year date adjustment in hardware.

8.5.1 Functional Blocks of RTC

The internal RTC is made of two parts: one is an analog circuit, powered by a battery VBAT, and the other part is a digital circuit, powered by a main power VDD. *Figure 9-4* shows the block diagram of the internal RTC.

When writing data (time, alarm or date) to the RTC directly (by passing them through BIOS routine or operating system API calls), the application should verify that the data is in BCD format; binary mode is not supported. The data should be valid date/time, as the validation of the data can only be performed at the software level.

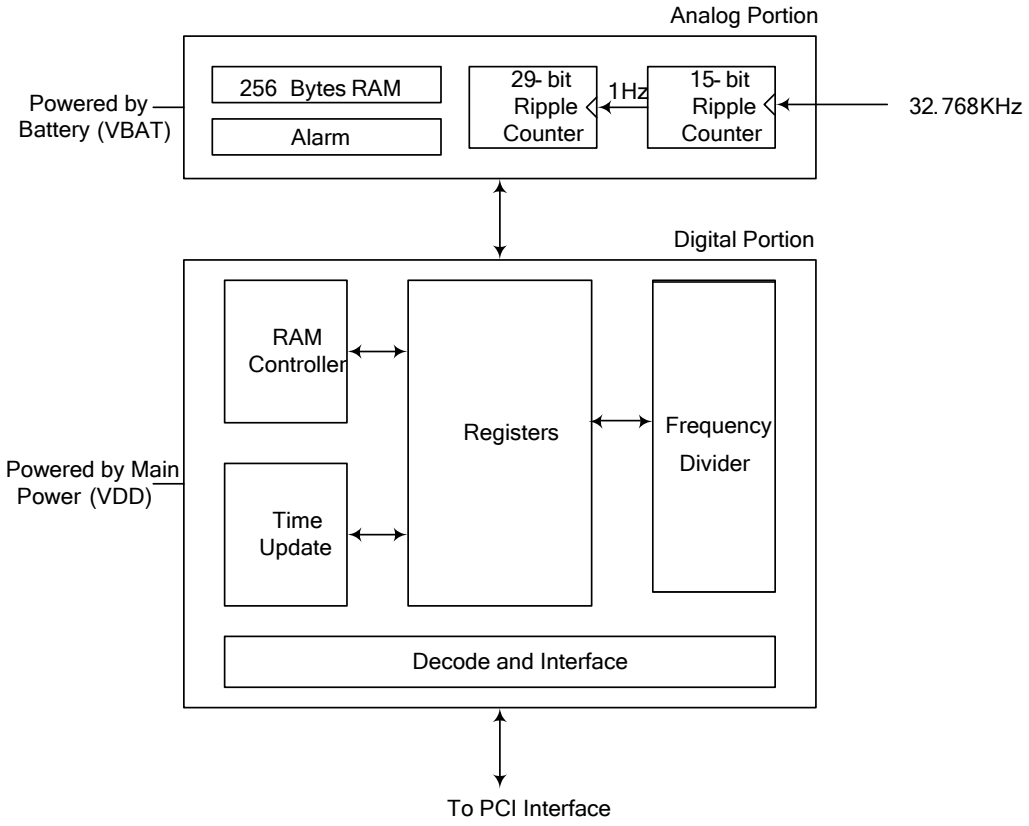


Figure 8-4: Block Diagram of Internal RTC

8.6 PATA Controller

The integrated parallel ATA controller contains a single channel but can be configured as primary or secondary channel. It can be configured to operate in legacy or native IDE mode.

8.7 SATA (Serial ATA) Controller

The integrated Serial ATA controller processes host commands and transfers data between the host and Serial ATA devices. It supports six independent Serial ATA channels. Each channel has its own Serial

ATA bus and supports one Serial ATA device. On transfer rate, SATA controller supports both Serial ATA Generation I (1.5 Gb/s) and Generation II (3.0 Gb/s). *Figure 9-5* below is a diagram for the SATA block.

The SP5100 SATA controller can operate in three modes:

1) All six channels can be configured as IDE mode. In this configuration, the programming interface of two of the channels (4 and 5) is under the PATA controller

2) Four channels configured as SATA AHCI and channel 4 and 5 configured in IDE mode. In this configuration, the programming interface of channel 4 and 5 are under the PATA controller

3) All six channels are configured as SATA AHCI mode.

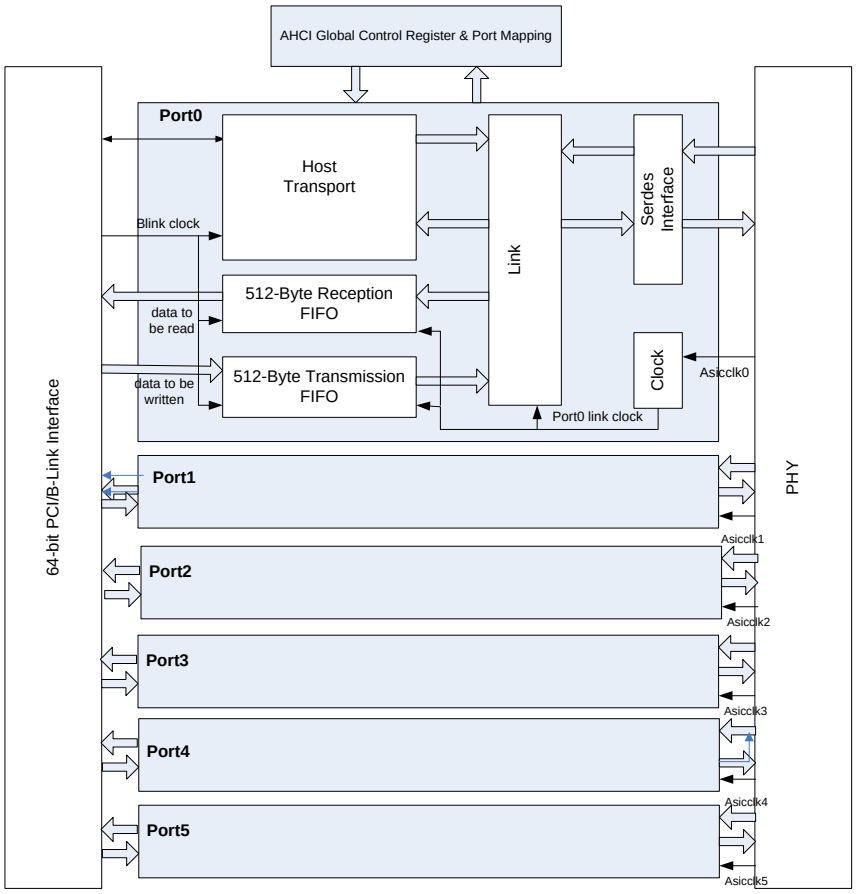


Figure 8-5: Block Diagram for the SATA Module

8.8 PCI Bridge

SP5100 PCI Bridge supports 5 PCI slots by default but can be optionally configured to support a 6th slot. The PCI bridge runs at 33 MHz and can support CLKRUN# function with individual clock override (option not to stop specific PCICLK). In addition, it has the capability to hide individual PCI device.

SP5100 has a strapping option for loading the boot codes from the PCI bus on the very first boot (1st boot after RSMRST#). Subsequent boots will revert back to the ROM selection determined by the ROM straps or PMIO programming. This is to allow system manufacturers to populate the motherboard with a blank flash device (for BIOS) and use this option to program it. This is particularly useful for systems built without a socket for the BIOS ROM.

8.9 High Definition Audio

Intel® High Definition (HD) Audio is the next-generation PC audio technology intended for replacing the AC '97. The primary goal for developing HD Audio is to create a uniform programming interface and to provide capabilities beyond those supported by the AC '97. It is not intended to be backward compatible with the AC '97. The link protocols and operations of these two standards are not compatible, which means AC '97 and HD Audio codecs cannot be mixed on the same link.

8.9.1 HD Audio Codec Connections

Figure 8-6 below shows the HD Audio interface connections to the HD Audio codecs. SP5100 can support up to 4 HD Audio codecs. Each codec will have its own AZ_SDIN (data input) for the HD Audio interface. Figure 8-6 shows the connection of a 2 codec configuration.

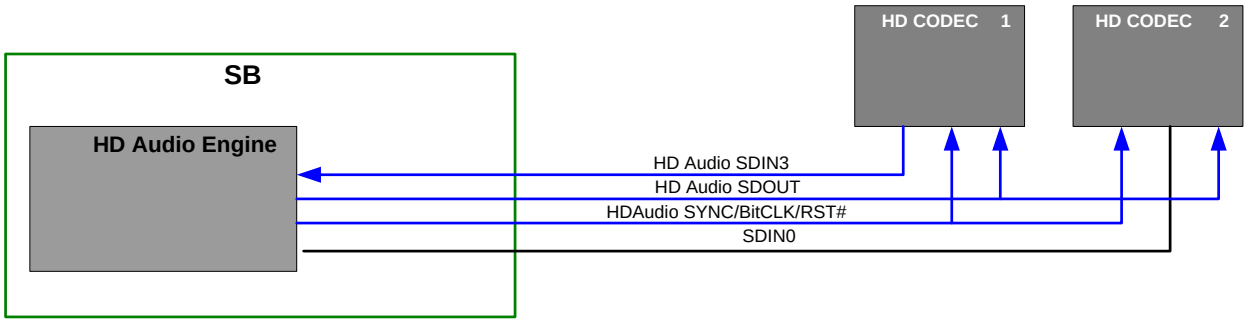


Figure 8-6: HD Audio Codec Connections

8.10 Power management/ACPI

The SP5100 power management/ACPI logic supports C3/C1e and stutter mode and S states for F series and prior versions of CPUs. With the newer CPUs and RS78x series NB, C and P states are controlled by the CPU and NB. Under this configuration, SP5100 becomes a client and uses ALLOW_LDTSTP as a handshake with NB to help NB to manage the C and P states accordingly.

8.11 General Events and GPIOs

Table 8-5 below lists the SMI, SCI, and Wake Events supported by SP5100's GPIO and GEVENT pins.

Table 8-5: SMI, SCI, and Wake Event Support by GPIO and General Event Pins

Pin Name	SMI Event	SCI Event	Wake Event
GPIO2	X	X	X
GPM [0:9]	X	X	X
GEVENTS [2:8]	X	X	X
EXTERNAL EVENTS [0:1]	X	X	X

Table 8-6 shows the state of the GPIO and GEVENT pins in different ACPI states. Note that even if some GPIOs are in the S5 domain, its functionality may not be maintained in the S5 state.

Table 8-6: Functionality of the General Events and GPIOs across ACPI States

GPIO / GEVENT	GPIO and G-Events Functionality across ACPI states			
	S0/S1	S2/S3	S4/S5	G3
EXTEVENT0#, EXTEVENT1# GEVENT# [7:2]	Maintain state			Undefined
GPM [9:0]	Maintain state			Undefined
IMC_GPIO§	Maintain state			Undefined
GPOC [1:0]	Maintain state	Undefined		
GPOC [3:2]	Maintain state			Undefined
GPIO [0:10,13,15;30,33:45,48:52,65]	Maintain state	Undefined		
GPIO[[11, 12 14, 31, 32, 46, 47, 53:64, 66]	Maintain state	Undefined		

Notes:
***** All GPIO and GPM pins are software configurable to assume alternate functions. Please refer to the GPIO section in the *AMD SP5100 Register Reference Guide* for information on how to configure the GPIO pins to alternate functions.

§ If IMC is disabled, the IMC GPIOs maintain state in S4 and S5 only if the register field PMIO_BB[5] is set to 1. See the *AMD SP5100 Register Reference Guide* for a more detailed description of the register.

8.12 Hardware Monitor Interface

The hardware monitor interface supports voltage sensors, fan control, and digital TSI to AM3 processors.

Pin Name	Type	Voltage	Functional Description
Fan control Outputs			
FANOUT0/GPIO3	I/O	3.3V (5V Tolerance)	Fan Output 0 / GPIO 3
FANOUT1/GPIO48	I/O	3.3V (5V Tolerance)	Fan Output 1 / GPIO 48
FANOUT2/GPIO49	I/O	3.3V (5V Tolerance)	Fan Output 2 / GPIO 49
FANIN0/GPIO50	I/O	3.3V (5V Tolerance)	Fan Tachometer Input 0 / GPIO 50
FANIN1/GPIO51	I/O	3.3V(5V Tolerance)	Fan Tachometer Input 1 / GPIO 51

Pin Name	Type	Voltage	Functional Description
FANIN2/GPIO52	I/O	3.3V(5V Tolerance)	Fan Tachometer Input 2 / GPIO 52
CLK_REQ1#/SATA_IS4/ FANOUT3/GPIO39	I/O	3.3V	PCI Express® Clock Request / SATA Interlock Switch Port 4 (input) / Fan Output 3 / GPIO39
Voltage Sensor inputs			
VIN0/GPIO53	I/O	3.3V	Voltage Monitor Input 0 / GPIO 53
VIN1/GPIO54	I/O	3.3V	Voltage Monitor Input 1 / GPIO 54
VIN2/GPIO55	I/O	3.3V	Voltage Monitor Input 2 / GPIO 55
VIN3/GPIO56	I/O	3.3V	Voltage Monitor Input 3 / GPIO 56
VIN4/GPIO57	I/O	3.3V	Voltage Monitor Input 4 / GPIO 57
VIN5/GPIO58	I/O	3.3V	Voltage Monitor Input 5 / GPIO 58
VIN6/GPIO59	I/O	3.3V	Voltage Monitor Input 6 / GPIO 59
VIN7/GPIO60	I/O	3.3V	Voltage Monitor Input 7 / GPIO 60
TSI input (Shared with SMBUS Clock 3 / Data 3 inputs)			
SCL3/IMC_GPIO13	I/O	0.8-V threshold, S5_3.3V domain	SMBus Clock 3/IMC GPIO13
SDA3/IMC_GPIO14	I/O	0.8-V threshold, S5_3.3V domain	SMBus Data 3/IMC GPIO14
Analog Power			
AVDD	-	3.3V (Analog Power)	Hardware Monitor Analog PWR
AVSS	-	Analog Ground	Hardware Monitor Analog GND

9 System Clock Specifications

9.1 System Clock Descriptions and Frequency Specifications

Table 9-1 to Table 9-3 list the SP5100 Clock description and frequency specifications.

Table 9-1: SP5100 System Clock Descriptions

Clock Domain	Frequency	Source	Usage
PCIE_RCLKP, PCIE_RCLKN	100MHz	Main clock generator	Reference clock for A-Link Express and internal PLL for core logic and ACPI timers.
SATA_X1, SATA_X2	25MHz	25MHz Crystal	SATA Controller Reference clock
X1, X2	32kHz	32kHz Crystal	RTC reference clock
USBCLK	48MHz	48MHz OSC / 48MHZ from main clock generator	USB Controllers and HD Audio Reference clock

Table 9-2: SP5100 System Clock Input Frequency Specifications

Clock	Frequency	Min	Max
USBCLK	48.000 MHz	47.995 MHz	48.005 MHz
SATA_X1, SATA_X2	25.000 MHz	24.997 MHz	25.005 MHz
PCIE_RCLKP, PCIE_RCLKN	100.000 MHz	99.999950 (-50 PPM)	100.00005 (+ 50 PPM)
X1, X2	32kHz	32.768 KHz	

Table 9-3: SP5100 System Clock Output Frequency Specifications

Clock	Frequency	Min	Max
PCICLK {5:0}	33.000 MHz	30.03 MHz	33.33 MHz
LPC CLK	33.000 MHz	30.03 MHz	33.33 MHz
RTC CLOCK	32kHz	32.768 KHz	

9.2 System Clock AC Specifications

Table 9-4 to Table 9-9 list all the AC specifications of SP5100 clocks, some at specific VIH/VIL combinations. Figure 9-1 to Figure 9-3 below illustrate the timing labels that appear in those tables.

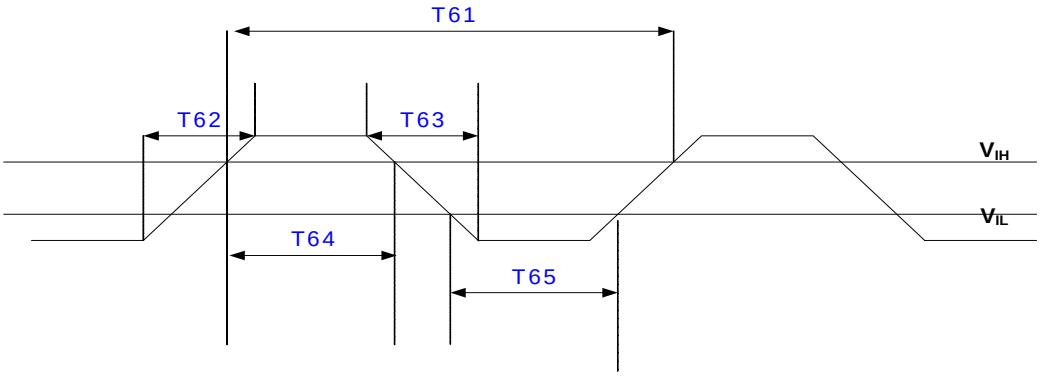


Figure 9-1: Timing Labels for AC Specifications of the SP5100 Clocks

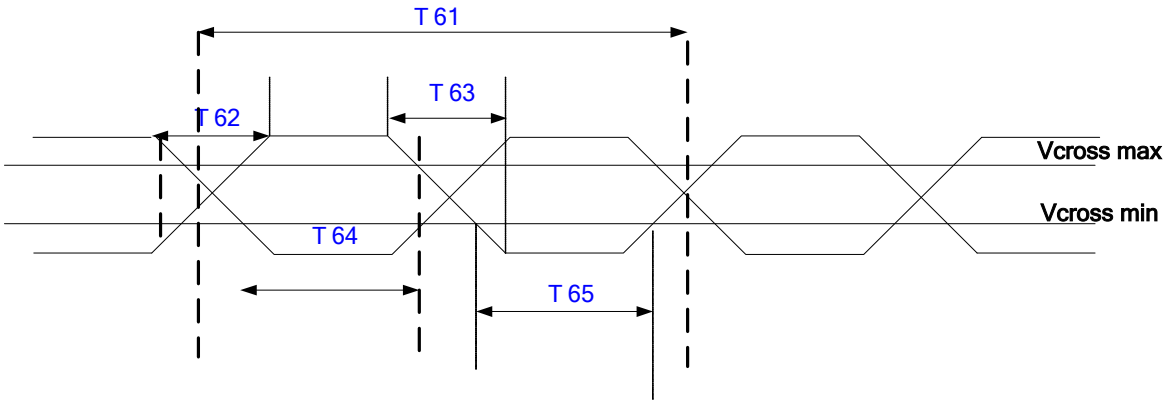


Figure 9-2: Timing Labels for AC Specifications of the SP5100 Diff Clocks

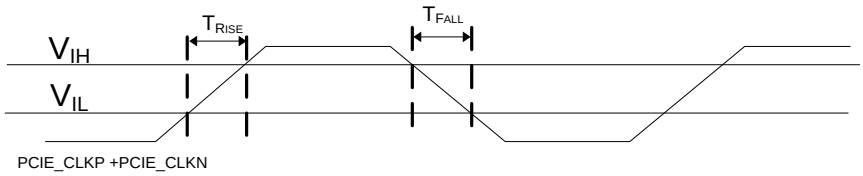


Figure 9-3: SP5100 Diff Clocks Rise and Fall Time Measurement

Table 9-4: 48MHz USB Clock AC Specifications

48 MHz USB					
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Note**
T61	Clock Period	20.831	20.836	ns	1
T62	Clock/Data rise time	0.5	3.0	ns	2
T63	Clock/Data fall time	0.5	3.0	ns	
T64	Clock high period	8.8	11	ns	
T65	Clock low period	7.7	10	ns	

48 MHz USB					
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Note**
-	Max Jitter	-	130	ps	-
-	Duty Cycle	45	55	%	-

Notes:
1 Clock frequency tolerance is +/- 100 ppm
2 VIL= 0.4 V ; VILmax = 0.6 V and VILmin = 0 V
VIH = 2.4 V; VIHmax=VDDR and VIHmin = 2.0 V

Table 9-5: RTC X1 Clock AC Specifications

RTC X1 Clock					
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Note**
T61	Clock Period	Typical at 32.7		kHz	1
T62	Clock/Data rise time	0.5	5	µs	2
T63	Clock/Data fall time	0.5	5	µs	
T64	Clock high period	13	17	µs	
T65	Clock low period	13	17	µs	
-	Duty Cycle	45	55	%	-
-	Frequency Tolerance	-20	20	PPM	-

Notes
1 Min/Max specifications depend on accuracy of the crystal used.
2 VIL= 0.25 V ; VILmax = 250 mV and VILmin = 0 V
VIH = 0.75 V; VIHmax=1V and VIHmin = 750 mV

Table 9-6: LPC Clock AC Specifications

LPC Clock					
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Note**
T61	Clock Period	30	33.3	ns	-
T62	Clock/Data rise time	-	3	ns	-
T63	Clock/Data fall time	-	3	ns	-
T64	Clock high period	12	-	ns	-
T65	Clock low period	12	-	ns	-

Table 9-7: PCI Clock AC Specifications

PCI Clock (6 clocks, PCICLK[5:0])					
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Note**
T61	Clock Period	30	33.3	ns	-
T62	Clock/Data rise time	-	3.0	ns	-
T63	Clock/Data fall time	-	3.0	ns	-
T64	Clock high period	12	-	ns	-
T65	Clock low period	12	-	ns	-

Table 9-8: PCI Express® Clock AC Specifications

Symbol	Parameter	Min	Max	Units	Note
T61	Clock Period	9.872	10.128	ns	SSC disabled
T62	Clock rise edge rate	0.6	4.0	V/ns	See Figure 9-2 and Note below
T63	Clock fall edge rate	0.6	4.0	V/ns	
T64	Clock high period	3	7	ns	-
T65	Clock low period	3	7	ns	-
ViH	Diff Clock input high	+150	-	mV	See Figure 9-3
ViL	Diff Clock input low	-	-150	mV	
Vcross	Absolute crossing point	+250	+550	mV	-
Vcross delta	Variation across Vcross	-	+140	mV	-

Note: Signal must be monotonic throughout the Rise and all time region.

Table 9-9: RTC 32-KHz Output Clock AC Specifications

RTC 32-KHZ output					
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Note**
T61	Clock Period	32.768		KHz	-
T62	Clock/Data rise time	2.2	0.33	V/ns	Nominal voltage 3.3 V
T63	Clock/Data fall time	2.2	0.33	V/ns	
T64	Clock high period	13.7	-	µs	-
T65	Clock low period	16.8	-	µs	-

10 States of Power Rails during ACPI S1 to S5 States

SP5100 supports the ACPI states S1 to S5. Table 10-1 below shows the expected state of each power rail during these power states.

Table 10-1: State of Each Power Rail during ACPI S1 to S5 States

Pin name	Schematic Signal	ACPI STATE			
		S0	S1/S2	S3	S4/S5
VDDQ	+3.3_SB_R	+3.3 V	+3.3 V	0 V	0 V
VDD	+1.2_SB_R	+1.2 V	+1.2 V	0 V	0 V
S5_1.2V	S5 Power	+1.2 V	+1.2 V	+1.2 V	+1.2 V
VDD33_18	VDD33_18	3.3V	3.3V	0 V	0 V
AVDDC	Analog USB 2.0 Power	+3.3 V	+3.3 V	+3.3 V	+3.3 / 0 V
AVDDTX_[5:0] /AVDDRX_[5:0]	USB_AVDD	+3.3 V	+3.3 V	+3.3 V	+3.3 / 0 V
USB_PHY_1.2V	USB Phy digital power	+1.2 V	+1.2 V	+1.2 V	+1.2 / 0 V
AVDD_SATA	SATA Power	+1.2 V	+1.2 V	0 V	0 V
PLLVDD_SATA	SATA PLL Power	+1.2 V	+1.2 V	0 V	0 V
XTLVDD_SATA	SATA XTAL Power	+3.3 V	+3.3 V	0 V	0 V
V5_VREF	+5-V Ref Voltage	+5.0 V	+5.0 V	0 V	0 V
AVDDCK_3.3V	PLL Analog Power	+3.3 V	+3.3 V	0 V	0 V
AVDDCK_1.2V	PLL Digital Power	+1.2 V	+1.2 V	0 V	0 V
S5_3.3V	S5 I/O Power	+3.3 V	+3.3 V	+3.3 V	+3.3 V
PCIE_PVDD	PCI Express® PLL Power	+1.2 V	+1.2 V	0 V	0 V
PCIE_VDDR	PCI Express I/O Power	+1.2 V	+1.2 V	0 V	0 V
SLP_S3#	SLP_S3#	+3.3 V	+3.3 V	0 V	0 V
SLP_S5#	SLP_S5#	+3.3 V	+3.3 V	+3.3 V	0 V
PWR_GOOD	SB_PWROK	+3.3 V	+3.3 V	0 V	0 V
SUS_STAT#	SUS_STAT#	+3.3 V	0 V	0 V	0 V
RSMRST#	RSMRST#	+3.3 V	+3.3 V	+3.3 V	+3.3 V

11 Electrical Characteristics

Note: Values quoted in this section are preliminary and require further verification.

11.1 Absolute Maximum Ratings

Table 11-1 specifies the absolute maximum ratings that should never be exceeded. Exceeding the specified absolute maximum ratings may damage the ASIC. These ratings are guidelines for absolute worst case operating conditions and should not to be interpreted as recommended operating condition.

Table 11-1: Absolute Maximum Rating

Signal Name	Limits (V)	With respect to	Description
VDD_[12:1]	-0.5 to 1.32	VSS	Core power
VDDQ_[28:1]	-0.5 to 3.66	VSS	3.3-V I/O Power
VDD33_18	-0.5 to 3.66	VSS	3.3-V I/O Power
S5_1.2V_[4:1]	-0.5 to 1.32	VSS	1.2-V S5 Power
S5_3.3V_[6:1]	-0.5 to 3.66	VSS	3.3-V S5 Power
AVDDCK_3.3V	-0.5 to 3.66	AVSSCK	3.3-V power for analog PLLs
AVDDCK_1.2V	-0.5 to 1.32	AVSSCK	1.2-V power for analog PLLs
PCIE_PVDD	-0.5 to 1.32	PCIE_VSS	A-Link Express II PLL Power
PCIE_VDDR[13:1]	-0.5 to 1.32	PCIE_VSS	A-Link Express II Analog power
AVDD_SATA[15:1]	-0.5 to 1.32	AVSS_SATA	SATA Analog Power
PLLVDD_SATA_[2:1]	-0.5 to 1.32	AVSS_SATA	SATA PLL Power
XTLVDD_SATA	-0.5 to 1.32	AVSS_SATA	SATA XTAL Power
VBAT	-0.5 - 3.6V BAT	RTC_GND	RTC backup power
AVDDC	-0.5 to 3.66	AVSSC	Analog Power for USB PHY PLL
AVDDRX_[5:0]	-0.5 to 3.66	AVSS_USB	Analog Power for USB PHY RX
AVDDTX_[5:0]	-0.5 to 3.66	AVSS_USB	Analog Power for USB PHY TX
USB_PHY_1.2V[5:1]	-0.5 to 1.32	AVSS_USB	1.2-V USB PHY standby Power
V5_VREF	-0.5 to 5.5	VSS	5-V Reference voltage for PCI interface
Any 3.3 V input signal	-0.5 to 3.66	VSS	See Section 3 for signal names
Any 3,.3 / 5 V tolerant input signal	-0.5 to VREF+0.5	VSS	

11.2 Functional Operating Range for Signal Input

The functional operating range for any signal input to the SP5100 is +/-5% of the signal's typical input level.

11.3 DC Characteristics

Table 11-2: DC Characteristics for Power Supplies to the SP5100

Signal Name	Description	Min. Voltage	Typical Voltage	Max. Voltage	Unit
AVDDCK_1.2V	Core PLL digital power	1.14	1.2	1.26	V
PCIE_PVDD	A-Link Express II PLL power	1.14	1.2	1.26	V
PCIE_VDDR[13:1]	A-Link Express II power	1.14	1.2	1.26	V
PLLVDD_SATA[2:1]	SATA PLL power	1.14	1.2	1.26	V
AVDD_SATA[15:1]	SATA analog power	1.14	1.2	1.26	V
S5_1.2V	Standby power	1.14	1.2	1.26	V
USB_PHY_1.2V[5:1]	USB PHY standby power	1.14	1.2	1.26	V
VDD[12:1]	Core voltage	1.14	1.2	1.26	V
VDD33_18	I/O power	3.13	3.3	3.465	V
XTLVDD_SATA	SATA XTAL power	3.135	3.3	3.465	V
VBAT	RTC backup power	2.5*	3.3	3.6	V
AVDDCK_3.3V	Core PLL analog power	3.135	3.3	3.465	V
AVDDC	Analog power for USB PHY PLL	3.135	3.3	3.465	V
AVDDRX_[5:0]	Analog power for USB PHY	3.135	3.3	3.465	V
AVDDTX_[5:0]	Analog power for USB PHY	3.135	3.3	3.465	V
S5_3.3v[6:1]	Core standby power	3.135	3.3	3.465	V
VDDQ[28:1]	I/O power	3.135	3.3	3.465	V
V5_VREF	5V reference voltage	4.75	5	5.25	V

* **Note:** For VBAT below 2.5 V, the battery-low error will occur. At 2.0 V, the CMOS content may be lost.

Table 11-3: DC Characteristics for Interfaces on the SP5100

Symbol	Parameter	Minimum	Maximum	Unit	Condition
GPIO/ IMC_GPIO					
VDDQ	I/O power	3.135	3.46	V	
VIL	Input Low Voltage	-0.5	1.3	V	
VIH	Input High Voltage	1.8	VDD	V	
VOL	Output Low Voltage	-	0.4	V	IOL = 8.0 mA
VOH	Output High Voltage	2.4	-	V	IOH = -8.0 mA
ILI	Input Leakage Current	-	+/-10	µA	
CIN	Input Capacitance	-	10	pF	
PCI					
VDDQ	I/O power	3.135	3.46	V	
V5REF	Reference	3.135	5.25	V	
VIL	Input Low Threshold	-0.5	0.3VDD	V	
VIH	Input High Threshold	0.5VDD	V5REF	V	
VOL	Output Low Voltage	-	0.4	V	IOL = 4.0 mA
VOH	Output High Voltage	2.4	-	V	IOH = -4.0 mA
ILI	Input Leakage Current	-	+/-10	µA	

Symbol	Parameter	Minimum	Maximum	Unit	Condition
CIN	Input Capacitance	-	10	pF	
IDE					
VDD33_18*	I/O power	3.135	3.46	V	
VIH	Input High Voltage	0.5VDD	V5REF	V	
VIL	Input Low Voltage	-0.5	03VDD	V	
VOL	Output Low Voltage	-	0.662	V	IOL= 6 mA
VOH	Output High Voltage	VDD-0.66	-	V	IOH = -6 mA
ILI	Input Leakage Current	-	+/-10	µA	Pull-up & pull-down Resistors disabled
CIN	Input Capacitance	-	10	pF	
CPU					
VCPU_IO	CPU IO Voltage	-	-	V	
VIL	Input Low Voltage	-0.5	0.58VCPU_IO	V	
VIH	Input High Voltage	0.73VCPU_IO	VCPU_IO	V	
VOL	Output Low Voltage	-0.15	0.25VCPU_IO	V	IOL = 4.0 mA
VOH	Output High Voltage / Internal Pull-up Voltage	-	VCPU_IO	V	
ILI	Input Leakage Current	-	+/-10	µA	
CIN	Input Capacitance	-	10	pf	
All signals from SP5100 to CPU are open drain					
NB – ALLOW_LDTSTP					
VIL	Input Low Voltage	-0.5	0.6	V	
VIH	Input High Voltage	1.0	-	V	
VOL	Output Low Voltage	-	0.4	V	IOL = 4.0 mA
VOH	Output High Voltage / Internal Pull-up Voltage	-	3.3	V	With external pull-up
ILI	Input Leakage Current	-	+/-10	µA	
CIN	Input Capacitance	-	10	pf	
LPC					
See values for the PCI pins.					
RSMRST#					
S5_3.3V	Core standby power	3.1	3.4	V	
VIL	Input Low Voltage	-0.5	1.5	V	
VIH	Input High Voltage	1.5	2.0	V	
ILI	Input Leakage Current	-	+/-10	µA	
CIN	Input Capacitance	-	10	pf	
SBPWRGD					
VDDQ	I/O power	3.1	3.4	V	
VIL	Input Low Voltage	-0.5	1.5	V	
VIH	Input High Voltage	1.5	2.0	V	
ILI	Input Leakage Current	-	+/-10	µA	
CIN	Input Capacitance	-	10	pf	

Table 11-4: GPIO/GEVENT Input DC Characteristics

Pin Name	Voltage	ViL(V)		ViH (V)	
		Min	Max	Min	Max
SATA_IS3#/GPIO0	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
ROM_CS#/GPIO1	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25

Pin Name	Voltage	ViL(V)		ViH (V)	
		Min	Max	Min	Max
SPKR/GPIO2	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
FANOUT0/GPIO3	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
SMARTVOLT1/ SATA_IS2#/GPIO4	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
SMARTVOLT2/ SHUTDOWN#/ GPIO5	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
SATA_IS1#/GPIO6	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
DDC1_SDA/GPIO8	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
DDC1_SCL/GPIO9	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
SATA_IS0#/GPIO10	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
SPI_DO/GPIO11	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
SPI_DI/GPIO12	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
LAN_RST#/GPIO13	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
ROM_RST#/ GPIO14	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
IDE_D[15:0]/GPIO[30:15]	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
SPI_HOLD#/ GPIO31	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
SPI_CS1#/GPIO32	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
INTE#/GPIO33	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
INTF#/GPIO34	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
INTG#/GPIO35	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
INTH#/GPIO36	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
AZ_SDIN0/ GPIO42	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
AZ_SDIN1/ GPIO43	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
AZ_SDIN2/ GPIO44	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
AZ_SDIN3/GPIO46	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
SPI_CLK/GPIO47	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
FANOUT1/GPIO48	3.3 V	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
FANOUT2/GPIO49	3.3 V	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
FANIN0/GPIO50	3.3 V	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
FANIN1/GPIO51	3.3 V	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25

Pin Name	Voltage	ViL(V)		ViH (V)	
		Min	Max	Min	Max
FANIN2/GPIO52	3.3 V	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
VIN[7:0]/GPIO[60:53]	3.3 V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
TEMPIN[2:0]/GPIO[63:61]	3.3 V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
TEMPIN3/TALERT#/ GPIO64	S5_3.3V	-0.5	0.3* VDDQ	0.7*VDDQ	VDDQ + 0.25
BMREQ#/REQ5#/ GPIO65	3.3 V	-0.5	0.3* VDDQ	0.7*VDDQ	VDDQ + 0.25
LLB#/GPIO66	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
SATA_ACT#/ GPIO67	3.3 V	-0.5	0.3* VDDQ	0.7*VDDQ	VDDQ + 0.25
LDRQ1#/GNT5#/ GPIO68	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
REQ3#/GPIO70	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
REQ4#/GPIO71	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
GNT3#/GPIO72	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
GNT4#/GPIO73	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
USB_OC[5:0]#/GPM[5:0]#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
BLINK/GPM6#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
SYS_RESET#/ GPM7#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
USB_OC8#/ AZ_DOCK_RST#/ GPM8#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
SLP_S2/GPM9#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
RI#/EXTEVENT0#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
LPC_SMI#/ EXTEVENT1#	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
SMBALERT#/THRMTRIP#/ GEVENT2#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
LPC_PME#/ GEVENT3#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
PCI_PME#/ GEVENT4#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
S3_STATE/ GEVENT5#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
USB_OC6#/ GEVENT6#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
GEVENT7#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
WAKE#/GEVENT8#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
SCL0/GPOC0#	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25

Pin Name	Voltage	ViL(V)		ViH (V)	
		Min	Max	Min	Max
SDA0/GPOC1#	3.3 V (5-V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
SCL1/GPOC2#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
SDA1/GPOC3#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
IMC_GPIO[17:16, 12:11, 7:3, 1:0]	S5_3.3V (5-V Tolerance)	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	V5_Ref + 0.25
IMC_GPIO[41:18, 15:13, 10:8, 2]	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25

Table 11-5: GPIO/GEVENT Output DC Characteristics

Pin Name	Parameter	VOL	VOH
		Minimum	Maximum
All GPIO and GEVENT pins listed in Table 11-4	Output High Voltage	**2.4 V**	**—**
	Output Low Voltage	**—**	**0.4 V**
		Output Drive	
	Output Drive	**8 mA**	

Table 11-6: RTC Clock Output DC Characteristics

Pin Name	Parameter	VOL	VOH
		Minimum	Maximum
RTCCLK	Output High Voltage	**2.4 V**	**—**
	Output Low Voltage	**—**	**0.4 V**
		Output Drive	
	Output Drive	**4 mA Min / 8 mA Max**	
		Output drive controlled by PMIO 42 [6]	

11.4 Reset Signal Requirements

Table 11-7: Reset Signal Requirements

Pin Name	Assertion requirements	Comments
SYS_RST#	Must be asserted for 10 ms minimum.	At deassertion, the SYS_RST# signal will not be sampled by the internal logic for a period of 32 ms as it first goes through the internal debouncing circuit.
RSMRST#	Must be asserted for 10 ms minimum.	At deassertion, the RSMRST# signal will not be sampled by the internal logic for a period of 32 ms as it first goes through the internal debouncing circuit.
KBRST#	Must be asserted for 30 ns minimum. The KBRST# should be de-asserted before A_RST# and LDT_RST# are de-asserted.	—

11.5 RTC Battery Current Consumption

The RTC battery current consumption is estimated as follows:

Table 11-8: RTC Battery Current Consumption

Power State	RTC Battery Current	
	Typical	Maximum
G3 (Off)	< 0.5 µA	< 4 µA
S0-S5	< 0.2 µA	-

RTC battery life is calculated using the rated capacity of the battery and typical current numbers. The typical batteries used for RTC are normally rated for 170 mAh and the worst case current consumption for the SP5100 is 4.0 µA. Thus, the life of battery will be calculated as follows:

170,000 µAh / 4 µA = 42,500 h = 4.8 years

12 Package Information

12.1 Physical Dimensions

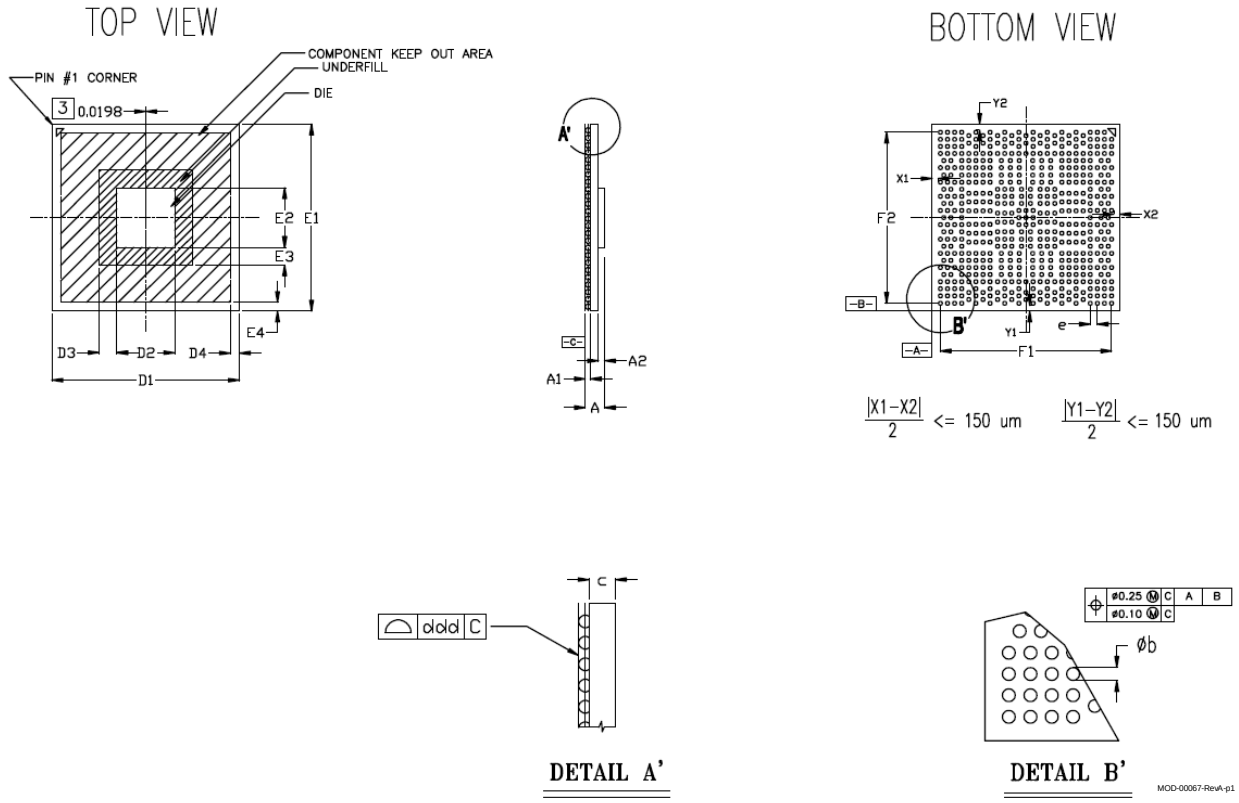


Figure 12-1: SP5100 21 mm x 21 mm 0.8 mm Pitch 528-FCBGA Package Outline

Table 12-1: SP5100 21 mm x 21 mm 0.8 mm Pitch 528-FCBGA Physical Dimensions

Ref.	Min(mm)	Nominal (mm)	Max. (mm)
c	0.56	0.66	0.76
A	1.77	1.92	2.07
A1	0.30	0.40	0.50
A2	0.81	0.86	0.91
ϕb	0.40	0.50	0.60
D1	20.85	21.00	21.15
D2	-	6.47	-
D3	2.00	-	-
D4	1.00	-	-
E1	20.85	21.00	21.15
E2	-	6.68	-
E3	2.00	-	-
E4	1.00	-	-
F1	-	19.20	-
F2	-	19.20	-
e (min. pitch)	-	0.80	-
ddd	-	-	0.20

Note: Maximum height of SMT components is 0.650 mm.

12.2 Pressure Specification

To avoid damages to the ASIC (die or solder ball joint cracks) caused by improper mechanical assembly of the cooling device, follow the recommendations below:

- It is recommended that the maximum load that is evenly applied across the contact area between the thermal management device and the die does not exceed 6 lbf. Note that a total load of 4-6 lbf is adequate to secure the thermal management device and achieve the lowest thermal contact resistance with a temperature drop across the thermal interface material of no more than 3°C. Also, the surface flatness of the metal spreader should be 0.001 inch/1 inch.
- Pre-test the assembly fixture with a strain gauge to make sure that the flexing of the final assembled board and the pressure applying around the ASIC package will not exceed 600 micron strain under any circumstances.
- Ensure that any distortion (bow or twist) of the board after SMT and cooling device assembly is within industry guidelines (IPC/EIA J-STD-001). For measurement method, refer to the industry approved technique described in the manual IPC-TM-650, section 2.4.22.

13 Thermal Information

This section describes some key thermal parameters of the SP5100. For a detailed discussion on these parameters and other thermal design descriptions including package level thermal data and analysis, please consult the *Thermal Design and Analysis Guidelines for SP5100*.

Table 13-1 SP5100 Thermal Limits

Parameter	Minimum	Nominal	Maximum	Unit	Note
Operating Case Temperature	0	—	105	°C	1
Absolute Rated Junction Temperature	—	—	125	°C	2
Storage Temperature	-40	—	60	°C	
Ambient Temperature	0	—	55	°C	3
Thermal Design Power	—	4.5	—	W	4

Notes:
1 - The maximum operating case temperature is the die geometric top-center temperature measured through proper thermal contact to the back side of the die based on the methodology given in the document *Thermal Design and Analysis Guidelines for SP5100* (Chapter 11). This is the temperature at which the functionality of the chip is qualified.
2 - The maximum absolute rated junction temperature is the junction temperature at which the device can operate without causing damage to the ASIC.
3 - The ambient temperature is defined as the temperature of the local intake air to the thermal management device. The maximum ambient temperature is dependent on the heat sink's local ambient conditions as well as the chassis' external ambient, and the value given here is based on AMD's reference server heat sink solution for the SP5100. Refer to Chapter 5 in the *Thermal Design and Analysis Guidelines for SP5100* for heat sink and thermal design guidelines. Refer to Chapter 6 of the above mentioned document for details of ambient conditions.
4 - Thermal Design Power (TDP) is defined as the highest power dissipated while running currently available worst case applications at nominal voltages. The core voltage was raised to 5% above its nominal value for measuring the ASIC power. Since the core power of modern ASICs using 65nm and smaller process technology can vary significantly, parts specifically screened for higher core power were used for TDP measurement. The TDP is intended only as a design reference, and the value given here is preliminary.

14 Testability

14.1 Test Control Signals

Table 14-1 below shows the signals used for the integrated test controller of the SP5100.

Table 14-1: Signals for the Test Controller of the SP5100

Signal Name	Description
14M_X1 / 14M_X2	25-MHz Reference Clock.
TEST0	Test0 input.
TEST1	Test1 input.
TEST2	Test2 input.

Table 14-2 shows how Test[2:0] are used to select the normal operation, ASIC debug, or test mode.

Table 14-2: Test Mode Signals

TEST2	TEST1	TEST0	Test Mode	Description
0	0	0	None	Normal operation
0	0	1	Reserved	Reserved for ASIC debug
0	1	x	Test Mode	EnableTest Mode
1	X	X	Reserved	Reserved for ASIC debug

When TEST2 is low, a low on TEST1 will reset all test logic and allow TEST0 to choose between normal operation and the reserved debug mode. A high on TEST1 should be followed by a bit sequence on TEST0 to define the test mode into which the SP5100 will enter. A new test mode can be entered when a new bit sequence is transmitted. In addition to resetting the test controller asynchronously with TEST1, a bit sequence can also be used to synchronously change the test mode. Table 14-3 shows the legal bit sequences for TEST0. Note: Once the Test mode or Test mode and sub test mode is entered, Test2 and Test1 should be kept at 0, 1 respectively until the requirement for the Test Mode is completed.

Table 14-3: TEST0 Bit Sequence

TEST0 bit sequence	Test Mode
11111	Look for first 0 to define a new test mode
00000	Reserved
00001	Alt Pull High Test
00010	Pull Outputs High
00011	Pull Outputs Low
00100	Pull Outputs to Z
00101	XOR Test Mode

Figure 14-1 illustrates the data timing for the test signals with respect to the OSC clock. Any timing reference referred in this section is assumed to be based on OSC clock running at 25 MHz. The OSC clock can be slowed down to 1 MHz as long as the bit stream applied on TEST0 pin is also in sync with this clock. The 25-MHz OSC clock should be disconnected first. For setting any Test 0 bit sequence, the OSC clock is required only up-to the time the mode set is completed. After this the clock can be stopped and as long as TEST1 and Test2 pins are set to {1, 0} respectively to maintain the selected mode to be

active. Note that once TEST1 is set to one, TEST0 needs to be asserted to one for at least 8 clocks before transmitting the test mode bit sequence. The rising of “Internal Test Mode” in the diagram indicates the time when the SP5100 enters into test mode.

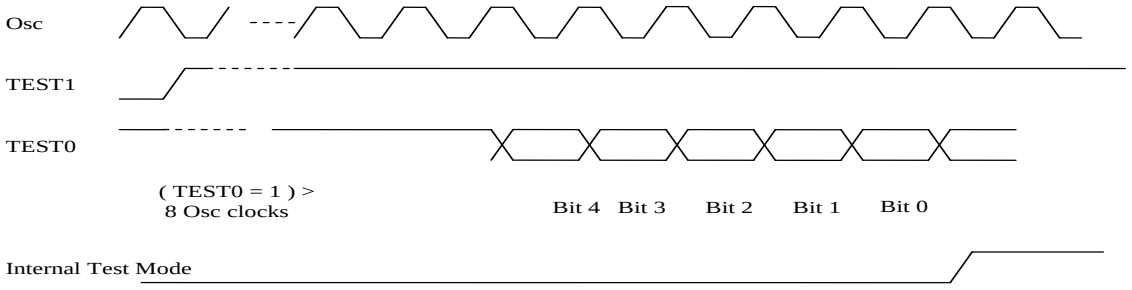


Figure 14-1: Test Mode Capturing Sequence Timing

14.2 XOR Chain Test Mode

14.2.1 Brief Description of an XOR Chain

A sample of a generic XOR chain is shown in the figure below.

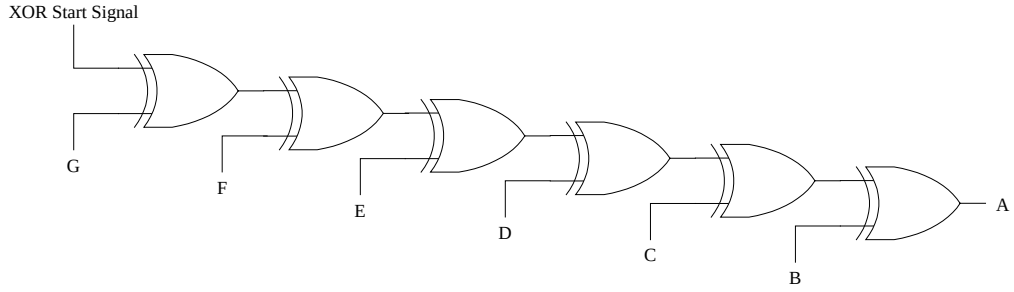


Figure 14-2: A Generic XOR Chain

Pin A is assigned to the output direction, and pins B through F are assigned to the input direction. It can be seen that after all pins from B to F are assigned to logic 0 or 1, a logic change in any one of these pins will toggle the output pin A.
The following is the truth table for the XOR Chain shown in Figure 14-2. The XOR start signal is assumed to be logic 1.This is an internal signal to the ASIC and is not part of the XOR tree pins listed in Table 14-5.
Once the inputs are set to the respective value the output pin will reflect the correct value within 200 ns. Note: OSC clock is not required to be running after the mode is already set and the pads are exercised in XOR Tree function.

Table 14-4: Truth Table for an XOR Chain

Test Vector number	Input Pin G	Input Pin F	Input Pin E	Input Pin D	Input Pin C	Input Pin B	Output Pin A
1	0	0	0	0	0	0	1
2	1	0	0	0	0	0	0
3	1	1	0	0	0	0	1
4	1	1	1	0	0	0	0
5	1	1	1	1	0	0	1
6	1	1	1	1	1	0	0
7	1	1	1	1	1	1	1

14.2.2 Description of the SP5100 XOR Chain

During XOR Chain Test Mode, most of the chip pads on the SP5100 are connected together using XOR gates as shown in Figure 14-3. The first input of the chain is connected to a logic level high (internal connection), and all pads (listed in Table 14-5) are configured as inputs except for the last pad in the chain, which is configured as an output. KBRST#/GEVENT1# is the start of the chain and SERIRQ is the end of the chain. Table 14-5 lists all pads that are on the SP5100 XOR chain, as well as and their order of connection. Pads are chained together in the shown order, i.e., pad number 1 is the first pad on the XOR chain, pad number 2 the second, and so on.

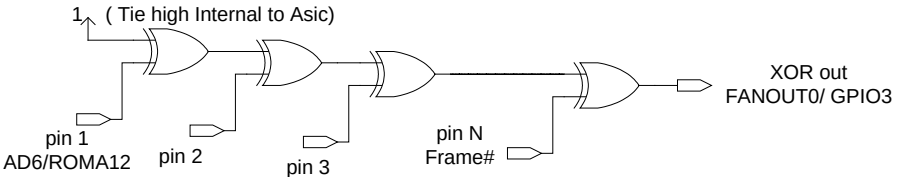


Figure 14-3: On-chip XOR Chain connectivity

Table 14-5: List of Pins on the SP5100 XOR Chain and the Order of Connection

XOR #	Pin Name
1	KBRST#/GEVENT1#
2	GA20IN/GEVENT0#
3	NB_PWRGD
4	SATA_ACT#/GPIO67
5	LDRQ1#/GNT5#/GPIO68
6	AD20
7	CBE2#
8	REQ2#
9	BMREQ#/REQ5#/GPIO65
10	REQ4#/GPIO71
11	GNT3#/GPIO72
12	CLKRUN#
13	REQ3#/GPIO70

XOR #	Pin Name
14	GNT4#/GPIO73
15	INTF#/GPIO34
16	REQ1#
17	GNT1#
18	INTE#/GPIO33
19	INTH#/GPIO36
20	GNT0#
21	INTG#/GPIO35
22	AD31
23	GNT2#
24	REQ0#
25	AD29
26	AD30

XOR #	Pin Name
27	AD25
28	AD27
29	AD28
30	FRAME#
31	IRDY#
32	AD24
33	AD26
34	AD19
35	AD16
36	TRDY#
37	AD21
38	AD22
39	AD23
40	CBE3#
41	AD17
42	STOP#
43	DEVSEL#
44	PERR#
45	CBE0#
46	AD9
47	AD18
48	SERR#
49	LOCK#
50	AD2
51	AD4
52	AD7
53	AD6
54	AD14
55	CBE1#
56	PAR
57	AD15
58	AD0
59	AD5
60	AD10
61	PCICLK4
62	PCICLK5/GPIO41
63	AD8
64	AD3
65	AD12
66	AD11
67	AD13
68	AD1
69	PCICLK0
70	PCICLK1
71	PCICLK3
72	PCICLK2
73	FANIN2/GPIO52

XOR #	Pin Name
74	FANIN1/GPIO51
75	FANIN0/GPIO50
76	FANOUT0/GPIO3
77	FANOUT2/GPIO49
78	FANOUT1/GPIO48
79	AZ_SDOUT
80	AZ_BITCLK
81	AZ_SYNC
82	A_RST#
83	AZ_SDIN3/GPIO46
84	PCIRST#
85	AZ_RST#
86	AZ_SDIN2/GPIO44
87	AZ_DOCK_RST#/GPM8#
88	LPC_PME#/GEVENT3#
89	SUS_STAT#
90	SDA1/GPOC3#
91	SCL1/GPOC2#
92	AZ_SDIN1/GPIO43
93	AZ_SDIN0/GPIO42
94	SMBALERT#/THRMTRIP#/ GEVENT2#
95	SYS_RESET#/GPM7#
96	ROM_RST#/GPIO14
97	SLP_S2/GPM9#
98	WAKE#/GEVENT8#
99	PWR_BTN#
100	SPI_DI/GPIO12
101	DDR3_RST#/GEVENT7#
102	SPI_HOLD#/GPIO31
103	SPI_CS1#/GPIO32
104	SPI_DO/GPIO11
105	S3_STATE/GEVENT5#
106	RI#/EXTEVNT0#
107	PCI_PME#/GEVENT4#
108	BLINK/GPM6#
109	SPI_CLK/GPIO47
110	LLB#/GPIO66
111	USB_OC0#/GPM0#
112	USB_OC1#/GPM1#
113	USB_FSD13P
114	USB_FSD12P
115	VIN3/GPIO56
116	VIN4/GPIO57
117	VIN2/GPIO55
118	VIN1/GPIO54
119	VIN0/GPIO53

XOR #	Pin Name
120	VIN7/GPIO60
121	VIN6/GPIO59
122	VIN5/GPIO58
123	TEMPIN3/TALERT#/GPIO64
124	TEMPIN2/GPIO63
125	TEMPIN1/GPIO62
126	TEMPIN0/GPIO61
127	USB_OC2#/GPM2#
128	USB_OC3#/GPM3#
129	USB_OC4#/IR_RX/GPM4#
130	USB_OC5#/IR_TX/GPM5#
131	USB_OC6#/IR_CTRL/ GEVENT6#
132	USBCLK/ 14M_25M_48M_OSC
133	IMC_GPO17
134	IMC_GPIO40
135	IMC_GPIO41
136	IMC_GPIO9
137	IMC_GPIO8
138	IMC_GPIO12
139	IMC_GPIO15
140	IMC_GPO16
141	IMC_GPIO38
142	IMC_GPIO39
143	IMC_GPIO18
144	IMC_GPIO13
145	IMC_GPIO34
146	IMC_GPIO35
147	IMC_GPIO37
148	IMC_GPIO36
149	IMC_GPIO19
150	IMC_GPIO10
151	IMC_GPIO14
152	IMC_GPIO11
153	IMC_GPIO32
154	IMC_GPIO33
155	IMC_GPIO0
156	LDT_PG
157	IMC_GPIO1
158	IMC_GPIO4
159	IMC_GPIO29
160	IMC_GPIO31
161	IMC_GPIO30
162	IMC_GPIO7
163	IMC_GPIO25
164	IMC_GPIO27

XOR #	Pin Name
165	IMC_GPIO28
166	IMC_GPIO26
167	IMC_GPIO24
168	IMC_GPIO23
169	IMC_GPIO22
170	IMC_GPIO21
171	IMC_GPIO20
172	IMC_GPIO5
173	IMC_GPIO6
174	IDE_RST#/F_RST#/ IMC_GPO3
175	ALLOW_LDTSTP
176	PROCHOT#
177	LDT_STP#
178	LDT_RST#
179	LPCCLK1
180	LPCCLK0
181	SPI_CS2#/IMC_GPIO2
182	LDRQ0#
183	LAD1
184	LAD0
185	LFRAME#
186	LAD2
187	LAD3
188	LPC_SMI#/EXTEVNT1#
189	SDA0/GPOC1#
190	CLK_REQ2#/SATA_IS5#/ FANIN3/GPIO40
191	SPKR/GPIO2
192	DDC1_SDA/GPIO8
193	SMARTVOLT2/SHUTDOWN#/ GPIO5
194	DDC1_SCL/GPIO9
195	SMARTVOLT1/SATA_IS2#/ GPIO4
196	IDE_A2
197	IDE_A0
198	IDE_CS3#
199	IDE_CS1#
200	IDE_IORDY
201	IDE_IRQ
202	IDE_D12/GPIO27
203	IDE_DACK#
204	IDE_A1
205	IDE_D15/GPIO30
206	IDE_IOW#
207	IDE_IOR#
208	IDE_D3/GPIO18

XOR #	Pin Name
209	IDE_D1/GPIO16
210	IDE_D0/GPIO15
211	IDE_DRQ
212	IDE_D14/GPIO29
213	IDE_D2/GPIO17
214	IDE_D13/GPIO28
215	IDE_D11/GPIO26
216	IDE_D4/GPIO19
217	IDE_D9/GPIO24
218	IDE_D6/GPIO21
219	IDE_D5/GPIO20
220	IDE_D10/GPIO25
221	IDE_D8/GPIO23

XOR #	Pin Name
222	IDE_D7/GPIO22
223	SATA_IS0#/GPIO10
224	CLK_REQ3#/SATA_IS1#/ GPIO6
225	SCL0/GPOC0#
226	CLK_REQ0#/SATA_IS3#/ GPIO0
227	CLK_REQ1#/SATA_IS4#/ FANOUT3/GPIO39
228	LAN_RST#/GPIO13
229	SERIRQ

14.2.2.1 Unused Pins

The pins that are part of the XOR chain (see Table 14-5) but are not used for testing must be pulled-up or down before the XOR chain is activated. No pins in the XOR chain should be left floating. All digital or analog pins not included in Table 14-5 are not part of the XOR chain and can be left floating during an XOR test. That includes the output of the XOR chain, FANOUT0/GPIO3, and other pads shown in Table 14-6 below.

Table 14-6: Pins Excluded from the XOR Chain

Pin Name	Description
RSMRST#	Used for capturing straps
PWR_GOOD	Used for capturing straps
SLP_S5#	In S5 power well. No test support.
SLP_S3#	In S5 power well. No test support.
SIC	No test support
TEST0	Test controller data input
TEST1	Test controller mode
TEST2	Reserved Test Input
14M_X1	Test control clock
14M_X2	Test control clock
RTCCLK	No test support
SERIRQ	Output of the XOR chain

Appendix A: Pin Listing

Processor Interface	
ALLOW_LDTSTP	**F23**
LDT_PG	**F22**
LDT_STP#	**G25**
LDT_RST#	**G24**
PROCHOT#	**F24**
LPC Interface	
LPCCLK0	**G22**
LPCCLK1	**E22**
LAD0	**H24**
LAD1	**H23**
LAD2	**J25**
LAD3	**J24**
LFRAME#	**H25**
LDRQ0#	**H22**
LDRQ1#/GNT5#/GPIO68	**AB8**
LPC_SMI#/EXTEVNT1#	**K24**
SERIRQ	**V15**
A-Link Express II Interface	
PCIE_RCLKP/NB_LNK_CLKP	**N25**
PCIE_RCLKN/NB_LNK_CLKN	**N24**
PCIE_TX0P	**V23**
PCIE_TX0N	**V22**
PCIE_TX1P	**V24**
PCIE_TX1N	**V25**
PCIE_TX2P	**U25**
PCIE_TX2N	**U24**
PCIE_TX3P	**T23**
PCIE_TX3N	**T22**
PCIE_RX0P	**U22**
PCIE_RX0N	**U21**
PCIE_RX1P	**U19**
PCIE_RX1N	**V19**
PCIE_RX2P	**R20**
PCIE_RX2N	**R21**
PCIE_RX3P	**R18**
PCIE_RX3N	**R17**
PCIE_CALRP	**T25**
PCIE_CALRN	**T24**
PCI 33 Interface	
PCICLK0	**P4**
PCICLK1	**P3**
PCICLK2	**P1**
PCICLK3	**P2**
PCICLK4	**T4**
PCICLK5/GPIO41	**T3**
A_RST#	**N2**
PCIRST#	**N1**
INTE#/GPIO33	**AD3**
INTF#/GPIO34	**AC4**
INTG#/GPIO35	**AE2**
INTH#/GPIO36	**AE3**
AD0	**U2**
AD1	**P7**
AD2	**V4**
AD3	**T1**
AD4	**V3**
AD5	**U1**
AD6	**V1**
AD7	**V2**
AD8	**T2**
AD9	**W1**
AD10	**T9**
AD11	**R6**
AD12	**R7**
AD13	**R5**
AD14	**U8**
AD15	**U5**
AD16	**Y7**
AD17	**W8**
AD18	**V9**
AD19	**Y8**
AD20	**AA8**
AD21	**Y4**
AD22	**Y3**
AD23	**Y2**
AD24	**AA2**
AD25	**AB4**
AD26	**AA1**
AD27	**AB3**
AD28	**AB2**
AD29	**AC1**
AD30	**AC2**
AD31	**AD1**
CBE0#	**W2**
CBE1#	**U7**
CBE2#	**AA7**
CBE3#	**Y1**
FRAME#	**AA6**

DEVSEL#	**W5**
IRDY#	**AA5**
TRDY#	**Y5**
PAR	**U6**
STOP#	**W6**
PERR#	**W4**
SERR#	**V7**
LOCK#	**V5**
REQ0#	**AC3**
REQ1#	**AD4**
REQ2#	**AB7**
REQ3#/GPIO70	**AE6**
REQ4#/GPIO71	**AB6**
BMREQ#/REQ5#/GPIO65	**AD7**
GNT0#	**AD2**
GNT1#	**AE4**
GNT2#	**AD5**
GNT3#/GPIO72	**AC6**
GNT4#/GPIO73	**AE5**
LDRQ1#/GNT5#/GPIO68	**AB8**
CLKRUN#	**AD6**
USB Interface	
USB_FSD13P	**E6**
USB_FSD13N	**E7**
USB_FSD12P	**F7**
USB_FSD12N	**E8**
USB_HSD11P	**H11**
USB_HSD11N	**J10**
USB_HSD10P	**E11**
USB_HSD10N	**F11**
USB_HSD9P	**A11**
USB_HSD9N	**B11**
USB_HSD8P	**C10**
USB_HSD8N	**D10**
USB_HSD7P	**G11**
USB_HSD7N	**H12**
USB_HSD6P	**E12**
USB_HSD6N	**E14**
USB_HSD5P	**C12**
USB_HSD5N	**D12**
USB_HSD4P	**B12**
USB_HSD4N	**A12**
USB_HSD3P	**G12**
USB_HSD3N	**G14**
USB_HSD2P	**H14**
USB_HSD2N	**H15**
USB_HSD1P	**A13**
USB_HSD1N	**B13**
USB_HSD0P	**B14**
USB_HSD0N	**A14**
USBCLK/14M_25M_48M_OSC	**C8**
USB_RCOMP	**G8**
ATA66/100/133	
IDE_RST#/F_RST#/IMC_GPO3	**F25**
IDE_IORDY	**AA24**
IDE_IRQ	**AA25**
IDE_A0	**Y22**
IDE_A1	**AB23**
IDE_A2	**Y23**
IDE_DACK#	**AB24**
IDE_DRQ	**AD25**
IDE_IOR#	**AC25**
IDE_IOW#	**AC24**
IDE_CS1#	**Y25**
IDE_CS3#	**Y24**
IDE_D0/GPIO15	**AD24**
IDE_D1/GPIO16	**AD23**
IDE_D2/GPIO17	**AE22**
IDE_D3/GPIO18	**AC22**
IDE_D4/GPIO19	**AD21**
IDE_D5/GPIO20	**AE20**
IDE_D6/GPIO21	**AB20**
IDE_D7/GPIO22	**AD19**
IDE_D8/GPIO23	**AE19**
IDE_D9/GPIO24	**AC20**
IDE_D10/GPIO25	**AD20**
IDE_D11/GPIO26	**AE21**
IDE_D12/GPIO27	**AB22**
IDE_D13/GPIO28	**AD22**
IDE_D14/GPIO29	**AE23**
IDE_D15/GPIO30	**AC23**
Serial ATA	
SATA_TX0P	**AD9**
SATA_TX0N	**AE9**
SATA_RX0N	**AB10**
SATA_RX0P	**AC10**
SATA_TX1P	**AE10**
SATA_TX1N	**AD10**
SATA_RX1N	**AD11**
SATA_RX1P	**AE11**
SATA_TX2P	**AB12**
SATA_TX2N	**AC12**
SATA_RX2N	**AE12**
SATA_RX2P	**AD12**
SATA_TX3P	**AD13**

SATA_TX3N	**AE13**
SATA_RX3N	**AB14**
SATA_RX3P	**AC14**
SATA_TX4P	**AE14**
SATA_TX4N	**AD14**
SATA_RX4N	**AD15**
SATA_RX4P	**AE15**
SATA_TX5P	**AB16**
SATA_TX5N	**AC16**
SATA_RX5N	**AE16**
SATA_RX5P	**AD16**
SATA_CAL	**V12**
SATA_X1	**Y12**
SATA_X2	**AA12**
SATA_ACT#/GPIO67	**W11**
SATA_IS0#/GPIO10	**AE18**
SMARTVOLT1/SATA_IS2#/ GPIO4	**AA19**
CLK_REQ0#/SATA_IS3#/ GPIO0	**W17**
CLK_REQ1#/SATA_IS4#/ FANOUT3/GPIO39	**V17**
CLK_REQ2#/SATA_IS5#/ FANIN3/GPIO40	**W20**
CLK_REQ3#/SATA_IS1#/ GPIO6	**AD18**
HD Audio Interface	
AZ_BITCLK	**M1**
AZ_SDOUT	**M2**
AZ_SYNC	**L6**
AZ_RST#	**M4**
AZ_SDIN0/GPIO42	**J7**
AZ_SDIN1/GPIO43	**J8**
AZ_SDIN2/GPIO44	**L8**
AZ_SDIN3/GPIO46	**M3**
Real Time Clock	
X1	**A3**
X2	**B3**
VBAT	**B2**
RTCCLK	**C3**
INTRUDER_ALERT#	**C2**
Clocks	
14M_X1	**J21**
14M_X2	**J20**
USBCLK/14M_25M_48M_OSC	**C8**
25M_48M_66M_OSC	**L18**
PCIE_RCLKP/NB_LNK_CLKP	**N25**
PCIE_RCLKN/NB_LNK_CLKN	**N24**
NB_DISP_CLKP	**K23**
NB_DISP_CLKN	**K22**
NB_HT_CLKP	**M24**
NB_HT_CLKN	**M25**
CPU_HT_CLKP	**P17**
CPU_HT_CLKN	**M18**
SLT_GFX_CLKP	**M23**
SLT_GFX_CLKN	**M22**
GPP_CLK0P	**J19**
GPP_CLK0N	**J18**
GPP_CLK1P	**L20**
GPP_CLK1N	**L19**
GPP_CLK2P	**M19**
GPP_CLK2N	**M20**
GPP_CLK3P	**N22**
GPP_CLK3N	**P22**
Hardware Monitor	
FANOUT0/GPIO3	**M8**
FANOUT1/GPIO48	**M5**
FANOUT2/GPIO49	**M7**
CLK_REQ1#/SATA_IS4#/ FANOUT3/GPIO39	**V17**
FANIN0/GPIO50	**P5**
FANIN1/GPIO51	**P8**
FANIN2/GPIO52	**R8**
CLK_REQ2#/SATA_IS5#/ FANIN3/GPIO40	**W20**
TEMP_COMM	**C6**
TEMPIN0/GPIO61	**B6**
TEMPIN1/GPIO62	**A6**
TEMPIN2/GPIO63	**A5**
TEMPIN3/TALERT#/GPIO64	**B5**
VIN0/GPIO53	**A4**
VIN1/GPIO54	**B4**
VIN2/GPIO55	**C4**
VIN3/GPIO56	**D4**
VIN4/GPIO57	**D5**
VIN5/GPIO58	**D6**
VIN6/GPIO59	**A7**
VIN7/GPIO60	**B7**
AVDD	**F6**
AVSS	**G7**
SPI ROM Interface	
SPI_DI/GPIO12	**G6**
SPI_DO/GPIO11	**D2**
SPI_CLK/GPIO47	**D1**
SPI_HOLD#/GPIO31	**F4**

SPI_CS1#/GPIO32	**F3**
SPI_CS2#/IMC_GPIO2	**H21**
NB / Power Mgmt	
SLP_S2/GPM9#	**H7**
SLP_S3#	**F5**
SLP_S5#	**G1**
PWR_BTN#	**H2**
PWR_GOOD	**H1**
SUS_STAT#	**K3**
TEST0	**H3**
TEST1	**H4**
TEST2	**H5**
Integrated Micro-controller	
IMC_GPIO0	**H19**
IMC_GPIO1	**H20**
SPI_CS2#/IMC_GPIO2	**H21**
IDE_RST#/F_RST#/IMC_GPO3	**F25**
IMC_GPIO4	**D22**
IMC_GPIO5	**E24**
IMC_GPIO6	**E25**
IMC_GPIO7	**D23**
IMC_GPIO8	**A18**
IMC_GPIO9	**B18**
IMC_PWM0/IMC_GPIO10	**F21**
SCL2/IMC_GPIO11	**D21**
SDA2/IMC_GPIO12	**F19**
SCL3_LV/IMC_GPIO13	**E20**
SDA3_LV/IMC_GPIO14	**E21**
IMC_PWM1/IMC_GPIO15	**E19**
IMC_PWM2/IMC_GPO16	**D19**
IMC_PWM3/IMC_GPO17	**E18**
IMC_GPIO18	**G20**
IMC_GPIO19	**G21**
IMC_GPIO20	**D25**
IMC_GPIO21	**D24**
IMC_GPIO22	**C25**
IMC_GPIO23	**C24**
IMC_GPIO24	**B25**
IMC_GPIO25	**C23**
IMC_GPIO26	**B24**
IMC_GPIO27	**B23**
IMC_GPIO28	**A23**
IMC_GPIO29	**C22**
IMC_GPIO30	**A22**
IMC_GPIO31	**B22**
IMC_GPIO32	**B21**
IMC_GPIO33	**A21**
IMC_GPIO34	**D20**

IMC_GPIO35	**C20**
IMC_GPIO36	**A20**
IMC_GPIO37	**B20**
IMC_GPIO38	**B19**
IMC_GPIO39	**A19**
IMC_GPIO40	**D18**
IMC_GPIO41	**C18**
General Events	
RI#/EXTEVNT0#	**E2**
LPC_SMI#/EXTEVNT1#	**K24**
GA20IN/GEVENT0#	**Y15**
KBRST#/GEVENT1#	**W15**
SMBALERT#/THRMTRIP#/ GEVENT2#	**J6**
LPC_PME#/GEVENT3#	**K4**
PCI_PME#/GEVENT4#	**E1**
S3_STATE/GEVENT5#	**F1**
USB_OC6#/IR_TX1/GEVENT6#	**B9**
DDR3_RST#/GEVENT7#	**G5**
WAKE#/GEVENT8#	**H6**
USB_OC0#/GPM0#	**E4**
USB_OC1#/GPM1#	**F8**
USB_OC2#/GPM2#	**E5**
USB_OC3#/IR_RX1/GPM3#	**A9**
USB_OC4#/IR_RX0/GPM4#	**A8**
USB_OC5#/IR_TX0/GPM5#	**B8**
BLINK/GPM6#	**F2**
SYS_RESET#/GPM7#	**J2**
AZ_DOCK_RST#/GPM8#	**L5**
SLP_S2/GPM9#	**H7**
SM Bus	
SCL0/GPOC0#	**AA18**
SDA0/GPOC1#	**W18**
SCL1/GPOC2#	**K1**
SDA1/GPOC3#	**K2**
SCL2/IMC_GPIO11	**D21**
SDA2/IMC_GPIO12	**F19**
SCL3_LV/IMC_GPIO13	**E20**
SDA3_LV/IMC_GPIO14	**E21**
General Purpose I/O	
CLK_REQ0#/SATA_IS3#/ GPIO0	**W17**
SPKR/GPIO2	**W21**
FANOUT0/GPIO3	**M8**
SMARTVOLT1/SATA_IS2#/ GPIO4	**AA19**
SMARTVOLT2/SHUTDOWN#/ GPIO5	**Y19**

CLK_REQ3#/SATA_IS1#/ GPIO6	**AD18**
NB_PWRGD	**W14**
DDC1_SDA/GPIO8	**Y18**
DDC1_SCL/GPIO9	**AA20**
SATA_IS0#/GPIO10	**AE18**
SPI_DO/GPIO11	**D2**
SPI_DI/GPIO12	**G6**
LAN_RST#/GPIO13	**U15**
ROM_RST#/GPIO14	**J1**
IDE_D0/GPIO15	**AD24**
IDE_D1/GPIO16	**AD23**
IDE_D2/GPIO17	**AE22**
IDE_D3/GPIO18	**AC22**
IDE_D4/GPIO19	**AD21**
IDE_D5/GPIO20	**AE20**
IDE_D6/GPIO21	**AB20**
IDE_D7/GPIO22	**AD19**
IDE_D8/GPIO23	**AE19**
IDE_D9/GPIO24	**AC20**
IDE_D10/GPIO25	**AD20**
IDE_D11/GPIO26	**AE21**
IDE_D12/GPIO27	**AB22**
IDE_D13/GPIO28	**AD22**
IDE_D14/GPIO29	**AE23**
IDE_D15/GPIO30	**AC23**
SPI_HOLD#/GPIO31	**F4**
SPI_CS1#/GPIO32	**F3**
INTE#/GPIO33	**AD3**
INTF#/GPIO34	**AC4**
INTG#/GPIO35	**AE2**
INTH#/GPIO36	**AE3**
SERIRQ	**V15**
CLK_REQ1#/SATA_IS4#/ FANOUT3/GPIO39	**V17**
CLK_REQ2#/SATA_IS5#/ FANIN3/GPIO40	**W20**
PCICLK5/GPIO41	**T3**
AZ_SDIN0/GPIO42	**J7**
AZ_SDIN1/GPIO43	**J8**
AZ_SDIN2/GPIO44	**L8**
AZ_SDIN3/GPIO46	**M3**
SPI_CLK/GPIO47	**D1**
FANOUT1/GPIO48	**M5**

FANOUT2/GPIO49	**M7**
FANIN0/GPIO50	**P5**
FANIN1/GPIO51	**P8**
FANIN2/GPIO52	**R8**
VIN0/GPIO53	**A4**
VIN1/GPIO54	**B4**
VIN2/GPIO55	**C4**
VIN3/GPIO56	**D4**
VIN4/GPIO57	**D5**
VIN5/GPIO58	**D6**
VIN6/GPIO59	**A7**
VIN7/GPIO60	**B7**
TEMPIN0/GPIO61	**B6**
TEMPIN1/GPIO62	**A6**
TEMPIN2/GPIO63	**A5**
TEMPIN3/TALERT#/GPIO64	**B5**
BMREQ#/REQ5#/GPIO65	**AD7**
LLB#/GPIO66	**C1**
SATA_ACT#/GPIO67	**W11**
LDRQ1#/GNT5#/GPIO68	**AB8**
REQ3#/GPIO70	**AE6**
REQ4#/GPIO71	**AB6**
GNT3#/GPIO72	**AC6**
GNT4#/GPIO73	**AE5**
Reset	
RSMRST#	**D3**
SYS_RESET#/GPM7#	**J2**
Special Power	
V5_VREF	**AE7**
AVDDCK_3.3V	**J16**
AVDDCK_1.2V	**K17**
AVSSCK	**L17**
CKVDD_1.2V_1	**L21**
CKVDD_1.2V_2	**L22**
CKVDD_1.2V_3	**L24**
CKVDD_1.2V_4	**L25**
USB Analog Power	
AVDDTX_0	**A16**
AVDDTX_1	**B16**
AVDDTX_2	**C16**
AVDDTX_3	**D16**
AVDDTX_4	**D17**
AVDDTX_5	**E17**

AVDDRX_0	**F15**
AVDDRX_1	**F17**
AVDDRX_2	**F18**
AVDDRX_3	**G15**
AVDDRX_4	**G17**
AVDDRX_5	**G18**
AVDDC	**E9**
AVSSC	**F9**
USB Analog Ground	
AVSS_USB_1	**A15**
AVSS_USB_2	**B15**
AVSS_USB_3	**C14**
AVSS_USB_4	**D8**
AVSS_USB_5	**D9**
AVSS_USB_6	**D11**
AVSS_USB_7	**D13**
AVSS_USB_8	**D14**
AVSS_USB_9	**D15**
AVSS_USB_10	**E15**
AVSS_USB_11	**F12**
AVSS_USB_12	**F14**
AVSS_USB_13	**G9**
AVSS_USB_14	**H9**
AVSS_USB_15	**H17**
AVSS_USB_16	**J9**
AVSS_USB_17	**J11**
AVSS_USB_18	**J12**
AVSS_USB_19	**J14**
AVSS_USB_20	**J15**
AVSS_USB_21	**K10**
AVSS_USB_22	**K12**
AVSS_USB_23	**K14**
AVSS_USB_24	**K15**
PCI Express® Analog Power	
PCIE_PVDD	**P24**
PCIE_VDDR_1	**P18**
PCIE_VDDR_2	**P19**
PCIE_VDDR_3	**P20**
PCIE_VDDR_4	**P21**
PCIE_VDDR_5	**R22**
PCIE_VDDR_6	**R24**
PCIE_VDDR_7	**R25**
PCI Express® & Other Analog Grounds	
PCIE_CK_VSS_1	**H18**
PCIE_CK_VSS_10	**R16**
PCIE_CK_VSS_11	**R19**
PCIE_CK_VSS_12	**T17**
PCIE_CK_VSS_13	**U18**
PCIE_CK_VSS_14	**U20**
PCIE_CK_VSS_15	**V18**
PCIE_CK_VSS_16	**V20**
PCIE_CK_VSS_17	**V21**
PCIE_CK_VSS_18	**W19**
PCIE_CK_VSS_19	**W22**
PCIE_CK_VSS_2	**J17**
PCIE_CK_VSS_20	**W24**
PCIE_CK_VSS_21	**W25**
PCIE_CK_VSS_3	**J22**
PCIE_CK_VSS_4	**K25**
PCIE_CK_VSS_5	**M16**
PCIE_CK_VSS_6	**M17**
PCIE_CK_VSS_7	**M21**
PCIE_CK_VSS_8	**P16**
PCIE_CK_VSS_9	**P23**
PCIE_PVSS	**P25**
Serial ATA Analog Power	
AVDD_SATA_1	**AA14**
AVDD_SATA_2	**AA15**
AVDD_SATA_3	**AA17**
AVDD_SATA_4	**AB18**
AVDD_SATA_5	**AC18**
AVDD_SATA_6	**AD17**
AVDD_SATA_7	**AE17**
XTLVDD_SATA	**W12**
PLLVDD_SATA	**AA11**
Serial ATA Analog Ground	
AVSS_SATA_1	**T10**
AVSS_SATA_2	**U10**
AVSS_SATA_3	**U11**
AVSS_SATA_4	**U12**
AVSS_SATA_5	**V11**
AVSS_SATA_6	**V14**
AVSS_SATA_7	**W9**
AVSS_SATA_8	**Y9**
AVSS_SATA_9	**Y11**
AVSS_SATA_10	**Y14**
AVSS_SATA_11	**Y17**
AVSS_SATA_12	**AA9**
AVSS_SATA_13	**AB9**
AVSS_SATA_14	**AB11**
AVSS_SATA_15	**AB13**
AVSS_SATA_16	**AB15**
AVSS_SATA_17	**AB17**
AVSS_SATA_18	**AC8**
AVSS_SATA_19	**AD8**

AVSS_SATA_20	**AE8**
Core Power	
VDD_1	**L15**
VDD_2	**M12**
VDD_3	**M14**
VDD_4	**N13**
VDD_5	**P12**
VDD_6	**P14**
VDD_7	**R11**
VDD_8	**R15**
VDD_9	**T16**
3.3V I/O Power	
VDDQ_1	**L9**
VDDQ_2	**M9**
VDDQ_3	**T15**
VDDQ_4	**U9**
VDDQ_5	**U16**
VDDQ_6	**U17**
VDDQ_7	**V8**
VDDQ_8	**W7**
VDDQ_9	**Y6**
VDDQ_10	**AA4**
VDDQ_11	**AB5**
VDDQ_12	**AB21**
IDE I/O Power	
VDD33_18_1	**Y20**
VDD33_18_2	**AA21**
VDD33_18_3	**AA22**
VDD33_18_4	**AE25**
3.3V Standby Power	
S5_3.3V_1	**A17**
S5_3.3V_2	**A24**
S5_3.3V_3	**B17**
S5_3.3V_4	**J4**
S5_3.3V_5	**J5**
S5_3.3V_6	**L1**
S5_3.3V_7	**L2**
1.2V Standby Power	
S5_1.2V_1	**G2**
S5_1.2V_2	**G4**
USB Phy Digital Power	
USB_PHY_1.2V_1	**A10**
USB_PHY_1.2V_2	**B10**
Digital Ground	
VSS_1	**A2**
VSS_2	**A25**
VSS_3	**B1**
VSS_4	**D7**
VSS_5	**F20**
VSS_6	**G19**
VSS_7	**H8**
VSS_8	**K9**
VSS_9	**K11**
VSS_10	**K16**
VSS_11	**L4**
VSS_12	**L7**
VSS_13	**L10**
VSS_14	**L11**
VSS_15	**L12**
VSS_16	**L14**
VSS_17	**L16**
VSS_18	**M6**
VSS_19	**M10**
VSS_20	**M11**
VSS_21	**M13**
VSS_22	**M15**
VSS_23	**N4**
VSS_24	**N12**
VSS_25	**N14**
VSS_26	**P6**
VSS_27	**P9**
VSS_28	**P10**
VSS_29	**P11**
VSS_30	**P13**
VSS_31	**P15**
VSS_32	**R1**
VSS_33	**R2**
VSS_34	**R4**
VSS_35	**R9**
VSS_36	**R10**
VSS_37	**R12**
VSS_38	**R14**
VSS_39	**T11**
VSS_40	**T12**
VSS_41	**T14**
VSS_42	**U4**
VSS_43	**U14**
VSS_44	**V6**
VSS_45	**Y21**
VSS_46	**AB1**
VSS_47	**AB19**
VSS_48	**AB25**
VSS_49	**AE1**
VSS_50	**AE24**